第 27 卷　第 5 期　　　　半 导 体 学 报　　　　Vol. 27　No. 5
2006 年 5 月　　　　CHINESE JOURNAL OF SEMICONDUCTORS　　　　May, 2006

Alloy Temperature Dependence of Offset Voltage and Ohmic Contact Resistance in Thin Base InGaP/GaAs HBTs*

Yang Wei†, Liu Xunchun, Zhu Min, Wang Runmei, and Shen Huajun

(Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China)

Abstract: The alloy temperature dependence of V_{offset} and $R_{contact}$ is studied, and an optimal alloy temperature range for the best trade-off between V_{offset} and $R_{contact}$ is given for thin base HBTs. In addition, the reason for the high V_{offset} at high alloy temperature is interpreted using Schottky clamped theory. The lower V_{offset} of our U-shaped emitter HBT than that of traditional strip emitter HBTs is explained.

Key words: heterojunction bipolar transistor; U-shaped emitter; alloy; offset voltage
PACC: 7340J　　**EEACC:** 2560F; 2550H; 2550R
CLC number: TN385　　**Document code:** A　　**Article ID:** 0253-4177(2006)05-0765-04

1 Introduction

InGaP/GaAs HBTs have inherent advantages, including low 1/*f* noise, low manufacturing cost, and a reliable fabrication process, that make them attractive for use in MMIC circuits[1~5]. The cutoff frequency f_t of a device is a key parameter that directly confines circuit operation speed[6]. Decreasing the base thickness is an effective way to enhance f_t. In the fabrication of HBTs, a high-temperature alloy process is usually adopted to form an ohmic contact to the collector. It is necessary to consider the influence of high alloy temperature on the thin base HBT. An excessive alloy temperature of the collector metal will induce a high offset voltage (V_{offset}), while an insufficient alloy temperature will be bad for the formation of ohmic contact to the collector, and a bad contact will lead to a high specific contact resistance ($R_{contact}$). An HBT's performance is greatly affected under both conditions[7~9].

In this paper, the alloy temperature dependence of V_{offset} and $R_{contact}$ has been studied. In addition, the reason for the high V_{offset} at high alloy temperature is interpreted using Schottky clamped theory. The lower V_{offset} in our U-shaped emitter HBT than that in traditional strip emitter HBTs is explained by a formula deduced from the fundamental device equation.

2 Experiment

Epitaxial structure plays a key role in an HBT's performance. A 100mm GaAs-substrate epitaxial wafer grown by MBE was provided by the Shanghai Institute of Microsystem and Information Technology of the Chinese Academy of Sciences. The structure of the epitaxial layers is shown in Table 1. A high concentration of indium in the 9th layer helps form a good ohmic contact between the emitter metal and epitaxy layer. The 4th layer, as a base layer, is designed with a thickness of only 40nm to enhance f_t, whereas the normal base layer thickness is over 70nm.

Table 1　Structure of the epitaxial layers

Layer No.	Composition *x*		Thickness / nm	Doping / cm^{-3}	Dopant
9	$In_xGa_{1-x}As$	0.6	50	$>1\times10^{19}$	Si
8	$In_xGa_{1-x}As$	0.6～0	50	$>1\times10^{19}$	Si
7	GaAs		120	5×10^{18}	Si
6	$In_xGa_{1-x}P$	0.5	50	3×10^{17}	Si
5	GaAs		3	Undoped	
4	GaAs		40	4×10^{19}	Be
3	GaAs		2	Undoped	
2	GaAs		150	2×10^{16}	Si
1	GaAs		500	5×10^{18}	Si
SI GaAs substrate					

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* Project supported by the Knowledge Innovation Engineering of the Chinese Academy of Sciences (No. KGX2-101)

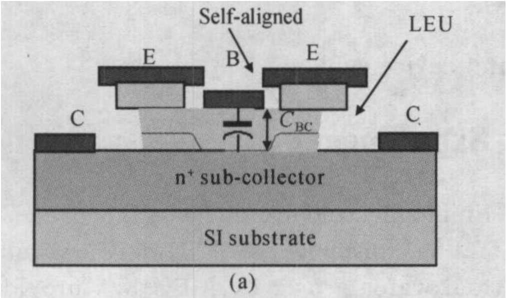
† Corresponding author. Email: weiyang@ustc.edu

Received 15 November 2005, revised manuscript received 17 February 2006

In the device fabrication, the key process involved a self-aligned U-shaped emitter, a lateral etched undercut (LEU), a high temperature alloy, etc.

In the self-aligned emitter, the emitter metal acts as the mask for etching the emitter and as a shield in depositing the base metal.

The majority of the extrinsic base-collector junction area is removed by LEU[10] with a selective etchant. This means that C_{bc}, a main nonlinear factor in HBTs, is greatly reduced in U-shaped emitter HBTs, compared to traditional strip HBTs[11]. The profiles of U-shaped emitter and traditional strip emitter HBTs are shown in Fig. 1.



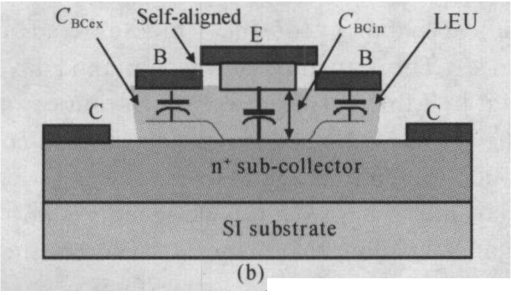


Fig. 1 Comparative profiles of U-shaped emitter and traditional strip emitter HBTs (a) U-shaped emitter; (b) Strip emitter

To find a proper alloy temperature for the thin base HBT, an experiment is conducted in a temperature range from 360 to 420 ℃, and V_{offset} and R_c are measured.

3 Results and discussion

The ohmic contact resistance is measured using the transmission line method. The results are shown in Fig. 2. The specific contact resistance of the metal-semiconductor contact ($R_{contact}$) is about $6 \times 10^{-6} \Omega \cdot cm^2$. $R_{contact}$ varies slowly with temperature, but it increases faster as the temperature falls below 390 ℃, and almost reaches $1 \times 10^{-5} \Omega \cdot cm^2$ at 360 ℃. Therefore, we think the alloy should be carried out above 390 ℃.

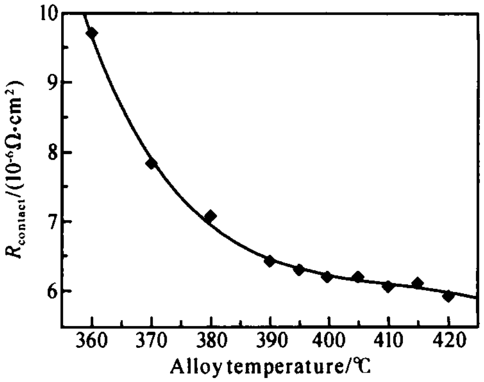


Fig. 2 Alloy temperature dependence of $R_{contact}$

The alloy temperature dependence of V_{offset} is shown in Fig. 3. The symbols are the experimental results, and the solid line is the fitting curve. V_{offset} increases slowly from 0.085 to 0.09V when the alloy temperature increases from 360 to 390 ℃. But when the temperature exceeds 400 ℃, V_{offset} increases dramatically, and reaches a very high value, 0.32V, in 420 ℃.

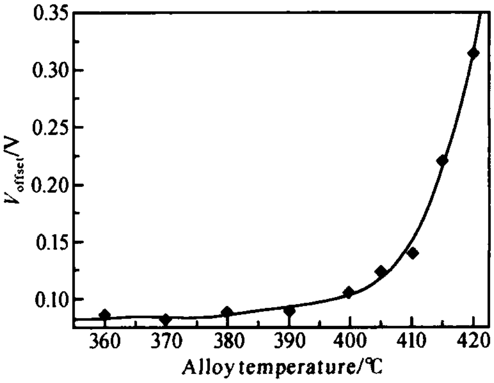


Fig. 3 Alloy temperature dependence of V_{offset} from 360 to 420 ℃

First, from the experimental results shown above, we can conclude that the optimal alloy temperature for a thin base HBT is between 390 and 400 ℃, for the best trade-off between V_{offset} and R_c.

Second, the high V_{offset} can be understood with Schottky clamped theory[12]. In a high temperature alloy, the base contact metal might penetrate the base layer and reach the collector area. Then a Schottky diode is formed between the base and the collector. As shown in Fig. 4, a Schottky diode is parallel to the normal base-collector p-n junction. Then the transistor is said to be " Schottky clamped". Since the turn-on voltage of a Schottky diode is lower than that of the p-n junction, V_{offset} is larger when Schottky clamping occurs. As V_{offset} and hence V_{knee} increase, the output power and power efficiency of the device decrease, which are harmful to the power amplifier with a low power supply.

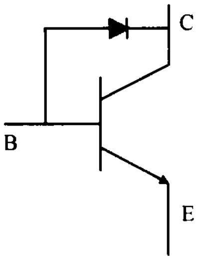


Fig. 4 Schottky clamped HBT

Another characteristic of the U-shaped HBT is that the value of V_{offset} is only about 0.09V, while that of a traditional strip emitter HBT is about 0.15V or higher[11]. InGaP/GaAs HBTs have received much attention due to their inherent advantages, including better DC and AC performance, noise figure properties, and reliability than AlGaAs/GaAs HBTs. However, a disadvantage of InGaP/GaAs HBT is its larger offset voltage[9]. The lower V_{offset} of the U-shaped emitter HBT is attributed to the U-shaped layout structure and LEU technology. As can be seen in Fig. 1, the effective base-collector area of the U-shaped emitter HBT is greatly reduced. Base-collector junction capacitors (C_{bc}) measured using ICCAP also de-monstrate a reduction in U-shaped HBTs. Liu[12] studied the relation between V_{offset} and the area ratio A_c/A_e for graded HBTs, where A_c and A_e are the collector and emitter areas, respectively. But abrupt HBTs have not been discussed. From fundamental physical relations, V_{offset} can be computed by[12]

$$V_{offset} = \frac{\eta_{bc} kT}{q}\ln\left(\frac{I_{cs}}{\alpha_f I_{es}}\right) + \frac{\eta_{bc}}{\eta_{be}} I_b R_e + \left(1 - \frac{\eta_{bc}}{\eta_{be}}\right)(V_{be} - I_b R_b) \quad (1)$$

where I_{cs} and I_{es} are the base-collector diode saturation current and base-emitter diode saturation current, respectively. η_{be} and η_{bc} are the ideality factors of the emitter current in the reverse-active mode and of the collector current in the forward-active mode, respectively, and α_f is the forward current transfer ratio. The first term of Eq. (1) is dominant in determining V_{offset}. Since the α_f, I_{cs}, and I_{es} are defined as follows:

$$I_{es} = \frac{qp_{e0} A_e D_{pe}}{L_E} + \frac{qn_{b0} A_e D_{nb}}{L_B}\coth(X_b/L_b) \quad (2)$$

$$I_{cs} = \frac{qp_{c0} A_c D_{pc}}{L_C} + \frac{qn_{b0} A_e D_{nb}}{L_B}\coth(X_b/L_b) \quad (3)$$

$$\alpha_f = \frac{1}{I_{es}} \times \frac{qn_{b0} A_e D_{nB}}{L_b}\coth(X_b/L_b) \quad (4)$$

From the above four equations, we get:

$$V_{offset} = \frac{\eta_{bc} kT}{q}\ln\left(1 + \frac{A_c}{A_e} \times \frac{L_b p_{c0} D_{pc}}{L_c n_{b0} D_{nb}}\right) + \frac{\eta_{bc}}{\eta_{be}} I_b R_e + \left(1 - \frac{\eta_{bc}}{\eta_{be}}\right)(V_{be} - I_b R_b) \quad (5)$$

$$L_c = \sqrt{D_{pc}\tau_c} \quad (6)$$

$$L_b = \sqrt{D_{nB}\tau_b} \quad (7)$$

$$D_n = \frac{kT}{e}\mu \quad (8)$$

where L_b is the minority electron diffusion length in the base and L_c is the minority hole diffusion length in the collector. Equation (5) shows that V_{offset} increases with A_c/A_e. Since the other parameters in Eq. (5) are mainly determined by epitaxial material, A_c/A_e, which is determined by layout, is the only variable. Calculations using Eq. (5) show a rough difference of 0.05V between the U-shaped emitter HBT and the traditional strip emitter HBT, which roughly agrees with the experimental results. There is still some error between the computations and experimental results, which may be caused by the fabrication process of the HBT.

4 Conclusion

For the best trade-off between V_{offset} and $R_{contact}$, a temperature in the range from 390 to 400 ℃, is appropriate for the alloy of thin base HBTs. High V_{offset} at high alloy temperatures can be interpreted using Schottky clamped theory. The lower V_{offset} in our U-shaped emitter HBT than in traditional strip emitter HBTs is attributed to the lower A_c/A_e. This further demonstrates the superiority of U-shaped emitters, which was shown by Bai *et al*.[10] with high f_t and f_{max}.

Acknowledgements The author would like to thank Wang Suqin, Wang Ning, Liu Hongmin, Wu Jin, and Ma Xiaolin, for their enthusiastic help with

this research.

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合金温度对薄基区 InGaP/GaAs 残余电压和欧姆接触的影响[*]

杨 威[†] 刘训春 朱 旻 王润梅 申华军

(中国科学院微电子研究所, 北京 100029)

摘要: 研究了薄基区 HBT 合金温度对残余电压 V_{offset} 和欧姆接触电阻 $R_{contact}$ 的影响, 给出了薄基区 HBT 的最佳合金温度区域. 用肖特基钳位理论解释了合金温度过高导致 V_{offset} 偏大的现象. 从晶体管基本物理机制推导出 V_{offset} 与集电极、发射极面积比 A_c/A_e 的关系, 并用此解释了 U 形发射极 HBT 具有较小 A_c/A_e 的原因, 进一步证明了 U 型发射极结构的优越性.

关键词: 异质结双极型晶体管; U 形发射极; 合金; 残余电压

PACC: 7340J **EEACC**: 2560F; 2550E; 2550R

中图分类号: TN385 **文献标识码**: A **文章编号**: 0253-4177(2006)05-0765-04

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[*] 中国科学院知识创新工程资助项目(批准号: KGX2-101)

[†] 通信作者. Email: weiyang@ustc.edu

2005-11-15 收到, 2006-02-17 定稿