Bias Current Compensation Method with 41. 4 % Standard Deviation Reduction to MOSFET Transconductance in CMOS Circuits *

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Abstract: A simple and successful method for the stability enhancement of integrated circuits is presented. When the process parameters, temperature, and supply voltage are changed, according to the simulation results, this method yields a standard deviation of the transconductance of MOSFETs that is 41. 4 % less than in the uncompensated case. This method can be used in CMOS LC oscillator design.

Key words: CMOS; transconductance; integrated circuits; transistor
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1 Introduction

Random fluctuations of the manufacturing process parameters due to the non-uniformity of the processing steps and environmental operating conditions such as supply voltage and temperature cause circuit performance parameters to spread around their nominal values. Integrated circuits (IC) need to be robust with respect to such process, voltage, and temperature (PVT) variations to avoid parametric yield loss[1].

In this paper, we propose a current compensation method to reduce the variation of the transconductance (g_m) of MOSFETs with PVT variations, therefore to improve the LC oscillator performance. The same method can be used in other circuits that require transistors with a steady g_m.

2 Proposed bias compensation circuits

In some kinds of circuits, such as LC oscillators, the g_m of transistors is a key parameter[2]. Figure 1 shows an LC oscillator circuit and its steady state equivalent, where the conductance g_{tank} represents the tank loss and $-g_{active}$ is the effective negative conductance of the active devices that compensates the losses in the tank. According to oscillator phase noise theory, the optimal phase noise performance appears when $-g_{active}$ is chosen to be the optimal value $-g_{opt}$. As $-g_{active}$ varies with PVT, the phase noise performance leaves the optimal point in real operation. There more deviation there is in $-g_{active}$, the poorer the phase noise performance becomes. Therefore, it is important to reduce the deviation of $-g_{active}$ with PVT changes.

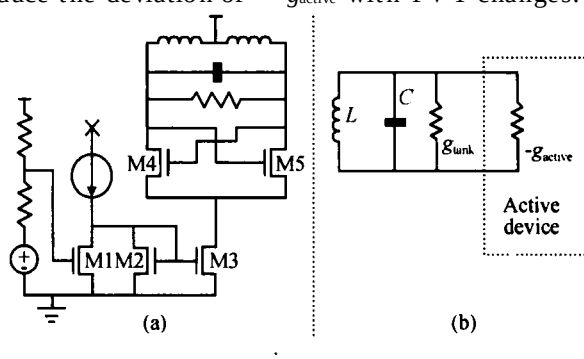

Fig. 1 Schematic (a) and equivalent circuit (b) of an LC oscillator

Figure 2 (a) shows a current mirror widely used as a current bias, and (b) shows a current mirror with compensation. MN4 is the transistor whose transconductance needs to be fixed, MN2 and MN3 compose the current mirror of the bias, and MN1, R_1, and R_2 are the compensation circuit we propose. The drain current (I_{ds}) and g_m of a

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transistor[3] can be expressed as

$$I_{ds} = \frac{1}{2} K(V_{gs} - V_{th})^2 (1 + \lambda V_{ds}) \quad (1)$$

and

$$g_m = K(V_{gs} - V_{th})(1 + \lambda V_{ds}) = \sqrt{2 K I_{ds} (1 + \lambda V_{ds})} \quad (2)$$

K, λ, and V_{th} vary when the process varies. For example, in an nMOS transistor of ST 0.13μm process, K is 13.4m, 15.89m, and 11.35m in TT, FF, and SS corners, respectively. It varies by about ±17%. Then according to the simulation, V_{th} varies by about ±7.3% when the process changes. Both of these variations affect I_{ds} and g_m. In the next section, we will analyze how the assistant circuit operates and why it reduces the transconductance fluctuation of MN4.

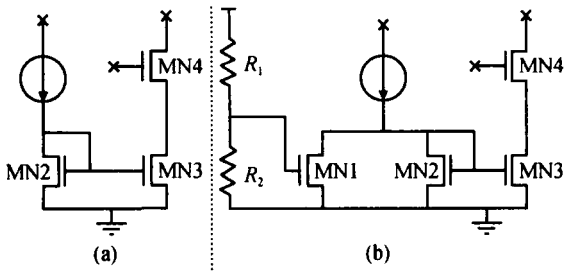

Fig. 2 Two bias current schemes for an nMOS transistor (a) Original one without compensation; (b) Improved one with compensation

First, we suppose that K increases due to the process variations. For simplicity, the channel length modulation is omitted. We can see that if $I_{ds,MN2}$ is not changed, $I_{ds,MN4}$ is not changed, either. According to Eq. (2), $g_{m,MN4}$ will increase with K, which is the case of the circuit in Fig. 2(a). Turning to Fig. 2(b), we get another story. Because $V_{gs,MN1}$ is constant and $I_{ds,MN1}$ increases with the decrease of K and $I_{ds,MN2}$. This compensates the increase of K and depresses the increase of the g_m of MN4. With careful design, the g_m of MN4 may even remain constant. The compensation circuit also works when K decreases.

Second, if the threshold voltage V_{th} decreases with process variations, then as shown in Fig. 2(a), according to Eq. (2), $V_{gs,MN2}$ decreases to keep $I_{ds,MN2}$ fixed, and we can easily get from Eq. (1) that $V_{gs,MN2} - V_{th}$ increases because of the decrease of $V_{ds,MN2} = V_{gs,MN2}$. Therefore $V_{gs,MN3} - N_{th}$, $I_{ds,MN3}$, $I_{ds,MN4}$, and g_m of MN4 all increase. When an auxiliary circuit is added in Fig. 2(b), $I_{ds,MN1}$ increases with the decrease of V_{th}, and $I_{ds,MN2}$ drops down, which reduces the associated $I_{ds,MN3}$ and $I_{ds,MN4}$. Therefore the increase of the g_m of MN4 due to the decrease of the threshold voltage is effectively reduced. Similar to the variation of K, the auxiliary circuits work when V_{th} increases.

Finally, let's refer to the power supply voltage variation of the circuits. If the voltage of the power supply increases, the voltage between the drains and sources of MN3 and MN4 increases, and the drain current of MN4 in Fig. 2(a) also increases. Therefore the g_m of MN4 increases. In Fig. 2(b), the increase of voltage boosts $V_{gs,MN1}$, and thus $I_{ds,MN1}$ increases. Just as mentioned above, the increase of $I_{ds,MN1}$ decreases the drain current of MN3 and MN4, therefore it depresses the increment of the g_m of MN4 to a certain degree.

When pMOS and CMOS circuits are involved, a similar compensation can be added as shown in Fig. 3.

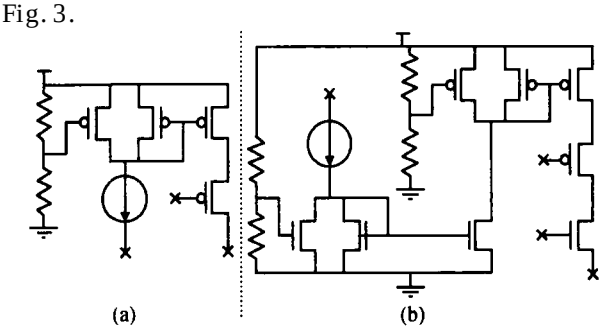

Fig. 3 Bias current compensation for pMOS (a) and CMOS (b) transistors

3 Simulation results

In this section, an example is carried out to show the compensation effect in oscillator design. The circuit is designed using a 1.2V ST HCMO9RF process[4]. Figure 1(a) is an nMOS LC oscillator, and g_{active} in Fig. 1(b) is g_m of M4 and M5. The compensation circuit is a little different from that in Fig. 2(b), i.e., a fixed voltage source is added between the two bias resistors to optimize the supply voltage compensation.

First, we set the power supply at 1.2V and the temperature at 27 ℃, and then run a corner simulation. The transistor corners are "fast", "typical", and "slow", and the resistor corners are "max", "typical", and "min". For a typical design, the output voltage of a band-gap voltage reference varies less than ±2%, and we also add the variation to

the corner simulation. The simulation result is shown in Fig. 4 (a) . We can see that the performance of compensated circuits varies less than that of an un-compensated one. In the second simulation ,we set the circuit device in a typical corner and the temperature at 27 ℃,and vary the supply power voltage by ±10 %. The voltage is set at 1. 08 ,1. 2 ,and 1. 32V ,and the simulation result is shown in Fig. 4 (b) . We can see that the proposed circuits can suppress variation of supply power voltage. Then we set the voltage and device parameters to normal values and run the simulation at different temperatures. The result is shown Fig. 4 (c) ,from which we can see that the proposed circuit can also suppress variation of temperature. Finally ,setting the voltage of the power supply at 1. 08 ,1. 2 ,and 1. 32V ,we simulate the circuits at temperatures of 0 ,27 ,and 70 ℃and transistor corners of typical ,fast ,and slow. Because resistors and a band-gap voltage reference are added in the compensation circuits ,their parameters change with the process. The simulation is carried out to cover the resistor in “typical ”,“max ”, and “min ” corners with the voltage reference varying by ±2 %. The simulation result of the transconductance of M4 in all possible corners in compensated and un-compensated circuits is shown in Fig. 5. The average g_m of M4 is 6. 1mS. It changes from 5. 1 to 7. 0mS in un-compensated circuits ,while this range in compensated circuits is 5. 4 to 6. 5mS ,which is 42 % less. The standard deviation g_m of the original un-compensated circuits is 0. 538mS , while that of compensated circuits reduces to 0. 288mS ,which is 46. 5 % less.

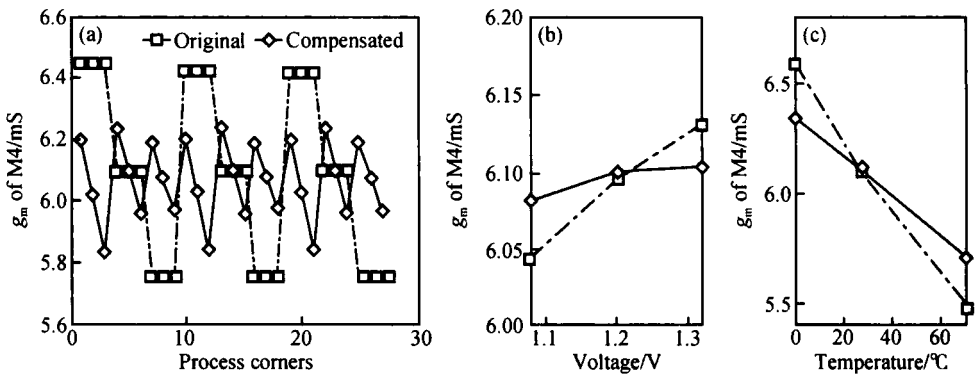

Fig. 4　Conner simulation

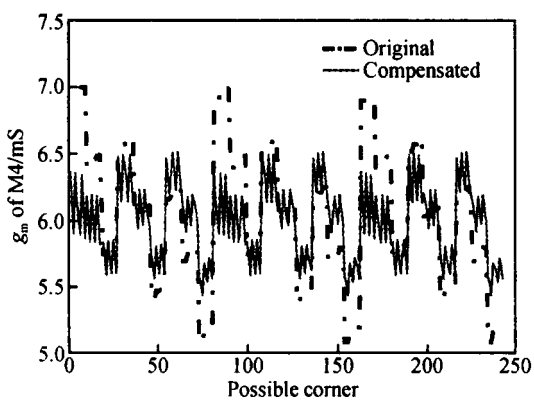

Fig. 5　Simulation results of the transconductance of M4 in all possible corners in compensated and un-compensated circuits

If the band-gap voltage reference is replaced by a diode ,the circuit becomes more simple. But the uncertain variation of $V_{gs,MN1}$ will increase ,and the compensation will be less efficient. Another simulation is carried out by replacing the voltage reference with a diode ,and the standard deviation of g_m reduces to 0. 315mS ,41. 4 % less than the un-compensated case.

4　Conclusion

We have presented a simple and successful method for enhancing the stability of circuits. When the temperature ,the supply voltage ,and the process parameters are changed ,this method can be used to keep the g_m of the circuits in a certain range that is smaller than those without applying our proposed method. This can make the circuits more robust ,and then the yield will be enhanced. It can be used ,but not only in oscillator design.

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用于降低 CMOS 集成电路中晶体管跨导标准差的偏置电流补偿电路*

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摘要: 介绍一种简单而有效的提高集成电路稳定性的电路补偿方法. 当电路制造过程中的工艺参数、工作电压或工作温度发生变化时, 根据仿真结果, 该方法可以使 MOS 晶体管跨导的标准差比未经补偿的电路降低 41.4%. 这种电路可以用于 CMOS LC 振荡器中.

关键词: CMOS; 跨导; 集成电路; 晶体管

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