Design and Analysis of Analog Front-End of Passive RFID Transponders*

Hu Jianyun†, He Yan, and Min Hao

(*State Key Laboratory of ASIC & Systems, Fudan University, Shanghai* 200433, *China*)

Abstract: An analog front-end of HF passive RFID transponders compatible with ISO/IEC 18000-3 is presented. Design considerations, especially the power transmission in the RFID transponder, are analyzed. Based on these considerations, an analog front-end is presented with novel architecture, high power conversion efficiency, low voltage, low power consumption, and high performance in an environment of noise and power fluctuation. The circuit is implemented in a Chartered 0.35μm standard CMOS process. The experimental results show that the chip can satisfy the design target well.

Key words: RFID; analog front-end; power transmission; architecture; low power
EEACC: 2570D
CLC number: TN402 **Document code**: A **Article ID**: 0253-4177(2006)06-0999-07

1 Introduction

In recent years, RFID (radio frequency identification)[1] has received much attention for its increasing applications in a wide range of areas, including public transportation, supply chain management, access control to buildings, animal tracking, and vehicle security[2,3]. An RFID system mainly comprises an interrogator and a transponder. The transponder is powered by the RF signals transmitted by the interrogator. It deals with the data embedded in the input RF signals and responds by the method of load modulation (HF RFID tag) or modulated backscattering (UHF RFID tag).

A passive RFID transponder with no battery lacks its own power supply, and all power required for its operation must be drawn from the electromagnetic field of the interrogator[1]. To achieve a large operation range without operation error, the transponder must have sufficient power over a large range[4,5]. Therefore high efficiency of power transmission and low power circuit[6] and architecture design are very important for passive RFID transponders. In addition, due to the fact that the transponder is easily influenced by noise and power fluctuations, which are mainly caused by the communication channel and the movement of the transponder in the field, respectively, a special design is needed for better performance. Moreover, it is important for it to be compatible with a standard CMOS process to achieve low cost.

However, conventional RFID transponders[2,4,6~11] cannot satisfy all of the considerations above. In this paper, an HF passive transponder operating at 13.56MHz and compatible with ISO/IEC 18000-3 is presented. It has a novel analog front-end architecture and is optimized for high PCE, low voltage, low power, and high performance in the environment of noise and power fluctuation, and it is compatible with a standard CMOS process. Although the circuit operates at 13.56MHz, most methods for low power and high performance are also suitable for transponders operating at UHF and other bands.

2 Power transmission

The power transmission of an RFID transponder is mainly determined by two factors (Fig. 1). One is the impedance matching between the chip circuits and the antenna. Only when the complex impedance of the antenna and resonant capacitor (Z_{ant_res}) matches that of the chip circuits (Z_{chip}) can the chip achieve maximum power

* Project supported by the National High Technology Research and Development Program of China (No. 2003AA1Z1280)
† Corresponding author. Email: hujy@fudan.edu.cn
Received 30 December 2005, revised manuscript received 19 March 2006

transfer. Therefore, we require that

$$Z_{\text{ant\_res}} = Z^{*}_{\text{chip}} \tag{1}$$

Note that the impedance Z_{chip} may vary with the power absorbed by the chip, so the impedance matching should be pursued assuming the condition of minimum power available for the chip to respond[4,5]. In practical design, the antenna and resonant capacitor can be designed after designing the chip. In addition to the consideration of impedance matching, due to the operation principle of inductive coupling, the design of the antenna and the resonant capacitor should be limited by Eq. (2) to achieve the maximum voltage in the resonant condition.

$$f_{\text{res}} = \frac{1}{2\pi\sqrt{L_{\text{ant}} C_{\text{chip\_res}}}} \tag{2}$$

where the $C_{\text{chip\_res}}$ means the total capacitance, including the resonant capacitance and the equivalent capacitance of the chip.

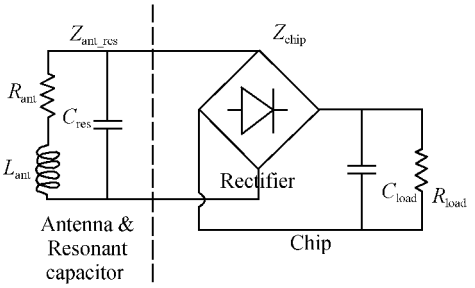

Fig. 1 Power transmission in RFID transponder

The other is the power conversion efficiency (PCE) of the rectifier. The higher the PCE of the rectifier, the more power the rest of the chip can get. Further discussion is presented in Sec. 4.1.

Thus the power of the chip following the rectifier (P_{load}) is

$$P_{\text{load}} = P_{\text{ant}}\,\eta_{\text{impedance}}\,\eta_{\text{rectifier}} \tag{3}$$

where P_{ant} is the power which the antenna receives, $\eta_{\text{impedance}}$ is the power transmission efficiency caused by impedance matching, and $\eta_{\text{rectifier}}$ is the power conversion efficiency of the rectifier.

3 Architecture

As discussed in the above, low power architecture is very important. However, most papers only deal with the conventional architecture[7~10]. Here a novel architecture of the analog front-end circuit is presented (Fig. 2). There are four sub-circuits. Sub-circuit 1 generates voltage and current references, power-on-reset, and supply voltage, which means that the PCE of the related rectifier circuit (Rec1) is very important and should be well optimized. Since sub-circuit 1 is the baseband voltage supply, then unlike conventional transponders, we have put the demodulator separately in sub-circuit 2 to avoid the error operation due to the work of a digital block, where the related rectifier circuit (Rec2) serves as an envelop detector and the demodulator needs to be carefully designed for a large dynamic detective range due to the movement of the transponder in the field of the interrogator. Sub-circuit 3 performs load modulation and cooperates with sub-circuit 1 to avoid large power consumption due to the influence of the charging and discharging of the RF limiter to the storage capacitor. Sub-circuit 4 performs clock extraction and provides a system clock for the digital block. Unlike in UHF transponders[12], in HF transponders the clock can be extracted directly from the antenna.

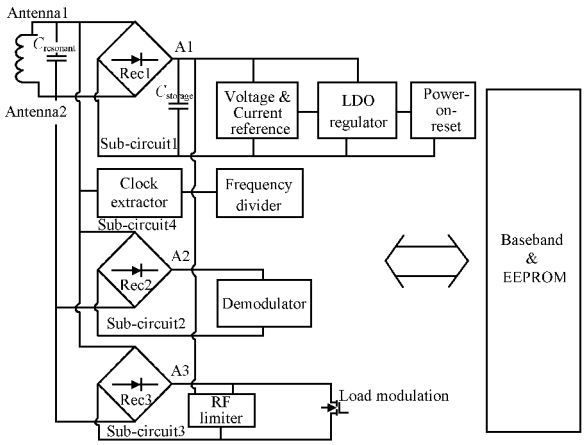

Fig. 2 Architecture of the novel analog front-end circuit

4 Building blocks

4.1 Rectifier

Three rectifier circuits are used in the analog front-end circuit. The advantage of this is that the rectifiers can be optimized separately. As discussed above, the PCE is very important for Rec1. The PCE is mainly reduced by the threshold voltage drop caused by diode-connected MOSFET, power consumption on the channel resistor, and the substrate leakage of the MOSFET transistor

diodes. The last two issues can be addressed by using a MOSFET with a large width-to-length ratio and adaptive substrate biasing techniques[8,13], respectively. The first issue can be addressed by using Schottky diodes[2,11,14]. However, a special process is needed.

Here a new rectifier compatible with a standard CMOS process is proposed (Fig. 3(a)). Unlike conventional full wave bridge rectifier circuits and nMOS gate cross-connected bridge rectifiers, it overcomes the problem of the threshold voltage drop caused by the diode-connected MOSFET. It is derived from the nMOS gate cross-connected bridge rectifier and uses the bootstrapped circuit technique[15].

According to the circuit structure, two states (on and off) can be found (Fig. 3). Here, take MN3 as an example; the analysis is also suitable for MN4 and its bootstrapped circuit. When antenna1 is low and antenna2 is high (see Fig. 3(b)) because the gates of MN8, MN10, MN11, MP9 are connected to anten2, MN8, MN10, and MN11 are on and MP9 is off. As a result, MN3 and MN7 are off. This is the off state. During this state, the bootstrapped capacitor C_b is charged to

$$V_{Cb} = V_{anten2max} - (V_{th} + \sqrt{2I_D/\mu C_{ox}(W/L)}) \quad (4)$$

where $V_{anten2max}$ is the highest voltage in antenna2 during the off state, and the term $V_{th} + \sqrt{2I_D/\mu C_{ox}(W/L)}$ is due to the diode-connected MN11. Here the size of MN11 is optimized to make the circuit have a better performance. When antenna1 is high and antenna2 is low (see Fig. 3(c)) MN8, MN10, and MN11 are off, while MP9, MN7, and MN3 are on. This state is called the on state. During this period, the gate and drain of MN3 are connected across C_b. Note that capacitor C_b and the size of MN3 should be optimized, since the parasitic capacitor of MN3 will redistribute the charge on C_b. In short, before anten1 is high, C_b is charged, and when anten1 is high, C_b can provide a high voltage for MN3's gate to make MN3 on. Therefore, during the on state, the voltage drop between the drain and source approaches zero and the circuit can avoid the threshold voltage drop.

4.2 Voltage and current reference

Here a conventional voltage and current reference [16] is used. A low power start-up circuit[17] is also used to bring out the reference circuit from its dead operating point to its normal operation point. Unlike conventional start-up circuits, the start-up circuit completely turns off once the reference circuit is started, and does not consume current during normal operation.

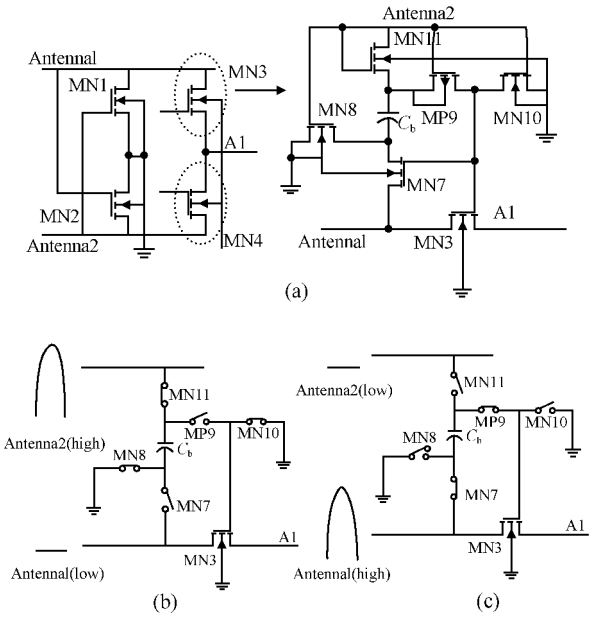

Fig. 3　Proposed rectifier circuit　(a) Circuit implementation; (b) Off state; (c) On state

4.3 Low drop-out (LDO) regulator

In order to avoid extra supply voltage and to reduce the power consumption, an LDO regulator is used to offer multiple supply voltage levels to make each circuit work at a suitable supply voltage. One is for baseband and analog blocks (1.6V), and the other is for EEPROM (1.8V). In addition, an LDO regulator is also used to provide a stable supply voltage. Here, to avoid a large chip area due to the large resistor for low quiescent current, the resistor can be replaced by a diode-connected MOSFET. Also, note that since EEPROM has different current consumptions in the read and erase/write states, the stability of the LDO regulator with different loads requires careful design[18].

4.4 Power-on-reset (POR)

One purpose of the POR is to reset the digital block when the transponder enters the electromagnetic field of the interrogator. Another purpose is to prevent the digital block from error op-

eration when the supply voltage drops below a certain level. Figure 4 shows the structure of the POR circuit. Here, to achieve a low supply current, we optimize branches 1, 2, and 3, which account for most of the power consumption. M5, which is combined with a current mirror, is used to control the current of branch 1 with a small current value (~50nA). MN1 is used to provide a hysteresis function to reduce the influence of the noise and power fluctuation.

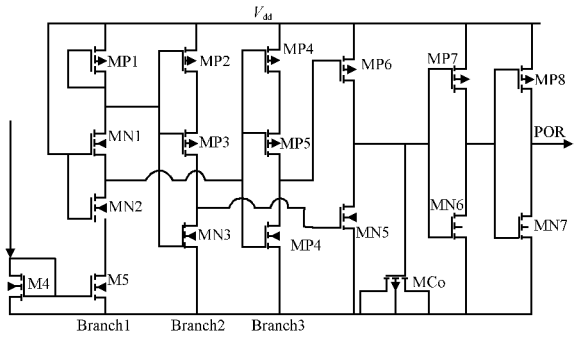

Fig. 4 Power-on-reset circuit

4.5 Clock extractor

As with the POR circuit, the clock extractor also needs a hysteresis function performed by a low power Schmitt trigger[19]. A low pass filter is also added before the Schmitt trigger to reduce the influence of glitches (Fig. 5). Since the clock extractor circuit works at a low voltage, a suitable structure[19] is used, which is modified by adding MP4 to make the Schmitt trigger achieve an initial state. Unlike conventional Schmitt triggers, this Schmitt trigger consumes little supply current during the operation.

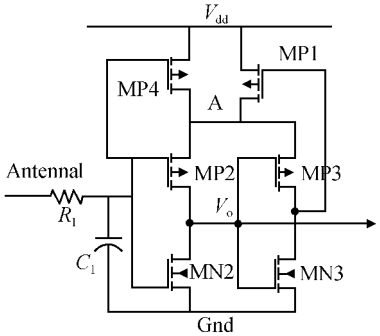

Fig. 5 Clock extractor circuit

4.6 Demodulator

Due to the fact that the transponder is not fixed in the field of the interrogator and can have a large movement range, the output voltage of rectifier Rec2 may vary on a large scale. Therefore, to make the demodulator a large dynamic scale for each kind of voltage, the output of the rectifier is used as the supply voltage of the demodulator, instead of using a fixed voltage (Fig. 6). In addition, the demodulator also uses a low pass filter (R_2-C_2) connected between it and the input of the hysteresis comparator, which is the core of the demodulator. It is also used to reduce the influence of noise and power fluctuations and to generate an inner reference voltage, and the voltage can vary with the output of rectifier Rec2. Note that to prevent demodulation errors caused by overshoot, a two-stage low pass filter (R_1-C_1, R_2-C_2) is used. A buffer powered by V_{dd1} is added after the output of the demodulator to provide a regulated voltage to the digital block.

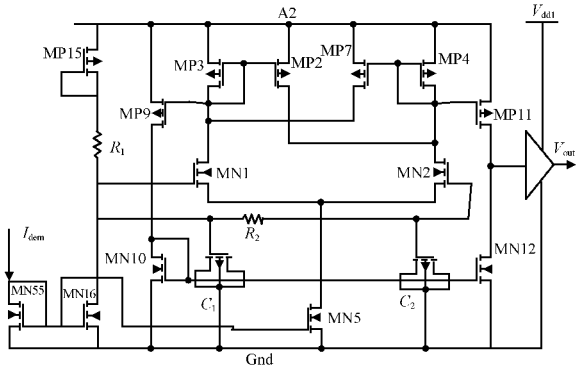

Fig. 6 Demodulator circuit

4.7 RF limiter

When the transponder is near the interrogator, the power received by the antenna can reach a very high level, leading to a high voltage level in the output of rectifier circuit. Thus an RF limiter is used to avoid any damage to the integrated components[9]. The RF limiter works like a shunt regulator, here to avoid large power consumption caused by charging and discharging of the RF limiter to the storage capacitor, and the input and output of the RF limiter are separate, connected to sub-circuit 1 and sub-circuit 4, respectively.

4.8 Load modulation

Conventional load modulation is implemented using a MOSFET switch with a resistor or capacitor, as shown in Fig. 2, and the load modulation is combined with sub-circuit 4 to make use of the ar-

chitecture and achieve a simple implementation.

By turning on or off the load modulation transistor controlled by data, the impedance of the transponder is changed, leading to a different impedance in the interrogator's antenna, which can be demodulated by the interrogator to achieve data transfer from transponder to interrogator[1].

5 Results

The whole analog front-end circuit assembly is implemented in a Chartered 0.35μm standard CMOS process. To achieve better performance, the layout must be given special consideration. Because the rectifiers are the first stage after the antenna and they sometimes receive a large voltage, in order to protect the rectifiers, the layout of transistors in the rectifiers are modified to have a wider drain and source than standard transistors. In addition, because of the inductive coupled operating principle, the guard ring around each module must not be a closed ring to avoid generating current in the guard ring due to inductive coupling with the interrogator. Moreover, there is no electrostatic discharge (ESD) protection on the antenna pads, since ESD protection brings too many parasitics at the antenna and results in power loss[20]. A microphotograph of the chip is shown in Fig. 7.

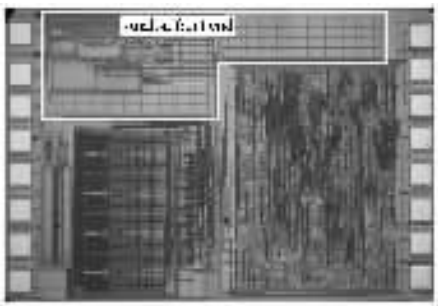

Fig. 7　Microphotograph of analog front-end

The chip is tested with a 13.56MHz interrogator. The test shows that the chip works well and satisfies the design target and the demand of ISO/IEC 18000-3. Experimental results are listed in Fig. 8 for an example. Figure 8(a) shows the antenna signal and rectifier output, which shows that the proposed rectifier can effectively eliminate the threshold voltage drop, leading to a high PCE. Through simulation under the same conditions, the PCE of the proposed rectifier is 70.1%, which is much higher than the conventional one (45.9%). Figure 8(b) shows the

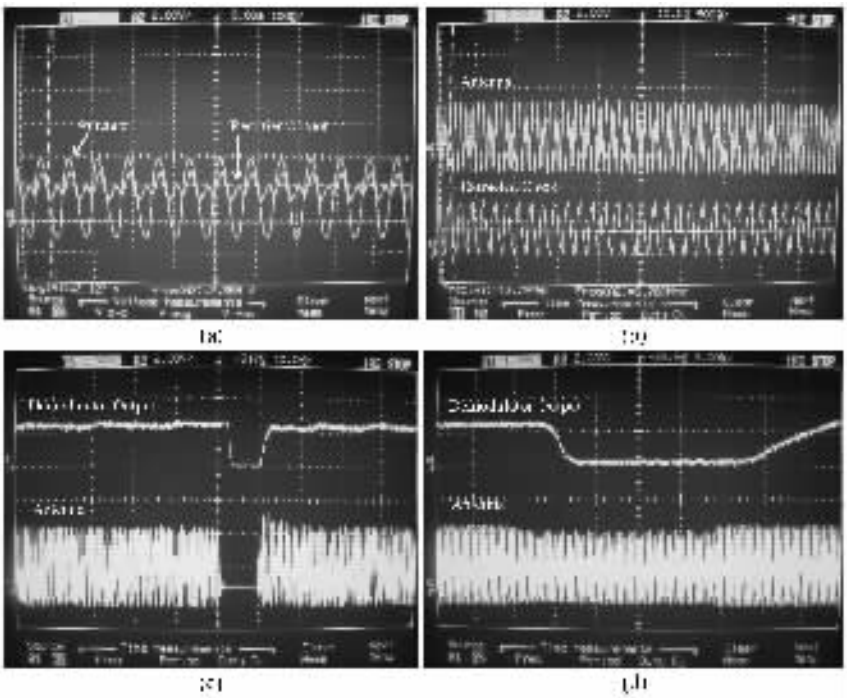

Fig. 8　Experimental results　(a) Antenna signal and rectifier output; (b) Antenna signal and extracted clock; (c) Antenna signal and demodulator output with 100% ASK modulation; (d) Antenna signal and demodulator output with 10% ASK modulation

antenna signal and extracted clock. Figure 8(c) shows the antenna signal and demodulator output with 100% ASK modulation. Figure 8(d) shows the antenna signal and demodulator output with 10% ASK modulation. The simulation shows that the total supply current consumption of the analog front-end is less than 3μA.

6 Conclusion

Implemented in a Chartered 0.35μm standard CMOS process, an analog front-end with a novel architecture of HF passive RFID transponders compatible with ISO/IEC 18000-3 is designed. Experimental and simulation results show that the chip has high power conversion efficiency (PCE), low voltage, low power, and high performance in an environment of noise and power fluctuation and satisfies the design target and the demands of ISO/IEC 18000-3.

References

[1] Finkenzeller K. RFID handbook: fundamentals and applications in contactless smart cards and identification. England: John Wiley & Sons, 2003

[2] Karthaus U, Fischer M. Fully integrated passive UHF RFID transponder IC with 16.7-μW minimum RF input power. IEEE J Solid-State Circuits, 2003, 38(10): 1602

[3] Rao K V S, Nikitin P V, Lam S F. Antenna design for UHF RFID tags: a review and a practical application. IEEE Trans Antennas and Propagation, 2005, 53(12): 3870

[4] Vita G D, Iannaccone G. Design criteria for the RF section of UHF and microwave passive RFID transponders. IEEE Trans Microw Theory Tech, 2005, 53(9): 2978

[5] Rao K V S, Nikitin P V, Lam S F. Impedance matching concepts in RFID transponder design. IEEE Workshop on Advanced Automatic Identification Technologies, 2005, 10: 39

[6] Vita G D, Iannaccone G. Ultra-low-power RF section of a passive microwave RFID transponder in 0.35μm BiCMOS. IEEE International Symposium on Circuits and Systems, 2005, 5: 5057

[7] Li Y, Liu J. A 13.56MHz RFID transponder front-end with merged load modulation and voltage doubler-clamping rectifier circuits. IEEE International Symposium on Circuits and Systems, 2005, 5: 5095

[8] Masui S, Ishii E, Iwawaki T, et al. A 13.56MHz CMOS RF identification transponder integrated circuit with a dedicated CPU. IEEE International Solid-State Circuits Conference, 1999, 2: 162

[9] Kaiser U, Steinhagen W. A low-power transponder IC for high-performance identification systems. IEEE J Solid-State Circuits, 1995, 30(3): 306

[10] Abrial A, Bouvier J, Renaudin M, et al. A new contactless smart card IC using an on-chip antenna and an asynchronous microcontroller. IEEE J Solid-State Circuits, 2001, 36(7): 1101

[11] Strassner B, Chang K. Passive 5.8GHz radio-frequency identification tag for monitoring oil dill pipe. IEEE Trans Microw Theory Tech, 2003, 51(2): 356

[12] Han Yifeng, Li Qiang, Min Hao, et al. A low voltage low power oscillator suitable for RFID transponder. Chinese Journal of Semiconductors, 2005, 26(4): 775(in Chinese)[**韩益锋, 李强, 闵昊, 等. 一种适用于射频电子标签的低电压低功耗振荡器. 半导体学报**, 2005, 26(4): 775]

[13] Ghovanloo M, Najafi K. Fully integrated wideband high-current rectifiers for inductively powered devices. IEEE J Solid-State Circuits, 2004, 39(11): 1976

[14] Li Qiang, Wang Junyu, Han Yifeng, et al. Design and fabrication of Schottky diode with standard CMOS process. Chinese Journal of Semiconductors, 2005, 26(2): 238

[15] San H, Kobayashi H, Myono T, et al. High-efficient low-voltage-operation charge pump circuits using bootstrapped gate transfer switches. T IEE Japan, 2000, 120-C(10): 1339

[16] Allen P E, Holberg D R. CMOS analog circuit design. England: Oxford University Press, Inc, 2002

[17] Khan Q A, Wadhwa S K, Misri K. Low power startup circuits for voltage and current reference with zero steady state current. Proceedings of the International Symposium on Low Power Electronics and Design, 2003, 8: 184

[18] Tantawy R, Brauer E J. Performance evaluation of CMOS low drop-out voltage regulators. The 47th Midwest Symposium on Circuits and Systems, 2004, 1: 1

[19] Al-Sarawi S F. Low power Schmitt trigger circuit. Electron Lett, 2002, 38(18): 1009

[20] Curty J, Joehl N, Dehollain C, et al. Remotely powered addressable UHF RFID integrated system. IEEE J Solid-State Circuits, 2005, 40(11): 2193

无源射频电子标签模拟前端的设计与分析*

胡建赟† 何 艳 闵 昊

（复旦大学专用集成电路与系统国家重点实验室，上海 200433）

摘要：提出了与 ISO/IEC 18000-3 兼容的高频无源射频电子标签模拟前端.分析了设计中的考虑因素,尤其是射频电子标签的能量传输.基于这些分析,提出了一种新架构、高能量转换效率、低电压、低功耗、在噪声和能量波动环境下具有高性能的模拟前端.此电路在 Chartered 0.35μm 标准 CMOS 工艺下实现,测试结果表明芯片能很好地满足设计要求.

关键词：RFID；模拟前端；能量传输；架构；低功耗

EEACC：2570D

中图分类号：TN402　　**文献标识码**：A　　**文章编号**：0253-4177(2006)06-0999-07

* 国家高技术研究发展计划资助项目(批准号:2003AA1Z1280)

† 通信作者.Email:hujy@fudan.edu.cn

2005-12-30 收到,2006-03-19 定稿