A High Performance 0.18μm RF nMOSFET with 53 GHz Cutoff Frequency*

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Abstract: This paper presents the fabrication and performance of a 0.18μm nMOSFET for RF applications. This device features a nitrided oxide/poly-silicon gate stack, a lightly-doped-drain source/drain extension, a retrograde channel doping profile, and a multiple-finger-gate layout, each of which is achieved with conventional semiconductor fabrication facilities. The 0.18μm gate length is obtained by e-beam direct-writing. The device is fabricated with a simple process flow and exhibits excellent DC and RF performance: the threshold voltage of 0.52V, the sub-threshold swing of 80mV/dec, the drain-induced-barrier-lowering factor of 69mV/V, the off-state current of 0.5nA/μm, the saturation drive current of 458μA/μm (for the 6nm gate oxide and the 3V supply voltage), the saturation transconductance of 212μS/μm, and the cutoff frequency of 53GHz.

Key words: structure; process; radio frequency; nMOSFET
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1 Introduction

In recent years, the scaling down of CMOS has led to significant improvements in the RF performance of MOS devices. Consequently, CMOS has become a viable option for analog/RF applications in the multi-GHz frequency range. Compared with the GaAs technology that is widely used in RF applications, CMOS technology has the advantages of a mature process, low cost, and high integration density. The ITRS Roadmap 2003[1] predicted that RF CMOS would be predominant in cost-sensitive RF applications, such as Bluetooth and WLAN, which have been demonstrated tremendous market potential. To date, many RF CMOS products have become available in markets or reached the demonstration stage. RF/mixed signal CMOS circuit fabrication services are also available in mainstream foundries[2~7].

However, in the Chinese mainland, RF CMOS research is far behind that of the international community. In 2004, we reported a 0.25μm SOI RF MOSFET with a 17.78GHz cutoff frequency[8]. This was later improved to 25.6GHz for the same gate length[9]. However, this is still much lower than that of currently available 0.25μm MOSFETs with cutoff frequencies in the 30 ~ 40GHz range[2,4]. With much effort, we have scaled the gate length down to 0.18μm for bulk silicon devices and achieved a 53GHz cutoff frequency in this work. These specifications are comparable to state of the art technologies provided by foundries (40~60GHz)[2,4]. The simple process flow and the DC characteristics of the device are also presented.

2 Structure and fabrication

The starting substrate material was 100mm p-type (001) wafer with a resistivity of 10~20Ω·cm. The main processes were based on the technology platform for 0.1~0.35μm CMOS integrated circuits that was developed at the Institute of Microelectronics of the Chinese Academy of Sciences (IMECAS)[10,11]. Some necessary adjustments were made for RF MOSFETs.

The process flow is shown in Fig. 1. After LOCOS isolation, dual implants (B and BF_2) were used in channel engineering to form a retrograde

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doping profile for the purpose of properly adjusting threshold voltage and suppressing short-channel effects (SCE). The doping profile, obtained with the TSUPREM simulator[12], is shown in Fig. 2. Our use of the e-beam direct-writing technique in combination with wafer pretreatment in plasma of CF_4 is a key for the patterning of the 0.18μm gate, as shown in the inset (a) of Fig. 2. A shallow source/drain (S/D) extension junction with sufficiently high doping is indispensable for slight SCE (short channel effects) and low series S/D resistance, which were obtained by low energy, medium-dose As implantation followed by typical heavy-dose, deep S/D As implantation and RTA (rapid thermal annealing). Ti-salicide with a Ge PAI (pre-amorphous implant) was used to reduce the parasitic resistance of the gate, drain, and source electrodes[11]. Note that the Ge PAI can suppress the $TiSi_2$ narrow line effects since it is the key factor in reducing the sheet resistances, especially for the 0.18μm gate. Additionally, for the layout, as a typical RF MOSFET gate structure, the multi-finger-gate pattern, which is shown in the inset (b) of Fig. 2, was used to further reduce the gate parasitic series resistance.

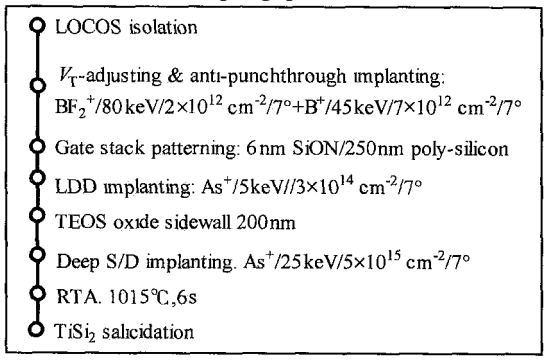


Fig. 1 Process flow for 0.18μm RF nMOSFET

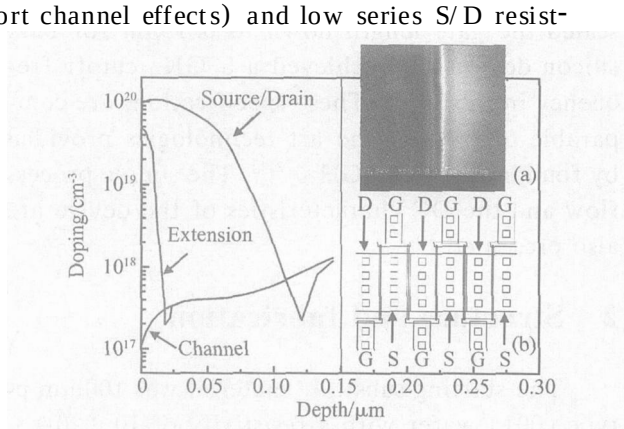
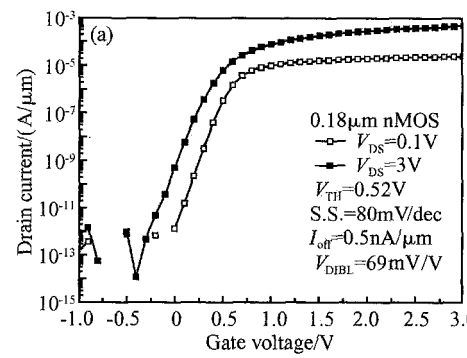


Fig. 2 Simulated doping profiles Insets are SEM image of 0.18μm gate line (a) and multi-finger gate structure (b).

3 Results and discussion

The DC characteristics of the fabricated devices were measured with an HP4145 semiconductor parameter analyzer, and the RF *S*-parameter was measured by an HP8510C vector network analyzer connected to a Cascade Microtech Summit 9000 probe station with ground-signal-ground (GSG) pattern probes. The *Y* parameters (converted from the measured *S* parameters) of the open patterns were subtracted from those of the DUT (device under test) in order to extract the parasitics inserted by the probes and the pads to a certain degree[13].

The transfer characteristics of the 0.18μm nMOSFET, under 0.1 and 3V drain biases, are shown in Fig. 3(a). A threshold voltage of 0.52V is obtained, which is moderate for operation with a 3V supply voltage. The other parameters extracted from this figure include the sub-threshold swing of 80mV/dec, the drain-induced-barrier-lowering



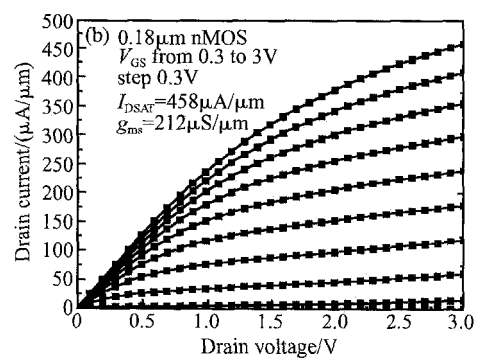


Fig. 3 DC characteristics of 0.18μm RF nMOSFET
(a) Transfer characteristics; (b) Output characteristics

(DIBL) factor of 69mV/V, and the off-state current of 0.5nA/μm. These parameters show that the SCE are well controlled by the dual implant approach combined with the LDD structure.

Figure 3(b) shows the output characteristics of the device. For operation with 3V supply voltage, the saturation drive current of 458μA/μm and the saturation transconductance of 212μS/μm are obtained, which are high enough for the 6nm gate oxide. Clearly, higher drive current and transconductance can be achieved by thinning the gate oxide, which is typically 3nm for 0.18μm technology in foundry services. Additionally, extrapolating the source-to-drain resistance (R_{DS}) of a group of devices with different gate lengths to zero gate length, an extracted parasitic S/D series resistance of ~259Ω·μm is obtained, which is ~30% larger than the prediction for high performance MOSFETs (<200Ω·μm) defined by ITRS 2003[1]. Further improvement may be achieved by adjusting the LDD extension structure (length and doping) or adopting advanced salicidation technologies, such as Ti/Co-, Co-, and Ni-salicidation[11,14].

Extrapolated cutoff frequencies (f_T) are shown in Fig. 4. The extrapolation is from the maximum available frequency of 15GHz and along the dashed line with the slope of -20dB/dec. The de-embedded and DUT cutoff frequencies are 53 and 31GHz, respectively. This indicates that the de-embedding approach is absolutely indispensable for the accurate characterization of RF devices on lossy silicon substrates. The 53GHz cutoff frequency is comparable to state-of-the-art 0.18μm RF CMOS technology[2,4]. However, it should be noted that there is still room for improvement of cutoff frequency since the S/D series resistance could be further reduced as mentioned above.

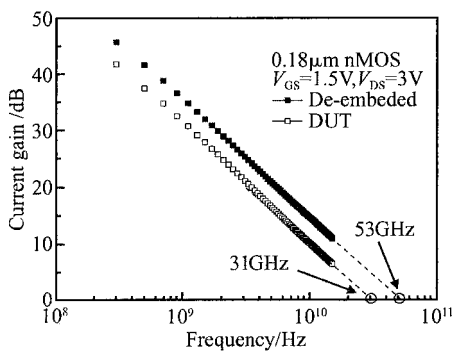


Fig. 4　Current gain versus frequency of 0.18μm nMOSFET

4 Conclusion

In this paper, the structure and process of a 0.18μm nMOSFET have been proposed for RF applications. The device is fabricated with a simple process flow and demonstrates excellent DC characteristics and the high cutoff frequency of 53GHz, which is comparable to current RF CMOS technologies provided by mainstream foundries. This device is promising for multi-GHz RF applications.

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截止频率 53 GHz 的高性能 0.18μm 射频 nMOSFET*

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摘要: 阐述了 0.18μm 射频 nMOSFET 的制造和性能. 器件采用氮化栅氧化层/多晶栅结构、轻掺杂源漏浅延伸结、倒退的沟道掺杂分布和叉指栅结构. 除 0.18μm 的栅线条采用电子束直写技术外, 其他结构均通过常规的半导体制造设备实现. 按照简洁的工艺流程制备了器件, 获得了优良的直流和射频性能: 阈值电压 0.52V, 亚阈值斜率 80mV/dec, 漏致势垒降低因子 69mV/V, 截止电流 0.5nA/μm, 饱和驱动电流 458μA/μm, 饱和跨导 212μS/μm (6nm 氧化层, 3V 驱动电压) 及截止频率 53GHz.

关键词: 结构; 工艺; 射频; nMOSFET
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