Design, Analysis, and Optimization of a CMOS Active Pixel Sensor *

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Abstract: A three-transistor active pixel sensor and its double sampling readout circuit implemented by a switch capacitor amplifier are designed. The circuit is embedded in a 64 ×64 pixel array CMOS image sensor and successfully taped out with a Chartered 0.35μm process. The pixel pitch is 8μm ×8μm with a fill factor of 57%, the photo-sensitivity is 0.8V/(lux ·s), and the dynamic range is 50dB. Theoretical analysis and test results indicate that as the process is scaled down, a smaller pixel pitch reduces the sensitivity. A deep junction n-well/p-substrate photodiode with a reasonable fill factor and high sensitivity are more appropriate for submicron processes.

Key words: CMOS image sensor; active pixel sensor; fill factor; photo-response sensitivity
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1 Introduction

CMOS image sensors (CIS) with active pixel have attracted much attention in the past ten years. The advantages of CIS are: (1) compatibility with standard CMOS processes; (2) low system cost and area due to the on-chip integration of amplifiers, analog-to-digital converters, and timing control circuits; (3) low power consumption since only one row of pixels needs to be active during the readout and it has a low operation voltage; and (4) random access to the image data[1]. The scaling down of the process yields a smaller pixel pitch, higher resolution, and lower power dissipation. Furthermore, a shallow junction and a low power supply voltage reduce the spectral response sensitivity and the signal-to-noise ratio (SNR), respectively[1,2]. Appropriate architectures must be developed to overcome performance deterioration. A three-transistor APS and its double sampling readout circuit are designed and fabricated with a Chartered 0.35μm CMOS process. Based on simulation and test results, the characteristics of fill factor, resolution, photo charge collection, and sensitivity are analyzed. A pixel structure with a reasonable fill factor and sensitivity in a deep submicron process is presented.

2 Photodiode APS circuit and operational sequence

The photodiode (PD) APS and its readout circuit design are shown in Fig. 1. (Logic 1 means gate closed, and logic 0 means gate open.) Each pixel comprises a PD, a reset transistor M1, a source follower transistor M2, and a row-select transistor M3. M4 is the column load transistor of the source follower buffer. The switch capacitor amplifier performs double sampling to reduce fixed pattern noise (FPN). Assuming that the transistors in the pixel have the same threshold voltage V_T, then when the PD is reset (reset = 1, sel = 1), the pixel output voltage is

$$V_{pixel} \approx V_{dd} - 2V_T - \sqrt{I_{bias}/K} \quad (1)$$

where I_{bias} is the bias current of the source follower, and K is $\mu C_{OX}(W/L)/2$ of M4.

Then the reset signal is put high to integrate the photocurrent on the PD. After the integration period is finished, the pixel output is

$$V_{out} \approx V_{dd} - 2V_T - i_{photo}\, t_{int}/C_{diode} - \sqrt{I_{bias}/K} \quad (2)$$

It can be seen from Eq. (2) that the threshold voltage offset of M1 and M2 can affect the output voltage and introduce FPN to the image.

A timing diagram of the APS is also shown in

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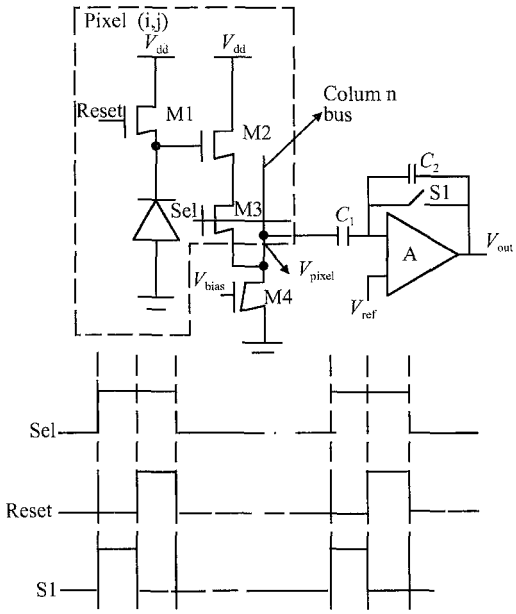

Fig. 1　APS circuit and timing diagram

Fig. 1. The sensor is read out one row at a time, and double sampling is performed by the switch capacitor amplifier. At the end of each row's exposure time, the row select signal sel and amplifier reset signal S1 are put high and the pixel output given by Eq. (2) is sampled by the sampling capacitance C_1. After sampling, the S1 signal is put low, and the reset signal is put high; the pixel enters the reset state, and the amplifier enters the amplification state. At this time, the sel signal remains high, and the sampling capacitor C_1 is also connected to the output of the pixel given by Eq. (1). The output of the amplifier can be written as

$$V_{out} = V_{ref} - \frac{C_1}{C_2}(V_{rst} - V_{sig}) = V_{ref} - \frac{C_1}{C_2}(i_{photo}\, t_{int}/C_{diode} - \sqrt{I_{bias}/K}) \quad (3)$$

The threshold voltage doesn't appear in Eq. (3). The variation of threshold voltage from pixel to pixel is eliminated because the result includes the difference between the reset output and the exposure output of the pixel. The output voltage can be adjusted to an appropriate level by V_{ref} to fit the following process[3].

3　Experiment and results

The three-transistor active pixel sensor and its readout circuit were designed and embedded in a 64 ×64 pixel array CIS with an 8-bit on-chip analog-to-digital converter. The sensor was fabricated with a Chartered 0.35μm CMOS process. A photograph of the chip is shown in Fig. 2.

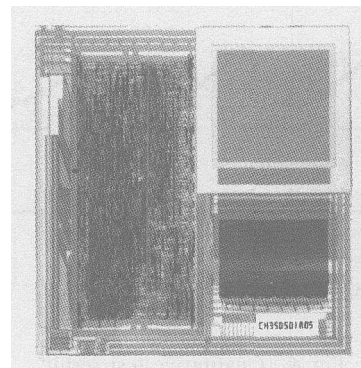

Fig. 2　Photograph of the CIS

The photodiode array is located in the upper right area of the chip. The analog signal processing circuitry is located adjacent to the photodiode array, in the lower right-hand corner of the chip. The timing control for the pixel array and processing circuit is located on the left side of chip. Metal 4 acts as a light shielding layer to reduce the photo charge generated in the non-photosensitive area of the pixel. The readout circuit was tested separately from the PD array with an external electrical stimulus. The performance of the readout circuit was confirmed by simulation and testing. The circuit inserted for testing the pixel is shown in Fig. 3. In the diagram, "buf" is a buffer used to drive a large outside load.

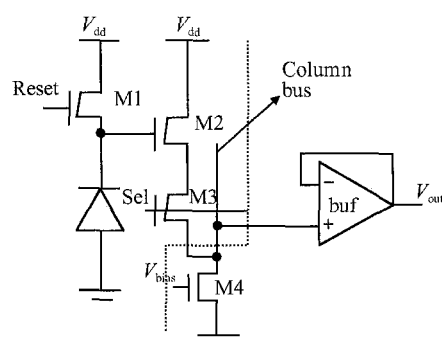

Fig. 3　Test circuit of the pixel

The qualitative test results of the photo response at room light are shown in Fig. 4. The illumination intensity was 800lux, as measured by a luxmeter. The row select signal sel is connected to V_{dd}, and the reset signal is provided by the FPGA

control circuit. The reset time is 500μs, and the output signal is measured by an oscillograph.

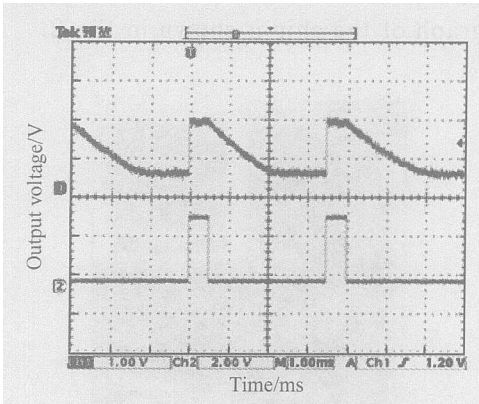

Fig. 4 Qualitative test result

The output voltage at different photo intensities is plotted in Fig. 5. The exposure time is 3ms, and the control circuit is the same as in Fig. 4. The incident light is adjusted by a bulb with variable illumination intensity.

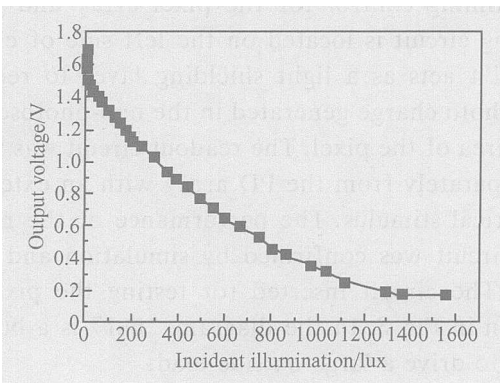

Fig. 5 Output voltage versus incidence density

The main characteristics of the APS are listed in Table 1. The zero digital output in darkroom conditions indicates that the FPN is less than 1 LSB of the 8-bit analog-to-digital converter, which is 3.9mV.

Table 1 Main characteristics of the APS

Technology	0.35μm 2P4M n-well CMOS
Pixel size	8μm × 8μm
Photo detector	n diffusion/p-substrate photodiode
Supply voltage	3.3V
Fill factor	57%
Signal swing	0.17～1.5V(1.33V)
Sensitivity	0.8V/(lux·s)
FPN	<3.9mV(1LSB of 8bit ADC)
Dynamic range	50dB

4 Characteristic analysis and optimization with device scaling considerations

4.1 Fill factor and resolution

The fill factor is the ratio of the photosensitive area to the pixel area. We want to increase the fill factor in order to enhance the sensitivity and dynamic range. First, the pixel capacitance includes a photosensitive part and a parasitic non-photosensitive part, which comes from the floor, the periphery, and the pixel buffer. The output voltage is shown in Eq. (4), where A is the photosensitive area and Q is the photo-generated charge[4,5].

$$V_{out} = Q(A)/[C_{photo}(A) + C_{parasitic}] \quad (4)$$

The photosensitivity can be improved by increasing the photosensitive capacitance. Second, unwanted charges that are non-linearly dependent on pixel area, such as dark current and "reset noise", can decrease the SNR, as shown in Eq. (5). As the fill factor increases, the Q_{noise} level is reduced, and the SNR is improved.

$$SNR = Q_{signal}/Q_{noise} \quad (5)$$

4.2 Photo-charge collection and sensitivity

Carriers generated by photons within the depletion region constitute the drift current that is collected by the PD. Carriers generated by photons in the bulk constitute the diffusion current that is collected by the PD within the diffusion length $L_{diff} = \sqrt{D\tau}$, where D is the diffusion constant and τ is the carrier lifetime. Both the mobility and the carrier lifetime decrease with process scaling due to the increase of the substrate doping. The effective volume for collecting photo charge reduces, leading to a decrease in spectral response sensitivity[1].

Three possible PD structures can be implemented using a p-substrate process: n^+/p-sub, p^+/n-well, and n-well/p-sub[5]. The first two are shallow junctions, and the third is a deep junction. The n^+/p-sub PD used in this design has a simple layout, small pixel area, low FPN due to lithographic variations, and a middle spectral response. The spectral response of the p^+/n-well PD is the worst because of narrowness and shallowness of the junction. Carriers generated outside of the well are shielded, and the n-well takes up much area, so this

structure cannot be used. The n-well/p-sub PD has the best spectral response for visible light due to the width and depth of its depletion region layer, which allows the collection of photo-generated minority carriers deep in the substrate. But the n-well also takes up much area. With a 0.35μm process, the n^+/p-sub may be the best tradeoff between area and spectral response.

The measured sensitivity is 0.8V/(lux ·s), which is lower than the typical value (0.7～3.5V/(lux ·s))[6]. The junction will be much shallower, and the sensitivity will decrease with process scaling. The n-well, on the other hand, will become much smaller, and the n-well/p-sub structure will be the best choice in deep sub-micron processes.

5 Conclusion

A three-transistor active pixel sensor and its double sampling readout circuit are designed. It is embedded in a 64 ×64 pixel array CIS and fabricated. The fill factor is 57 % with an 8μm ×8μm pixel pitch, the sensitivity is 0.8V/(lux ·s), and the dynamic range is 50dB. As processes are being scaled down, high resolution requires smaller pixel area and lower sensitivity with shallower junctions. Circuit size can be scaled down faster than pixel size, and the n-well/p-sub PD structure can be used to enhance sensitivity with an acceptable fill factor in deep submicron processes. Analysis and test results suggest that CIS process will depart from the standard CMOS process in the future. Since the depletion depths become shallower as feature size shrinks, CMOS technologies must be optimized by tailoring the depletion to maintain spectral sensitivity and reduce cross-talk for acceptable cost and performance.

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CMOS 有源像素传感器特性分析与优化设计*

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摘要: 设计了一个三管有源像素和其用开关电容放大器实现的双采样读出电路. 该电路被嵌入一 64 ×64 像素阵列 CMOS 图像传感器, 在 Chartered 公司 0.35μm 工艺线上成功流片. 在 8μm ×8μm 像素尺寸下实现了 57 %的填充因子. 测得可见光响应灵敏度为 0.8V/(lux ·s), 动态范围为 50dB. 理论分析和实验结果表明随着工艺尺寸缩小, 像素尺寸减小会使光响应灵敏度降低. 在深亚微米工艺条件下, 较深的 n 阱/p 衬底结光电二极管可以提供合理的填充因子和光响应灵敏度.

关键词: CMOS 图像传感器; 有源像素; 填充因子; 光响应灵敏度

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