A Passive Low-Pass Filter on Low-Loss Substrate *

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Abstract: The loss mechanisms of different passive devices (on-chip inductors and capacitors) on different substrates are analyzed and compared. OPS (oxidized porous silicon) and HR (high-resistivity) substrates are used as low-loss substrates for on-chip planar LPF (low pass filter) fabrication. For the study of substrate loss, a planar coil inductor is also designed. Simulation results show that Q (the quality factor) of the inductor on both substrates is over 20. Measurements of the LPF on OPS substrate give a -3dB bandwidth of 2.9GHz and a midband insertion loss of 0.87dB at 500MHz. The LPF on HR substrate gives a -3dB bandwidth of 2.3GHz and a midband insertion loss of 0.42dB at 500MHz.

Key words: LC low-pass filter; low-loss substrate; on-chip inductor; RF
EEACC: 2100
CLC number: TN713 **Document code:** A **Article ID:** 0253-4177(2006)09-1572-06

1 Introduction

To meet the needs of modern wireless communication systems, a variety of filters have been developed, such as CMOS active, lumped LC, mechanical, ceramic, surface acoustic wave (SAW), and bulk acoustic wave (BAW) filters. SAW and ceramic filters are mostly used for intermediate-frequency (IF) and radio-frequency (RF) modules, respectively[1]. However, they are all discrete components and consume a considerable area of the system chip and require a specific interface with integrated electronics. That is to say, off-chip components pose an important obstacle to the ultimate miniaturization and portability of wireless transceivers. Therefore, much effort has been focused on miniaturizing and integrating off-chip devices with IC circuits[2].

On-chip LC filters are a candidate for solving the problem[3,4]. However, it is quite difficult to fabricate high-performance on-chip inductors and capacitors with conventional IC processes. Very high substrate loss is one of the main obstacles to realize high Q (quality factor) passive devices[5]. Therefore, low-loss substrate should be developed to achieve high-performance passive filters.

In this paper, planar-integrated LC low-pass filters (LPF) are fabricated on OPS (oxidized porous silicon)[6,7] and high-resistivity (HR) substrates[8], respectively. The filter consists of two inductors and one MIM (metal-insulator-metal) capacitor. The loss mechanisms of passive devices (inductor/capacitor) on different substrates (low/middle/high resistivity substrate) are analyzed, and two kinds of low-loss substrate (OPS/HR substrate) are presented. To evaluate the effect of low-loss substrate, on-chip planar inductors on OPS and HR substrates are used as device examples. Based on the analysis, we present the design and fabrication of the LPF. The measurements show that the Q of RF passive components is improved on both OPS and HR substrates and that the performance of the LPF is promising for RF front-end applications.

2 Substrate loss analysis and comparison

For on-chip RF passive devices, including inductors and capacitors, the main loss mechanisms related to substrate are substrate-eddy-current-induced resistance (R_{eddy}) and coupled capacitive loss

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Received 16 March 2006, revised manuscript received 19 April 2006

(C_{couple}) through the insulating dielectric between the device and the underlying substrate[9].

However, these two factors exert different effects on inductors and capacitors. Figures 1 (a) and (b) give the simplified equivalent lumped circuit models of on-chip inductors[10] and MIM capacitors[11], respectively. In Fig. 1 (a), L_{s_L} is the designed inductance, C_{s_L} models the parasitic capacitance between two metal layers due to the overlapping winding, R_{s_L} is the series resistance of the inductor, including the contribution of R_{eddy} and ohm resistance, R_{si_L} is the substrate resistance, and C_{couple_L} represents the oxide layer capacitance. R_{eddy} is quite important to the performance of on-chip inductors because it is proportional to the square of frequency (f^2) and is the main part of R_{s_L}, which is critical to the Q of the inductor at the frequencies higher than about 1 GHz.

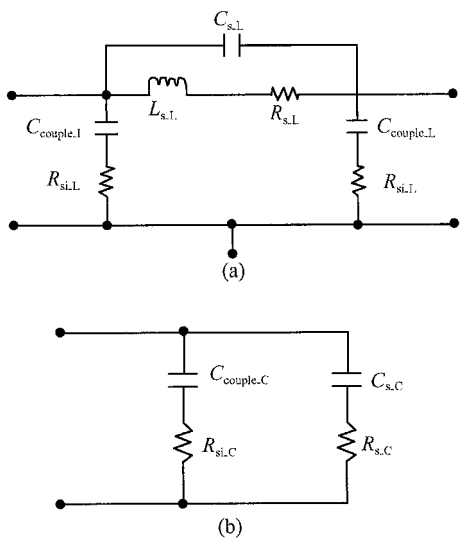

Fig. 1　(a) Simplified two-port equivalent lumped model of on-chip inductors; (b) Simplified one-port equivalent lumped model of MIM capacitors

In Fig. 1 (b), C_{s_C} is the designed capacitance, R_{s_C} is the parasitic series resistance, and R_{si_C} and C_{couple_C} have the same meanings as R_{si_L} and C_{couple_L} in Fig. 1 (a), respectively. C_{couple_C} and R_{si_C} can be regarded as the substrate charging branch, compared with the main branch, consisting of R_{s_C} and C_{s_C}. The main branch has a better Q and less charging time than the substrate branch, for R_{si_C} is always larger than R_{s_C}. At low frequencies (below 1 GHz), both branches can be charged and discharged. Therefore, the Q of the capacitor is mainly determined by that of the substrate branch, which consumes more losses than the main branch. At high frequencies, only the main branch is involved in the charging, and the Q of the device is mainly determined by that of the main branch.

From the analysis of the loss mechanisms of on-chip inductors and MIM capacitors, it is clear that the substrate plays an important role in improving device quality. The possible methods are to partly remove the substrate with wet or dry etching, to enhance the thickness of the isolation layer, or simply to use HR (more than 100 Ω·cm) substrate[12]. To remove the substrate underneath the structure can evidently improve the device performance, but additional complex and expensive processes must be used. Using a thick insulating layer (oxide layer) is also promising for effectively improving the device performance. Nevertheless, it is difficult to get enough thick oxide by common CVD deposition due to the low deposition rate. In contrast, substrate modification with OPS can easily obtain a very thick oxide layer on the order of ten micrometers[7], which decreases the couple capacitance C_{couple}. Using HRS (high resistivity substrate)[8], we can easily obtain good device performance by reducing the substrate-eddy-current-induced resistance and increasing the RC charging time of the substrate branch of the capacitor, which make the influence of substrate branch negligible. Therefore, both substrates used in our study have their own merits.

The Q of inductors and capacitors are directly related to the performance of the LPF. Figure 2 shows simulated curves of the LPF IL (insertion loss) at 500 MHz as it varies with the Q of the inductor and capacitor. $Q(C) = 50$ indicates that Q of the capacitor is fixed at 50 and Q of the inductor is varied from 1 to 40. $Q(L) = 50$ indicates that Q of the inductor is fixed at 50 and Q of the capacitor is varied from 1 to 40. From the two curves, it can be seen that the inductor and capacitor have almost the same effect on the IL of LPF. However, Q of MIM capacitors is always higher than that of on-chip inductors. Therefore, the performance of the inductors is usually the main concern in LC filter design.

To verify the effects of OPS and HR substrate, the same planar spiral inductor is designed and simulated on both of the substrates. Figure 3

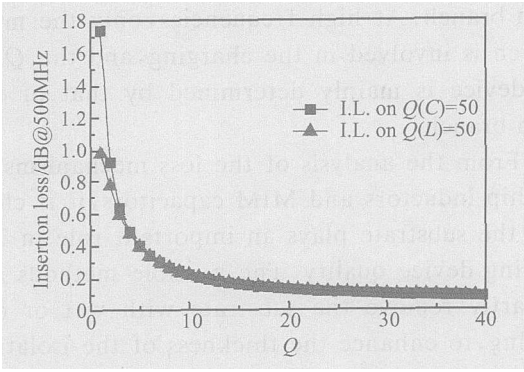

Fig. 2 IL of LPF changes with the quality factor Q of passive devices

shows the 2.5D simulated results of the device. The structure and substrate parameters of the inductor are given in Table 1.

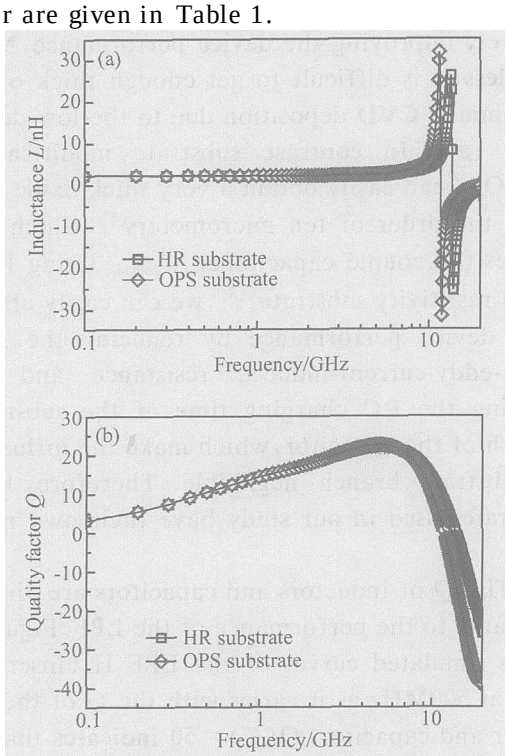

Fig. 3 Simulated (2.5D) results of the planar inductor (a) Inductance of the inductor; (b) Q of the inductor

Table 1 Structure and substrate parameters of inductor

Type	Parameters	Value
Structure parameters	Strip width/μm	36
	Turn-to-turn spacing/μm	12
	Strip thickness/μm	4
	Insulating layer thickness/μm	1.5
	Coil turns	2.5
Substrate parameters	OPS thickness/μm	30
	OPS substrate resistivity/ (Ω·cm)	0.01
	HR substrate resistivity/ (Ω·cm)	900

The measured L and Q of the inductor on HR substrate are 1.8nH at 2.4GHz and 20.0 at 2.4GHz, respectively. These results are similar with the simulated data (L of 2.0nH at 2.4GHz and Q of 18.6 at 2.4GHz), and show that the quality of passive devices is promising on these two kinds of low-loss substrates.

3 Filter design and fabrication

3.1 Design

The design of the LPF is based on a basic minimum capacitor Butterworth prototype structure, which consists of two series inductors and one shunt capacitor, as shown in Fig. 4[13]. Figure 4(a) is the filter circuit and Figure 4(b) gives a 3D schematic view of the LPF. The design parameters are shown in Table 2.

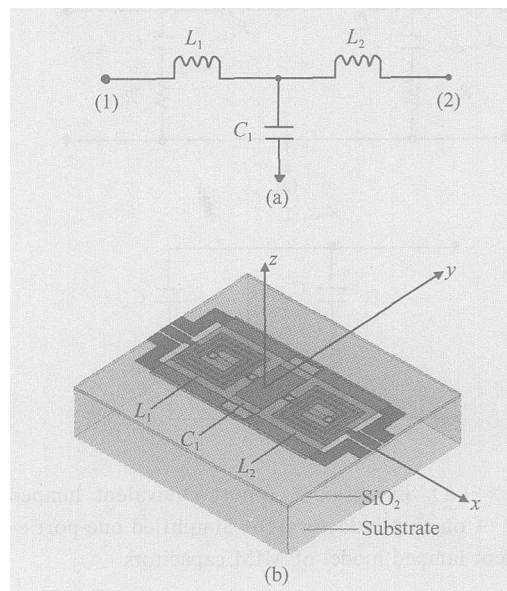

Fig. 4 (a) LC low-pass filter prototype structure; (b) Schematic view of LPF (also for 3D simulation)

Table 2 Design parameters of LPF

	Parameters	Value
Circuit design	3dB bandwidth/ GHz	2.4
	IL (dB @1GHz)	< 2
	Input resistance/Ω	50
	Output resistance/Ω	50
L design	L/ nH	4.2
	Coil turns	3
	Strip width/μm	36
	Turn-to-turn spacing/μm	12
	Strip thickness/μm	4

	Parameters	Value
C design	C/pF	1.8
	Top-plate thickness/μm	4
	Bottom-plate thickness/μm	1
	Insulating layer thickness/μm	1.5
	Width/μm	240
	Length/μm	420

3.2 Fabrication

The fabrication process of the LPF on OPS substrate is given as follows. On the 400μm silicon substrate, a 30μm OPS layer is selectively formed. To protect the OPS layer, SiO_2 and Si_3N_4 layers are deposited with LPCVD. Ti(50nm) and Cu(200nm) are then sputtered as a stick layer and a seed layer. After that, Cu with the thickness of 1μm is electroplated and patterned to form the underpass of the inductors and the bottom plate of the MIM capacitor. Polyimide is spun on as a dielectric layer. After the polyimide etching, another layer of Ti(50nm) and Cu(200nm) is sputtered. Finally, Cu with a thickness of 4μm is electroplated and patterned to serve as the spiral coil of the inductor and the top plate of the MIM capacitor.

The fabrication processes of the LPF on OPS and HR substrate are similar except for the preparation of the substrate. For HR substrate, SiO_2 and Si_3N_4 layers are directly deposited on the substrate without modifying the substrate.

4 Results and discussion

The filter was realized in a standard 1μm 1-poly, 2-metal, CMOS process. Figure 5 shows the profile of the modified substrate with OPS. The surface of the OPS is smooth enough for further processes of RF devices with an average coarseness of less than 2nm. Figure 6 is a SEM photograph of the LPF die. The entire area of the filter is 1350μm ×550μm, which can be further reduced by applying a minimum inductor rather than a minimum capacitor prototype[13]. Figure 7 shows the simulated and measured results of the designed LPF. The data are also compared in Table 3.

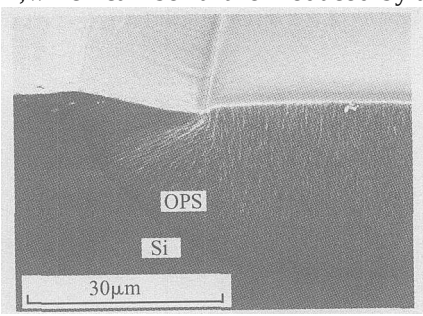

Fig. 5　Profile of modified substrate with OPS

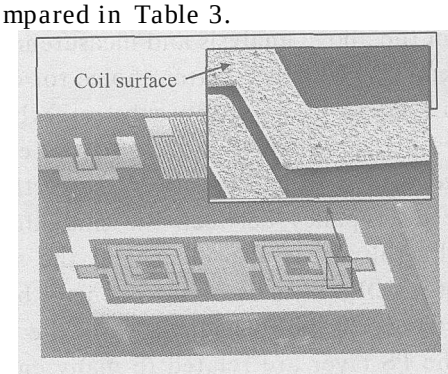

Fig. 6　SEM photograph of the LPF die

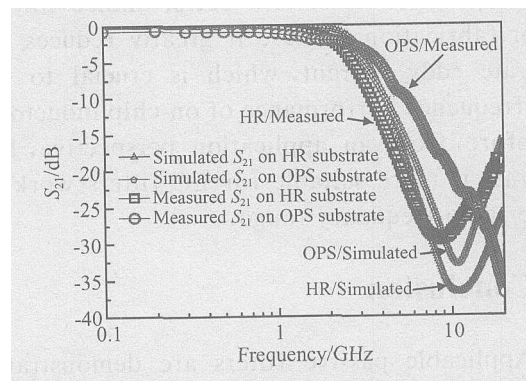

Fig. 7　Simulated and measured results of the designed LPF

Table 3　Simulated and measured data comparison

Parameters	OPS Results		HR Results	
	Simu	Meas	Simu	Meas
3dB BW/GHz	2.6	2.9	3.0	2.3
IL/dB @0.5GHz	0.21	0.87	0.22	0.42
IL/dB @1GHz	0.49	1.18	0.32	0.61
30dB BW/GHz	9.2	17.0	7.8	8.0
Self-resonance frequency f_{SR}/GHz	12.6	>20	11.0	11.4

Measurements of the LPF on OPS substrate give a -3dB bandwidth (BW) of 2.9GHz and a midband insertion loss of 0.87dB at 500MHz, and the LPF on HR substrate gives a -3dB bandwidth of 2.3GHz and a midband insertion loss of 0.42dB at 500MHz. The simulated S_{21} curves are also presented in Fig. 7. The insertion loss of the LPF on OPS and HRS is better than that in Refs. [3] (on 14Ω·cm p-type Si substrate, IL > 2dB at the pass-band) and [14] (on HRS, IL > 6dB at the pass-band). The results are also comparable to Ref. [15] (in MCM-Si Process, IL < 1dB at the pass-band).

The simulated and measured data show that both OPS and HR substrates are promising for RF passive devices, such as inductors, capacitors, and LC filters.

From the above analysis and measurements, it can be seen that OPS is a better choice for capacitors than HRS (high resistivity substrate), because it reduces C_{couple}, which is critical to the coupled capacitive loss of the capacitors. Nevertheless, from the discrepancy between the simulated and measured results, it is also clear that the surface quality of an OPS layer is hard to control because the growth of PS (porous silicon) and the oxidation of the PS layer are related to many environmental parameters[7,16,17], including current, area, and temperature. HRS is a better choice for inductor fabrication because it greatly reduces the substrate eddy current, which is crucial to the high-frequency performance of on-chip inductors. Therefore, from an application perspective, HR substrate is more suitable for LC filters working in the radio-frequency range.

5 Conclusion

Applicable passive filters are demonstrated and fabricated. Both HR and modified substrates with oxidized porous silicon (OPS) technology can reduce the insertion loss of passive RF devices, making LC filters suitable for high frequency applications. HR substrate is more suitable for LC filters in RF applications.

Acknowledgment The authors would like to thank IMECAS for microwave measurement and EM Laboratory for SEM.

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低损耗衬底上实现无源低通滤波器*

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摘要：分析比较了不同种类衬底上无源器件(片上电感和电容)的损耗机理,在 OPS(氧化多孔硅)和 HR(高阻硅)低损耗衬底上分别实现了片上低通滤波器.为了研究衬底损耗,设计了平面螺旋电感,其 Q 值在两种衬底上的仿真结果都超过了 20.在 OPS 衬底上的低通滤波器实测 - 3dB 带宽为 2.9GHz,通带插入损耗在 500MHz 为 0.87dB;在 HR 衬底上的低通滤波器实测 - 3dB 带宽为 2.3GHz,通带插入损耗在 500MHz 为 0.42dB.

关键词：LC 低通滤波器；低损耗衬底；片上电感；RF
EEACC：2100
中图分类号：TN713　　**文献标识码**：A　　**文章编号**：0253-4177(2006)09-1572-06

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2006-03-16 收到,2006-04-19 定稿