A Highly Linear Filter and VGA with DC-Offset Correction for GSM/WCDMA Receivers

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Abstract: This paper describes a complete baseband chain for both GSM and WCDMA receivers with a SMIC 0.35μm mixed signal process. The chain consists of a dual-mode, highly linear, fourth order Chebyshev active RC filter and three VGA stages. The filter is designed to meet the bandwidth specifications of the GSM and WCDMA standards and share the maximum number of components between the two modes to reduce manufacturing cost. The design is free of DC-offset and has an inter-stage high-pass filter, and operational amplifiers with adjustable GBW are used to minimize GSM-mode power consumption. The measured noise figures are 27.3 and 42dBm in WCDMA and GSM modes, respectively, at the maximum gain. The IIP_3 is 40dBm at unit gain in the WCDMA mode, and the circuit consumes 47.0mW. The IIP_3 is 28dBm in the GSM mode, and the circuit consumes 31.8mW. The supply voltage is 3.3V.

Key words: active RC filter; VGA; Tow-Thomas; DC-offset correction; dual-mode
EEACC: 1220
CLC number: TN431 **Document code**: A **Article ID**: 0253-4177(2007)03-0372-05

1 Introduction

A system that allows for both WCDMA in wideband systems and GSM in narrow-band systems is the developing trend for mobile phones[1]. However, a large increase in either the total manufacturing cost or the power consumption is not acceptable. Therefore, all the circuitry must be shared as much as possible by different modes[2]. This requires a high-order channel-select low-pass filter (LPF) so that the cut-off frequency can be switched from GSM to WCDMA, and a variable gain amplifier (VGA) that can provide more than 60dB of gain variation. For high linearity applications, active RC filters and the op-amp-based VGAs are good options. The cutoff frequency is switched by both resistors and capacitance matrices. While the power dissipation mainly depends on the op-amp used in the baseband chain, the GBW is made adjustable to minimize the power dissipation in different modes. This paper describes the design and implementation of a highly linear filter/VGA with built-in DC-offset correction circuit.

2 Circuit implementation

In the baseband chain architecture, the filter is inserted after the first gain stage of the VGA (Fig. 1). This arrangement of the baseband chain reduces the input referred noise of the filter at high gain settings while keeping the linearity of the whole chain at reasonable values[3]. Each gain stage provides 21dB of variable gain in 3dB step.

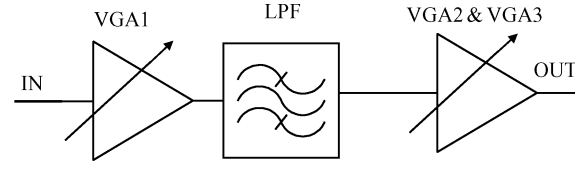

Fig. 1 Baseband chain

2.1 Filter description

A dual-mode baseband filter for WCDMA and GSM systems was implemented. The scalar differences of channel bandwidth between these systems made combining them difficult. In WCDMA mode, the channel bandwidth is 2.1MHz; while in GSM mode, the channel is 200kHz. The

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Received 5 June 2006, revised manuscript received 30 October 2006

wide bandwidth in WCDMA mode leads to high power consumption easily. In contrast, the low corner frequency of the GSM leads to large passive components occupying larger die area[2,4].

In this design, a Tow-Thomas state variable biquad is used which is based on the full feedback loop with the advantages of low output impedance and high input impedance. The two-stage cascaded filter is shown in Fig. 2, in which fully differential op-amps are used as the active elements.

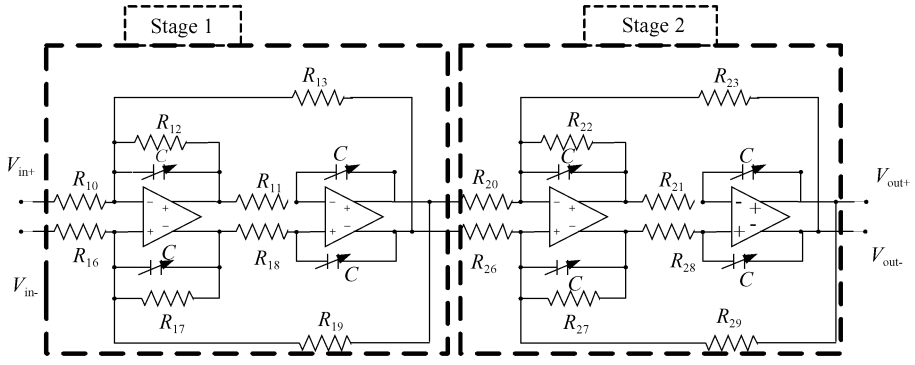

Fig. 2　Two-stage cascaded filter

The major source of noise in this filter is thermal noise. The Friss equation is

$$\mathrm{NF_{tot}} = 1 + (\mathrm{NF_1} - 1) + \frac{\mathrm{NF_2} - 1}{A_{\mathrm{p1}}} + \cdots + \frac{\mathrm{NF}_m - 1}{A_{\mathrm{p1}} \cdots A_{\mathrm{p}(m-1)}} \tag{1}$$

where NF_i is the noise figure of stage i, and $A_{\mathrm{p}i}$ is the DC gain of stage i. If the first stage exhibits amplification, the noise figure of the following circuit is attenuated as a result of reduction in the whole system. However, for m stages, we have

$$\frac{1}{\mathrm{IIP}^2_{3,\mathrm{total}}} \approx \frac{1}{\mathrm{IIP}^2_{3,1}} + \frac{A^2_{\mathrm{p1}}}{\mathrm{IIP}^2_{3,2}} + \frac{A^2_{\mathrm{p1}} A^2_{\mathrm{p2}}}{\mathrm{IIP}^2_{3,3}} + \cdots \tag{2}$$

where $\mathrm{IIP}_{3,i}$ denotes the input IIP_3 of stage i. Thus, if the first stage has a gain greater than unity, the nonlinearity of the latter stages becomes increasingly critical because the IIP_3 of each stage is scaled down by the gain of the first stage[7].

In this design, the first stage is a low-Q filtering stage, which has to provide sufficient gain and reject interference while having a reasonable noise performance. The main challenge is to get the linearity of the filter as high as possible with a limitation of noise.

2.2　VGA structure

For the requirement of high linearity, the structures of the three VGAs are all the same which are also based on active RC, as shown in Fig. 3. The gain variation is switched by resistors. In this design, there are no extra switches in the signal path that may greatly affect the linearity.

In this design, DC cancellation is implemented with an inter-stage HPF in the feed-forward path[3], as shown in Fig. 3. The transfer function of the VGA with HPF is

$$V_{\mathrm{out}} = -\frac{R_{\mathrm{f}}}{R_{\mathrm{in}}} \times \frac{1}{1 - \dfrac{R_{\mathrm{f}}}{R_1 R_2 SC}} V_{\mathrm{in}} \tag{3}$$

where R_{f} is the feedback resistance, R_{in} is the input resistance of the main op-amp, R_1 is the input resistance for the high-pass filter, R_2 is the feedback resistance from HPF to the main op-amp in the VGA, and C represents the capacitor in the HPF. The cutoff frequency of the HPF is $\omega = R_{\mathrm{f}}/R_1 R_2 C$, which is often designed as less than one-fifth of the input signal frequency.

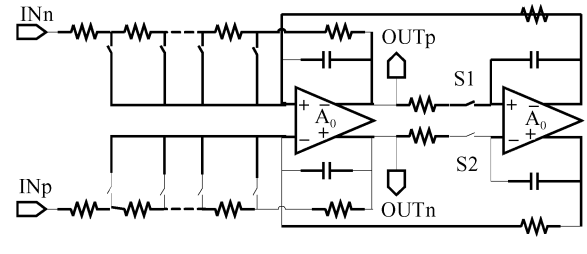

Fig. 3　Circuitry of VGA

To accelerate the response speed of the HPF, a control switch S1 (S2) is applied before the input of the HPF. When the main op-amp is at work, the switch remains on; when the main op-amp is off, the switch is also off. Then the correc-

tion voltage of the DC offset is kept in the capacitors of the HPF. Next time the switch is on again, and the DC offset cancellation can be done with the prefilled correction voltage. This skips the process of charging the capacitors in the HPF to improve the response speed.

2.3 Op-amp design

The block diagram of the fully differential two-stage op-amp is shown in Fig. 4. The op-amp is Miller-compensated with RHP zero nulling resistors[6]. The resistors are realized with nMOS transistors biased in the linear region to track the output stage g_m. To eliminate the effect of the op-amp on the filter as much as possible, a tried-and-true method is used following the equation

$$\mathrm{GBWP} \geqslant 10Qf_c \tag{4}$$

where Q is the polarity of the filter[9]. From this equation, the difference between cutoff frequencies of the filter was further amplified, making the bandwidths of the op-amp more rigorous. Instead of using completely different amplifiers, the GBW of the amplifiers was made programmable. First, the op-amp was designed for the larger bandwidth of WCDMA. In the GSM mode, the bandwidth can be reduced through decreasing the bias current. This is done by changing the width of the current source transistors feeding the input and output stages with the control switches as Ctr_Vbn (Fig. 4). In this way, there are no extra switches in the signal path, and the gate-source voltage of the current sources remains constant. This is important to minimize offset problems and to make bias currents close to their anticipated values.

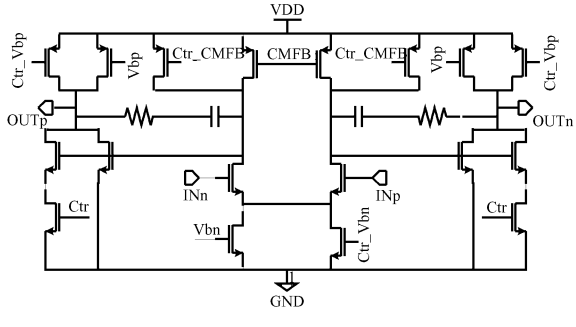

Fig. 4 Simplified schematic of the operational amplifier

A similar method is also used in the design of the op-amp used in the VGA stages.

2.4 Passives

Due to variations in processing and temperature, the actual resistance and capacitance values of the integrated components may differ significantly from the nominal value. In order to compensate for component variations, either resistances or capacitances can be made tunable[2,4]. In this work, the corner frequency in the filter was tuned by the 8-bit tuning capacitor matrices.

As the capacitor matrices occupy large area, they are shared by both modes. The switches were used to control whether the capacitors were connected to the circuit. When a tunable capacitor matrix is chosen to be shared, the resistance value can be reduced by using only part of the bit-weighted capacitors as shared components (Fig. 5). Consequently, the extension in resistor values is given by[2,4]

$$\frac{R_{\mathrm{GSM}}}{R_{\mathrm{WCDMA}}} = \frac{1}{2^{\mathrm{Nol}}} \times \frac{f_{\mathrm{C,WCDMA}}}{f_{\mathrm{C,GSM}}} \tag{5}$$

According to the above analysis, the designed figure of the capacitors in GSM is 10pF, while the one in WCDMA mode is 5pF. The tuning range is nearly 27.5%, and the tuning solution is 50μF. The resistances are composed of unit resistors to get a lower comparative offset.

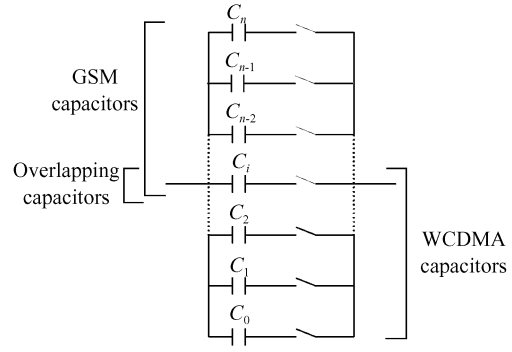

Fig. 5 Capacitor matrix

3 Experimental results

Figure 6 shows a microphotograph of the die with the total area of 1.155mm^2. The filter/VGA chain was implemented in a SMIC 0.35μm CMOS process. All differential resistor and capacitor matrix pairs were designed to be mirror symmetric. Furthermore, the two channels were also designed to be mirror symmetric. Long paths were drawn as guarded differential pairs to reduce capacitive coupling.

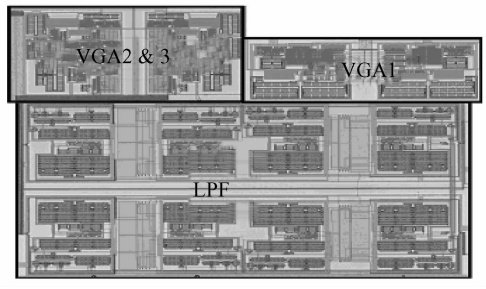

Fig. 6　Die micrograph

Figures 7 and 8 show the frequency response of the filter for different modes at room temperature. Changing the code of the capacitor matrix in GSM mode, another amplitude response was obtained (Fig. 9). Thus the filter is easily tuned accurately to the selected cutoff frequency.

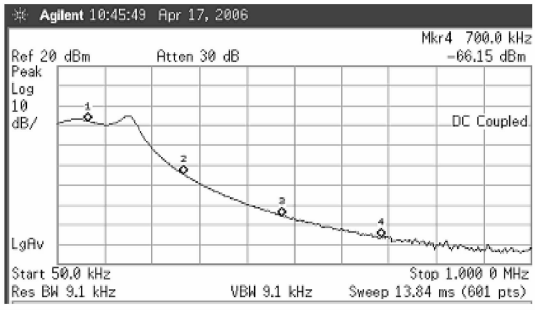

Fig. 7　Frequency response in GSM mode

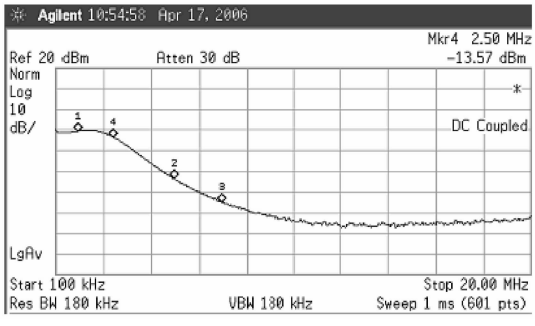

Fig. 8　Frequency response in WCDMA mode

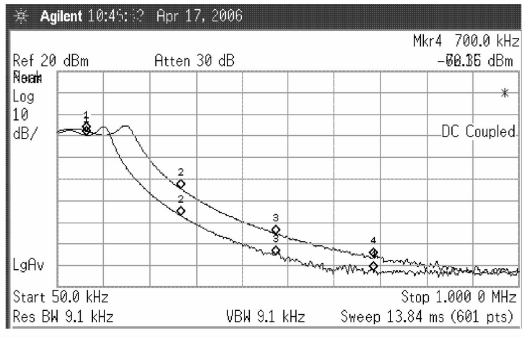

Fig. 9　Amplitude response with different codes in GSM mode

The maximum gain of the whole chain including the filter is 63dB. Figure 10 shows the response of the VGA2 and VGA3 for different gains in GSM mode. However, the high-pass filter inserted between the LPF and VGA cannot be detected at low cutoff frequencies. The third-order intermodulation distortion was measured at unit gain. In WCDMA mode, the IIP_3 was found to be 40dBm, and in GSM mode, the distortion is too small to be reliably measured, with a value of 28.6dBm. Figures 11 and 12 show the baseband chain output spectra in WCDMA and GSM modes at the same measurement point, respectively. Table 1 shows a comparison between this design and other reported work.

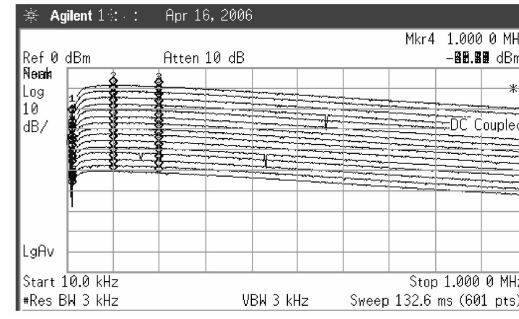

Fig. 10　Frequency response of the VGA2 and VGA3 (different gains)

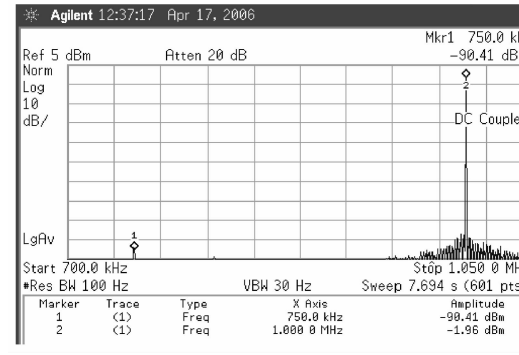

Fig. 11　Spectrum of IIP3 measurement in output of WCDMA mode

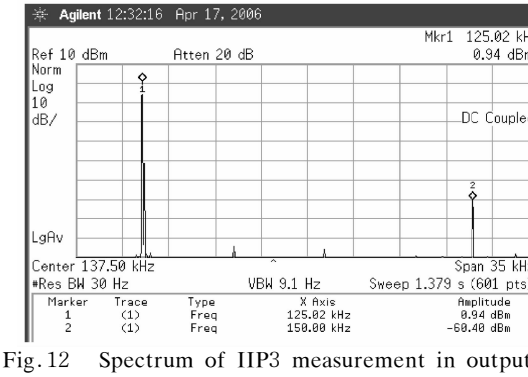

Fig. 12　Spectrum of IIP3 measurement in output of GSM mode

Table 1 Comparison with other reported works

Supply /V	Pwr cons. I + Q /mW	Cut off freq	Max gain /dB	IIP_3 /dBm	Noise, input ref /($\mu V/\sqrt{Hz}$)	Technology	Reference
2.7	25.4 (Filter)	2.1MHz	30	30	47	0.35μm CMOS	Ref. [2]
2.7	6.8 (Filter)	13kHz	30	–	17	0.35μm CMOS	Ref. [2]
1.4	27	–	67.5	2	0.019	90nm CMOS	Ref. [3]
3.3	31.8	200kHz	63	28	15.4	0.35μm CMOS	This work
3.3	47	2.1MHz	63	40	0.021	0.35μm CMOS	This work

4 Conclusion

This paper described the architecture and circuit of a baseband filter and VGA for GSM and WCDMA receivers. To meet the different bandwidths, the bandwidths of the operational amplifiers were made tunable and resistors as well as capacitors were shared in both modes. For DC offset cancellation, an HPF was inserted before both VGA stages. To get high linearity, all designs were based on active op-amp RC.

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一种适用于 GSM/WCDMA 的高线性度滤波器及带有消除直流偏置的可变增益放大器

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摘要： 采用 SMIC 0.35μm CMOS 混合信号工艺，实现了同时适用于 GSM/WCDMA 的完整的基带. 基带由双模的高线性度的四阶切比雪夫形式的有源 RC 低通滤波器以及三级可变增益放大器构成. 滤波器的设计同时满足 GSM 和 WCDMA 的带宽性能并且为降低制造成本在两种模式下具有最大的元件共享度. 基带由于插入了高通滤波器具有滤除直流的功能，并且为了优化 GSM 模式下的功耗，运放的带宽做成可调. 在最大增益情况下测得的噪声系数在 GSM 和 WCDMA 模式下分别为 42 和 27.3dBm. 在单位增益的情况下，WCDMA 模式下的 IIP_3 为 40dBm，功耗为 47.0mW；在 GSM 模式下，IIP_3 为 28dBm，功耗为 31.8mW. 电源电压为 3.3V.

关键词： 有源 RC 滤波器；可变增益放大器；Tow-Thomas；消除直流偏置；双模

EEACC： 1220

中图分类号： TN431 **文献标识码：** A **文章编号：** 0253-4177(2007)03-0372-05

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2006-06-05 收到，2006-10-30 定稿