Integrated Delta-Sigma 1.5bit Power DAC with 100dB Dynamic Range

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Abstract: A stereo 1.5bit delta-sigma digital-analog converter (ΔΣ DAC) integrated with a filterless class D power amplifier is introduced. It consumes no static power, and its maximum output power is 436mW with an 8Ω load. Its output dynamic range exceeds 100dB. The circuit is implemented with a TSMC 0.18μm process. The die area is 0.28mm². The supply voltage is 1.8V for the digital part and 3.3V for class D.

Key words: delta-sigma DAC; filterless class D power amplifier; interpolator; power DAC

1 Introduction

The past five years have been a golden time for the development of consumer electronic products. According to the prediction of the Internet Data Corporation (IDC), the multimedia market, including MP3 players, PDAs, DV cameras, and portable phones, will increase by at least 230% from 2004 to 2007. Therefore, the design of audio DACs, which are necessary components of these multimedia products, is also attracting much attention.

The delta-sigma DAC is the most popular structure for audio signal processing. A typical ΔΣ DAC consists of a digital interpolator, a digital ΔΣ-modulator (DSM), a 1bit DAC, and an analog signal reconstruction filter[1]. Since multimedia products require portability and low power-consumption, today’s audio DACs are often integrated with linear power amplifiers (PA) to drive a load such as a speaker directly[2].

The majority of the silicon area of DACs is occupied by digital circuitry whose area and power consumption are dropping dramatically with the development of technology scaling. The analog part, including a reconstruction filter and a PA, then becomes the bottle-neck for further improving DAC technology. In the new generation of CMOS processes, it is becoming more and more expensive to implement linear capacitors in the SC reconstruction filter. Moreover, the filter and linear PA introduce harmonic distortion and consume much power.

In this paper, a delta-sigma power DAC with filterless class D power amplifier is introduced. The proposed power DAC removes the reconstruction filter and replaces the linear PA with a filterless bridge-tied-load (BTL) differential-drive class D amplifier whose power efficiency is much higher. Its 3-level (1.5bit) output can reduce the circuit’s current consumption further. The proposed DAC can be conveniently applied as macro blocks in audio codecs and can more easily undergo a process migration following the fast evolution of the digital processes than can traditional structures. The supply voltage is 1.8V for the digital circuitry and 3.3V for the class D amplifier. The maximum output power is 436mW, and the measured dynamic range exceeds 100dB.

2 Architecture of the 1.5bit DS power DAC

Figure 1 shows the signal flow diagram of the 1.5bit DS power DAC. The 16bit digital input is first interpolated 64 times and then applied to the digital 4th-order 1.5bit DSM. The output of the modulator is converted to three voltage levels and drives headphones or speakers through a BTL class D amplifier. Since the DAC is used for audio codecs and people’s ears can only perceive signals
between 20Hz and 20kHz, no filters are needed to remove the noise beyond 20kHz. The power supply for the class D amplifier is 3.3V, while the digital circuit operates at 1.8V to reduce the digital power consumption and switching noise.

![Diagram](https://via.placeholder.com/150)

Fig. 1  Signal flow diagram of the 1.5bit ΔΣ power DAC

### 2.1 Interpolator design

A high over-sampling rate (OSR) can depress the in-band quantization noise and reduce the order needed for the ΔΣ modulator. Thus an interpolator is used here to enhance the OSR and filter the image. The order of the interpolator increases with the sample frequency and the width of the filter’s transition band. To reduce the order of the interpolator, a cascade structure is used with two FIR half-band interpolation filters and one band-pass interpolation filter (as shown in Fig. 1). The half-band filters increase the OSR of the input digital signal by 2 times, and the band-pass filter increases the OSR by 16 times. Since the transition bandwidth of the first filter is the narrowest, its order is the highest. To reduce the circuit cost, this filter is designed as one prototype filter with several sub-filters. The structures and coefficients of the sub-filters are completely identical. As expressed in Eqs. (1) and (2), if the prototype filters consist of 2m - 1 sub-filters whose order is 2n - 1, the order of the prototype filter \( F_{\text{prot}} \) is \( (2m - 1)(2n - 1) + 1 \):

\[
F_{\text{sub}}(z) = z^{-m} \sum_{k=0}^{m-1} f_k (m - k)(z^{-m-k} + z^{-m+k})
\]

\[
F_{\text{prot}}(z) = z^{-(2n-1)(2m-1)} + 2 \sum_{i=0}^{n-1} \{ f_i (n - i) \times \left[ F_{\text{sub}}(z^{-2}) \right]^{2i+1} (z^{-2})^{(2m-1)(n-i-1)} \}
\]

Then only one sub-filter needs to be realized with hardware, which can be reused 2n - 1 times to implement the high order prototype filter.

### 2.2 Design of the 1.5bit ΔΣ modulator

The structure of the 4th digital ΔΣ modulator is shown in Fig. 2. It shapes the quantization noise to a higher frequency band and then satisfies the required in-band SNR. To drive a low resistive load such as speakers or headphones, the output power of the modulator must be amplified. For a traditional linear PA, the quantization noise at high frequency must be filtered by the reconstruction filter in advance, and the order of the filter must be higher than that of the delta-sigma modulator. Such a high order filter occupies a large area, consumes great power, and introduces some distortion as well.

![Diagram](https://via.placeholder.com/150)

Fig. 2  1.5bit 4th ΔΣ modulator

To solve these problems, a 1.5bit ΔΣ modulator is proposed in this paper. Its output is a 3-level code (“00”, “10”, and “01”) that is applied directly as the input of a class D amplifier. Since this power DAC is applied for audio codecs, the person’s ear is an initial low pass filter (pass band is 20Hz~20kHz), so no post-filter is needed for the class D power amplifier. Compared with the traditional structure, the 1.5bit structure can achieve better SNR and equally good linearity. Moreover, the efficiency of the 1.5bit filter-less class D amplifier is also higher than that of a 1-bit one. As shown in Fig. 3, the differential output varies between positive and negative power supply for a 1bit class D amplifier because its load is low resistance. Then the current through the load is always high, which causes high power loss.

![Diagram](https://via.placeholder.com/150)

Fig. 3  Class D amplifier output voltage across load
For a 1.5bit class D amplifier, the voltage across the load is set at 0 during most of the working time when the output of the modulator is “00”. This greatly reduces both the $I^2R$ loss in the load and the switching power loss.

2.3 Class D amplifier

The class-D output stage not only provides large driving to the load but also acts as a 1.5bit DAC. It is critical to ensure that the signals in each branch of the differential path have equal rise and fall times. Then the layout of the output stage transistor should be designed to be as compact and symmetric as possible. Compared with conventional finger transistors, the bent-gate transistor as shown in Fig. 4 can increase the gate width while simultaneously allowing the gate strips to be packed more closely. The use of 135° bends is less prone to localized avalanche than 90° bends and can improve robustness under extreme conditions, such as those encountered during ESD testing. Moreover, it simplifies metallization and backgate contact distribution. The source and substrate of the transistor can be very close. Then this layout pattern is insusceptible to backgate debiasing and latchup.

3 Measured results

The chip micrograph of the integrated stereo delta-sigma power DAC is shown in Fig. 5. The chip is implemented with a TSMC 0.18μm CMOS process. The power supply is 1.8V for digital circuits and 3.3V for the class D amplifier. The scale of the digital circuit is 47,000 gates and the die area for the two-channel class D amplifier is 0.28mm². The maximum output power of the useful audio signal is 436mW with an 8Ω load. The chip was measured with an ATS-2 audio test system. As shown in Fig. 6, the floor noise is about $-100$dBV ($7.75\mu V$) and the output dynamic range exceeds 100dB. The total harmonic distortion (THD) is less than 0.02% and the THD + N (in-band noise) is less than $-72$dB. The detailed measured results are listed in Table 1.
greatly reduces the $I^2R$ losses in the load and the switching power loss. The tested output dynamic range of the power DAC exceeds 100dB.

References


