Study on Si-SiGe Three-Dimensional CMOS Integrated Circuits*

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Abstract: Based on the physical characteristics of SiGe material, a new three-dimensional (3D) CMOS IC structure is proposed, in which the first device layer is made of Si material for nMOS devices and the second device layer is made of Si_xGe_{1-x} material for pMOS. The intrinsic performance of ICs with the new structure is then limited by Si nMOS. The electrical characteristics of a Si-SiGe 3D CMOS device and inverter are all simulated and analyzed by MEDICI. The simulation results indicate that the Si-SiGe 3D CMOS ICs are faster than the Si-Si 3D CMOS ICs. The delay time of the 3D Si-SiGe CMOS inverter is 2～3ps, which is shorter than that of the 3D Si-Si CMOS inverter.

Key words: Si-SiGe; three-dimensional; CMOS; integrated circuits
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1 Introduction

With the dramatic developments in semiconductor technology and circuit design, more sophisticated systems have been implemented on a single chip. Some insurmountable problems have appeared in fabricating higher speed and performance planar chips with decreased device area and shortened interconnects. For example, the smaller chip size results in a more distinct quantum effect, and higher chip integration causes more problems coming from the increased self-heating and heat-dissipation[1～3]. Furthermore, interconnect delay becomes more considerable in the whole circuit's delay time with decreasing device area[4]. Adopting three-dimensional (3D) integrated circuits (ICs) could significantly shorten the length of interconnects by interconnecting in the vertical direction, thus improving the speed performance of ICs.

The idea of stacking transistors on top of others to form a three-dimensional integrated circuit is not a new concept, but up to now, 3D stacking techniques have just been used to realize high-density memory modules. This is mainly due to the complexity of fabricating the 3D circuits as well as the poor performance of the transistors made on the upper-layer of non-single-crystal silicon films.

At present, the study of 3D CMOS integration technology mainly focuses on: (1) "tri-gate" 3D CMOS integration technology[5]; (2) "recrystallization" 3D CMOS integration technology[6]; (3) "metal-induced lateral crystallization (MILC)" 3D CMOS integration technology[7]; (4) "selective epitaxial lateral overgrowth (SELO)" 3D CMOS integration technology[8]; (5) "wafer-bonding" 3D CMOS integration technology[9]. All of these technologies hold common ground: first, the structure of 3D integration studied only consists of two layers; second, the first device layer is made from single crystalloid Si material, from which the nMOS device is fabricated, and the second device layer is made from single crystalloid Si material or large grain size poly-silicon, from which the pMOS device is fabricated. Then the intrinsic performances of the CMOS is limited by pMOS, fabricated using the single crystalloid Si material or large grain size poly-silicon, because the hole mobility of single crystalloid Si material or polycrystalline Si material is lower than the electron mobility, which limits the performance of the circuits. A novel Si-SiGe 3D CMOS structure is put

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forward in this paper, the first device layer of which is made from single crystalloid Si material that is made into nMOS and the second device layer of which is made from strained Si_xGe_{1-x} material that is made into pMOS. In this way, the performances of the 3D integrated circuits with Si-SiGe CMOS structure depend on nMOS.

2 Theories of Si-SiGe 3D CMOS structure

The I_D-V_{DS} characteristics of Si nMOS and SiGe pMOS with differential gate oxidation thicknesses are simulated and compared using MEDICI, in order to indicate that the intrinsic performance of the Si-SiGe 3D CMOS circuits is limited by the electron mobility, which is determined by nMOS. The simulation results are shown in Fig. 1 and Fig. 2, which indicate that the drain current I_D of Si nMOS (with channel lengths of 0.5μm, oxide thickness of 10nm, and doping concentration of $1\times10^{16}cm^{-3}$ in the substrate) is about 200 $\mu A/\mu m$ for a gate voltage of 2V, and the drain current I_D of SiGe pMOS (with channel lengths of 0.5μm, oxide thickness of 10nm, and Ge content of 0.25) achieves 280$\mu A/\mu m$ at the same gate voltage. The drain current I_D of SiGe pMOS is larger with the Ge content becoming high. This could indicate that the electrical performance of Si-SiGe 3D CMOS circuits will be limited by the electron mobility in Si nMOS.

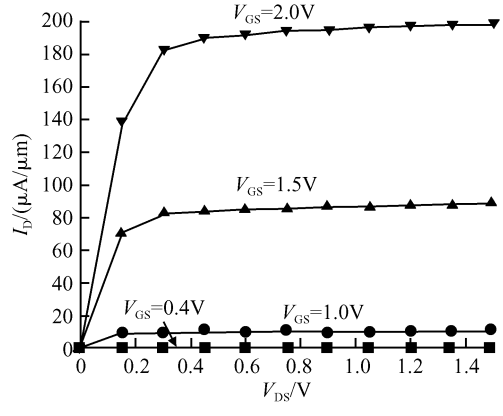

Fig. 1 Si nMOS I-V characteristics

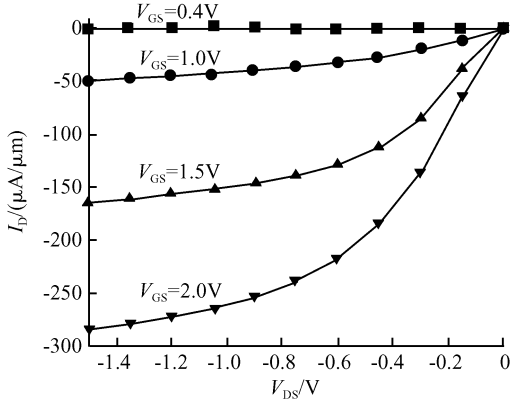

Fig. 2 SiGe pMOS I-V characteristics

3 Si-SiGe 3D CMOS structure

A schematic of the Si-SiGe 3D CMOS structure is shown in Fig. 3. The first layer for the Si nMOS device is fabricated using the traditional technology, and the second layer for SiGe pMOS devices is fabricated with strained SiGe material using the wafer-bonding technique, which is SGOI (SiGe on insulator) pMOS. The structure is based on three key issues: first, each device layer is well insulated from the others; second, the crystal performance of each device layer is perfect; and third, the fabrication temperature for the second layer device is lower in order to make sure that the performance of the first layer device will not be effected. The SiGe material is grown, and the SiGe pMOS is fabricated, after two device layers are bonded at low temperature (<700℃). The fabrication temperature of the SiGe pMOS is usually below 600~700℃, which has little influence on the first layer device, so the best choice is the SiGe pMOS for the second layer device. The material of the two layers is formed by low temperature wafer-bonding, and then the SiGe material and devices are completed.

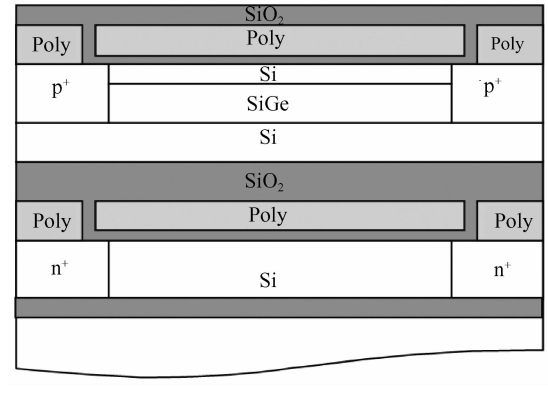

Fig. 3 Schematic of Si-SiGe 3D CMOS structure

4　Si-SiGe 3D CMOS simulation

The simulation results of Si nMOS and SiGe pMOS are shown in Fig. 4 after the structure and physical parameters of Si-SiGe 3D CMOS have been adjusted. In the SiGe pMOS, the thickness of SiGe layer is 15nm, with Ge content of 0.25, and the thickness of the cap layer is 3nm. In the Si nMOS, the doping concentration is $1\times10^{16}\,cm^{-3}$ in the substrate. It can be seen from Fig. 4 that the threshold voltage of the Si nMOS is 0.4V, and the saturation drain current is about $280\mu A/\mu m$ with the gate voltage being 2V; the threshold voltage of the SiGe pMOS is −0.4V, and the saturation drain current is about $320\mu A/\mu m$ with a gate voltage of −2V, and the drain current of the SiGe pMOS might achieve $340\mu A/\mu m$ with a Ge content of 0.36. Here, the characteristic of the SiGe pMOS is better than that of the Si nMOS. Thus the performance of Si-SiGe 3D CMOS is limited by the Si nMOS.

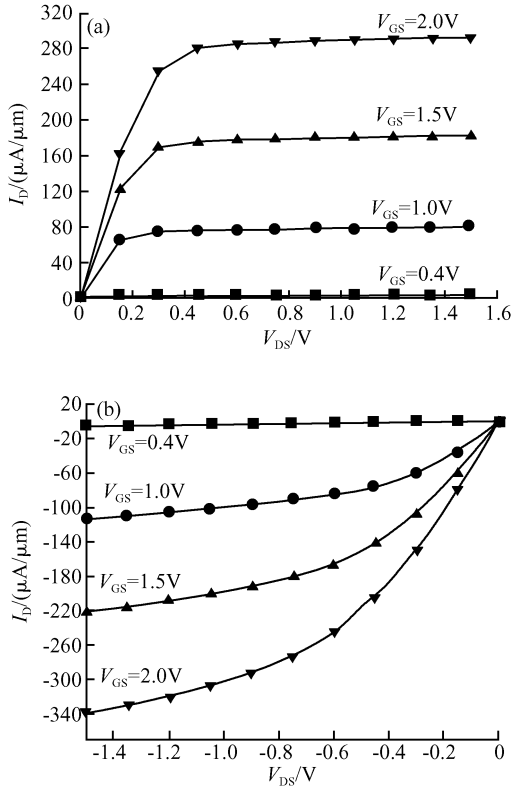

Fig. 4　*I-V* characteristics of Si nMOS (a) and SiGe pMOS (b) in Si-SiGe 3D CMOS structure

The trans-conductance of Si nMOS and SiGe pMOS was simulated and compared respectively, and the results are shown in Fig. 5. The trans-conductance of the Si nMOS is $220\sim230\mu S/\mu m$, but the trans-conductance of the SiGe pMOS is $310\mu S/\mu m$, which is higher than that of the Si nMOS.

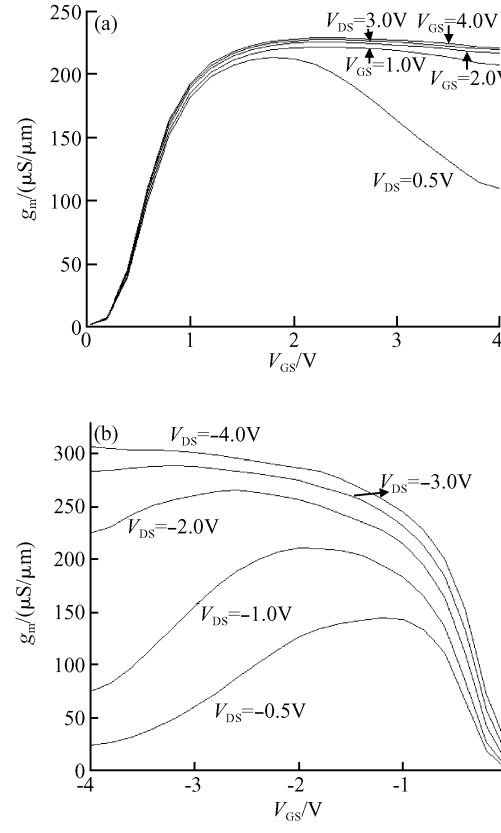

Fig. 5　g_m characteristics of Si nMOS (a) and SiGe pMOS (b) in Si-SiGe 3D CMOS structure

5　Si-SiGe 3D CMOS inverter simulation

The input-output characteristics of a Si-Si 3D CMOS inverter and a Si-SiGe 3D CMOS inverter were simulated respectively, with the result that the Si-SiGe 3D CMOS structure performance is superior to that of the Si-Si 3D CMOS structure. The input signal for both structures was a square wave signal with 200ps period and 5.0ps rise time, as shown in Fig. 6.

The output simulation result of the Si-Si 3D CMOS inverter is shown in Fig. 7, and the delay time is 6ps. It's reported that a Si-Si 3D CMOS inverter with a delay time of 11.8ps[9] has been fabricated by IBM using the wafer-bonding tech-

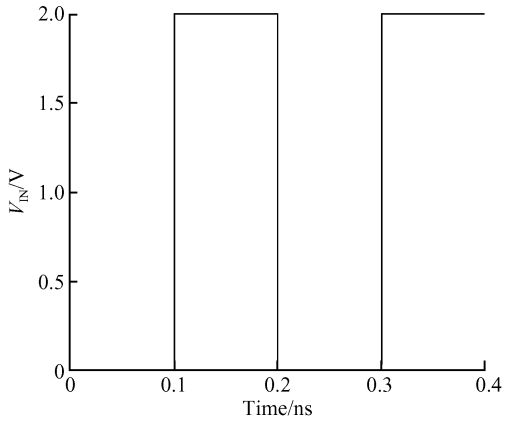

Fig. 6 Input wave of inverter

nique. A delay time of 8.6ps of a Si-Si 3D CMOS inverter[7] was reported by Hong Kong University of Science and Technology.

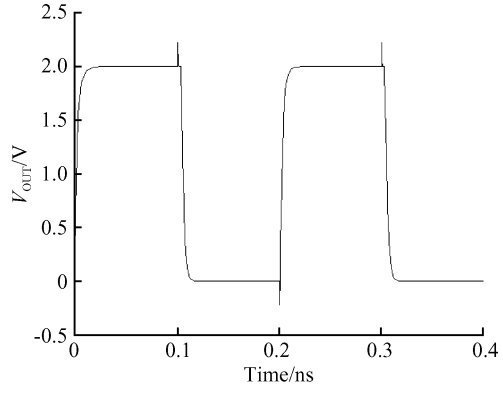

Fig. 7 Output wave of Si 3D CMOS inverter

The output simulation result of the Si-SiGe 3D CMOS inverter is shown in Fig. 8, and the delay time is about 2～3ps, which is less than the delay time of 6ps of the Si-Si 3D CMOS inverter. These results indicate that the Si-SiGe 3D CMOS

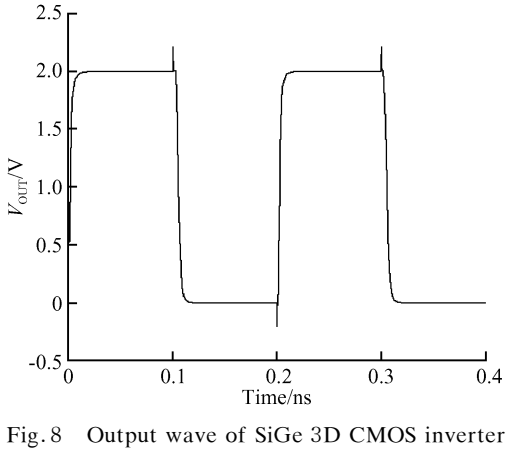

Fig. 8 Output wave of SiGe 3D CMOS inverter

structure holds more advantages than the Si-Si 3D CMOS structure, which was widely studied.

6 Conclusion

Based on the good performance of SiGe material and MOS devices, a Si-SiGe 3D CMOS structure is introduced, which is simulated and analyzed using MEDICI. The input-output signal of a Si-Si 3D CMOS inverter and a Si-SiGe 3D CMOS inverter are simulated as well, and the simulation results indicate that the electrical performance of the Si-SiGe 3D CMOS is superior to that of the Si-Si 3D CMOS, and the delay time of the Si-SiGe 3D CMOS inverter is less than that of the Si-SiGe 3D CMOS inverter. Thus the Si-SiGe 3D CMOS structure holds more advantages than the widely studied Si-Si 3D CMOS structure, and Si-SiGe 3D CMOS should be a promising IC technology.

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Si-SiGe 材料三维 CMOS 集成电路技术研究*

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摘要：根据 SiGe 材料的物理特性，提出了一种新有源层材料的三维 CMOS 集成电路. 该三维 CMOS 集成电路前序有源层仍采用 Si 材料，制作 nMOS 器件；后序有源层则采用 SiGe 材料，以制作 pMOS 器件. 这样，电路的本征性能将由 Si nMOS 决定. 使用 MEDICI 软件对 Si-SiGe 材料三维 CMOS 器件及 Si-SiGe 三维 CMOS 反相器的电学特性分别进行了模拟分析. 模拟结果表明，与 Si-Si 三维 CMOS 结构相比，文中提出的 Si-SiGe 材料三维 CMOS 集成电路结构具有明显的速度优势.

关键词：Si-SiGe；三维；CMOS；集成电路

PACC：7320D；7360T

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