A high efficiency PWM CMOS class-D audio power amplifier*

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Abstract: Based on the difference close-loop feedback technique and the difference pre-amp, a high efficiency PWM CMOS class-D audio power amplifier is proposed. A rail-to-rail PWM comparator with window function has been embedded in the class-D audio power amplifier. Design results based on the CSMC 0.5 μm CMOS process show that the max efficiency is 90%, the PSRR is –75 dB, the power supply voltage range is 2.5–5.5 V, the THD+N in 1 kHz input frequency is less than 0.20%, the quiescent current in no load is 2.8 mA, and the shutdown current is 0.5 μA. The active area of the class-D audio power amplifier is about 1.47×1.52 mm^2. With the good performance, the class-D audio power amplifier can be applied to several audio power systems.

Key words: class-D audio amplifier; PWM; CMOS; high efficiency; rail-to-rail comparator; difference

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1. Introduction

Conventional class-A, B, or AB audio amplifiers directly amplify the analog signals and must work in the triode region. Although class-AB audio amplifiers have high fidelity, their power dissipation is obvious and conversion efficiency is below 50%, which hardly satisfy the requirement of energy-saving. Some methods (such as employing push-pull output stage) are applied to compensate class-AB amplifiers, but when the power is high, power devices are still threatened and power output is limited, thereby the practical conversion efficiency is 30%–40% no matter that the theoretical value would be 78.5%, leading to a serious energy waste problem. At the same time we must increase the chip area or even add a plus radiating flange for the elimination of heat, thus too much area is taken and also the cost is unaffordable. On the other hand, class-D amplifiers have many advantages over the class A, B, or AB mentioned above, the characteristic working on the switching state make the theoretic efficiency could be 100%, the practical value could be over 80%, and so power dissipation, chip area and area taken by PCB could be greatly reduced. Since present electronic industry aims at small volume, low power and high efficiency, class-D amplifiers have a bright future[1–9].

At present, class-D audio power amplifiers have already been used in consumer electronic products such as DVD, LCD-TV, MP4 and cell phone. Compared to the conventional class-AB audio power amplifier, its greatest advantage is the high efficiency, the practical efficiency would be over 80%, and the theoretical efficiency would be 100%. In the class-D audio power amplifier, we compare the audio signal and high frequency constant signal, then modulate this compared result using the constant frequency carrier waves, thus digital signal is converted into PWM signal, which is of changeable pulse width and constant carrier frequency (hundreds kHz generally). The PWM signal is amplified by MOSFET, and the amplified PWM signal carrier frequency is removed by LC low-pass filter, thereby the original baseband audio signal drive speaker is obtained.

Based on the difference closed-loop feedback technique and the difference pre-amp, a high efficiency PWM CMOS class-D audio power amplifier is proposed, and a rail-to-rail comparator with window function is proposed as PWM comparator. The entire circuit is simulated and verified based on CSMC 0.5 μm CMOS process, and is proved to be of high efficiency and low power consumption.

2. High efficiency PWM class-D audio power amplifier

Since that system stability and noise characteristic of the closed loop system are much better than open loop system[9], we employ closed loop class-D audio power frequency architecture, with a feedback system, which is used to reduce the distortion. Considering the application without filter, full differential structure is used as input stage, a full differential operational amplifier cascaded as full differential integrator.

The proposed class-D amplifier as shown in Fig.1 is a fully differential amplifier with differential inputs and outputs. The fully differential amplifier consists of a differential amplifier and a common-mode amplifier. The differential amplifier ensures that the amplifier outputs a differential voltage on the output that is equal to the differential input times the gain. The common-mode feedback ensures that the common-mode

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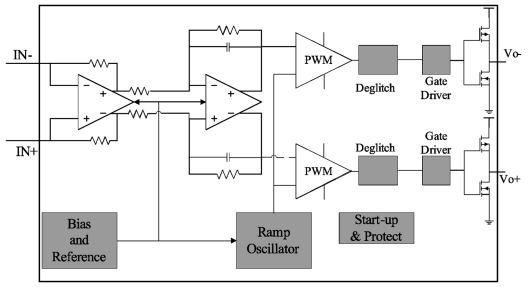

Fig.1. Diagram of class-D audio power amplifier.

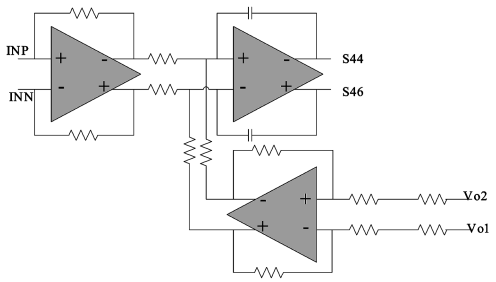

Fig.2. Diagram of preamplifier and feedback circuit.

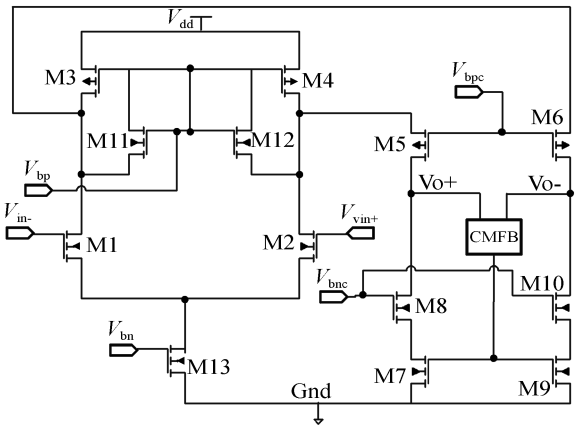

Fig.3. Full differential operational amplifier circuit.

voltage at the output is biased around $V_{DD}/2$ regardless of the common-mode voltage at the input. The proposed class-D amplifier can still be used with a single-ended input. However, the proposed class-D amplifier should be used with differential inputs when in a noisy environment, like a wireless handset, to ensure maximum noise rejection.

The fully differential amplifier allows the inputs to be biased at voltage other than mid-supply. For example, if a codec has a mid-supply lower than the mid-supply of the proposed class-D amplifier, the common-mode feedback circuit will adjust, and the proposed class-D amplifier outputs will still be biased at mid-supply of the proposed class-D amplifier. The inputs of the proposed class-D amplifier can be biased from 0.5 to $V_{DD} - 0.8$ V. If the inputs are biased outside of that range, input-coupling capacitors are required.

The fully differential amplifier does not require a bypass capacitor. This is because any shift in the mid-supply affects both positive and negative channels equally and cancels at the differential output. GSM handsets save power by turning on and shutting off the RF transmitter at a rate of 217 Hz. The transmitted signal is picked-up on input and output traces. The fully differential amplifier cancels the signal much better than the typical audio amplifier.

The diagram of class-D audio power amplifier in Fig.1 mainly includes input circuit, output drive circuit, logic control unit, dead zone control unit, PWM oscillator module, feedback circuit, soft start circuit, turnoff module, switching noise control module and so on. Input circuit is full differential operational amplifier, to limit the noise, increase the output voltage swing, and include the preceding proportional amplifier, connecting the full differential integrator constituted by full differential operational amplifier. PWM oscillator circuit generates a triangle wave, and the principle is to charge and discharge a capacity, the current of charge and discharge is generated by the same reference current mirror, for the same capacity, the time for charging and discharging is equal, and so to form a triangle wave, the oscillating frequency of which is determined by the capacitance and current, 250 kHz in this paper. PWM module, the most significant configuration in class-D audio amplifier, is mainly composed with two hysteresis comparators, generates square waves with different duty cycle by comparison with full difference of the preceding input circuit. The feedback module adopting two parallel RC filters, and the signal is fed to the differential input terminal of full differential integrator through a full differential operational amplifier.

3. Pre-amp and feedback of class-D audio power amplifier

Pre-amp and feedback of class-D audio power amplifier is shown in Fig.2, full differential operational amplifier is applied as the input stage, to pre-amplify the input difference audio signal, and its single terminal gain is determined by the value of external connected resistance. For the best performance, the single terminal gain should set below 2, in that low gain could drive the chip to work on the best state, and the high input voltage may make the input terminal insensitive to the noise. Hence, when the input voltage is low, should be pre-amplified by an amplified circuit, instead of reducing the resistance to increase the circuit gain.

As shown in Fig.2, the first stage of the input configuration is full differential proportional amplifier, the second stage is full differential integrator. The feedback module adopting two parallel RC filters, and the signal is fed to the differential input end of full differential integrator through a full differential operational amplifier. So, the most significant configuration in class-D audio amplifier pre-amplifier and feedback segment is full differential CMOS operational amplifier.

The full differential operational amplifier adopting the folded-Cascode configuration and the interior circuit is shown in Fig.3. The biased circuit and common-mode circuit is not presented due to the extent limit. M1–M3 compose the input stage difference amplifier, M3–M6 compose the output stage circuit, where M3, M4 are the power source, M5 and M6 are common-gate amplifier, M8 and M10 compose the active load transistor, M7 and M9 compose common-mode feedback

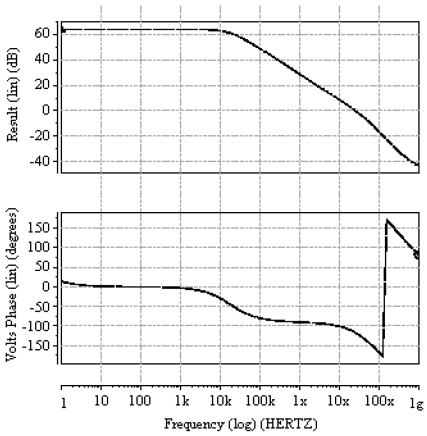

Fig.4. CMOS operational amplitude/phase-frequency characteristic.

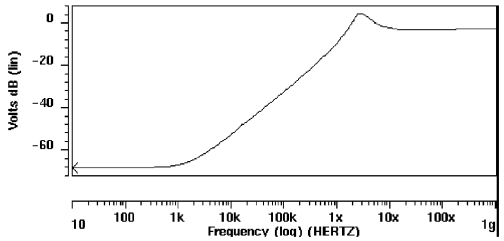

Fig.5. Power-supply rejection ratio characteristic of CMOS operational amplifier.

circuit, M11 and M12 are clamping transistors used for reducing the operational amplifier setting time, having no effect on AC small signal characteristics. Analyzing the circuit in Fig.3 according to the small signal model, and the voltage gain is

$$A_{\mathrm{V}} = -(g_{\mathrm{mn}}r_{\mathrm{on}})(g_{\mathrm{mp}}r_{\mathrm{op}})\frac{1}{1 + r_{\mathrm{on}}/R_{\mathrm{S}} + r_{\mathrm{on}}/R_{\mathrm{N}}}\frac{1}{1 + r_{\mathrm{op}}/R_{\mathrm{L}}}, \quad (1)$$

where g_{mn}, r_{on}, g_{mp} and r_{op} are the transconductance and output resistance of NMOS and PMOS, respectively, and R_{L}, R_{S} are the limited output resistance of power supply. R_{N} is the source equivalent input resistance of NMOS, and $R_{\mathrm{N}} = \frac{1}{g_{\mathrm{mp}}}(1 + \frac{R_{\mathrm{L}}}{r_{\mathrm{op}}})$, so we can improve the limited output resistance of power supply to improve the DC gain of operational amplifier. If the output resistance of the load is much bigger than that of MOS, the max gain of full differential Cascode CMOS operational amplifier will be simplified as

$$A_{\mathrm{Vmax}} = -2(g_{\mathrm{mn}}r_{\mathrm{on}})(g_{\mathrm{mp}}r_{\mathrm{op}}). \quad (2)$$

Based on BSIM3V3 model of CSMC 0.5 μm CMOS process, PWM comparator characteristic is simulated using Hspice, under the condition that power voltage V_{DD} is 5 V, temperature is 25 °C (room temperature). Figure 4 is the CMOS operational amplitude/phase-frequency characteristic. The greatest open loop gain is 63.7 dB, phase margin is 63 °C, and unit gain band width frequency is 26.1 MHz, which can relax the class-D audio power amplifier requirement. Figure 5 shows the power-supply rejection ratio characteristic of full differential CMOS operational amplifier. The PSRR is 68.4 dB, which can totally satisfy the wide power voltage application requirement of class-D audio power amplifier.

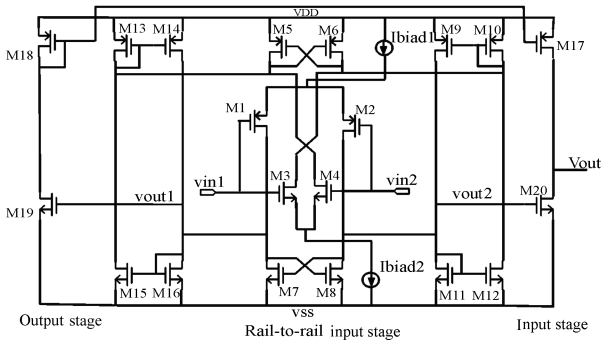

Fig.6. Rail-to-rail comparator with hysteresis function.

4. PWM rail-to-rail comparator

In order to improve the accuracy and gain of the comparator, PWM comparator circuit employs two-stage open loop comparator configuration, and for the reason that the comparator is applied in audio circuit, a noisy circumstance, also detect the signal variation at the threshold value, general comparators are inevitable to present noise at the output, thus we add the hysteresis configuration. M5, M13, M6, M10, M7, M11, and M8, M16 in Fig.6 are composed as corresponding hysteresis circuit, so to improve the anti-interference ability of comparator. As the comparator in class-D audio amplifier, its output modulation wave experienced a series digital logic change to control the power MOSFET. The best choice for the comparator common mode output to make MOSFET work normally is $V_{\mathrm{SS}} - V_{\mathrm{DD}}$, the full range output, which means it is necessary for the comparator common mode input range to be $V_{\mathrm{SS}} - V_{\mathrm{DD}}$, therefore, we must adopt rail-to-rail structure as the comparator input stage. This mentioned structure is usually made up of a parallel complementary P, N differential pair，and the input stage configuration, composed of NMOS M3, M4 and PMOS M1, M2, is shown in Fig.6. The common mode input range for PMOS differential pair is $V_{\mathrm{SS}} < V_{\mathrm{CM}} < V_{\mathrm{DD}} - |V_{\mathrm{DS}}| - |V_{\mathrm{GS}}|$, $V_{\mathrm{SS}} + V_{\mathrm{DS}} + V_{\mathrm{GS}} < V_{\mathrm{CM}} < V_{\mathrm{DD}}$ for NMOS pair, according to these two expressions, the common mode input range for this comparator is $V_{\mathrm{SS}} < V_{\mathrm{CM}} < V_{\mathrm{DD}}$.

The common mode input range of Rail-to-Rail architecture could be divided into three working regions: When V_{CM} is low, M1, M2 are turned on, M3, M4 are turned off, and the biased current is provided by $I_{\mathrm{bias1.}}$ When V_{CM} is high, M3, M4 are turned on, M1, M2 are turned off, and the biased current is provided by I_{bias2}. If V_{cm} is in intermediate range, the biased current is offered by both upper and lower tail currents, and then the sum of biased current will be I_{bias1}+I_{bias2}. The input stage total trans-conductance of rail-to-rail architecture is determined by

$$I_{\mathrm{D}} = \frac{1}{2}\mu C_{\mathrm{ox}}(\frac{W}{L})(V_{\mathrm{GS}} - V_{\mathrm{TH}})^2(1 + \lambda V_{\mathrm{DS}}). \quad (3)$$

Ignoring the channel modulation effect (λ=0), we get the total trans-conductance through derivation:

$$g_{\mathrm{m,total}} = \sqrt{\mu_{\mathrm{n}}C_{\mathrm{ox}}\left(\frac{W}{L}\right)_{\mathrm{n}} I_{\mathrm{bias2}}} + \sqrt{\mu_{\mathrm{p}}C_{\mathrm{ox}}\left(\frac{W}{L}\right)_{\mathrm{p}} I_{\mathrm{bias1}}}. \quad (4)$$

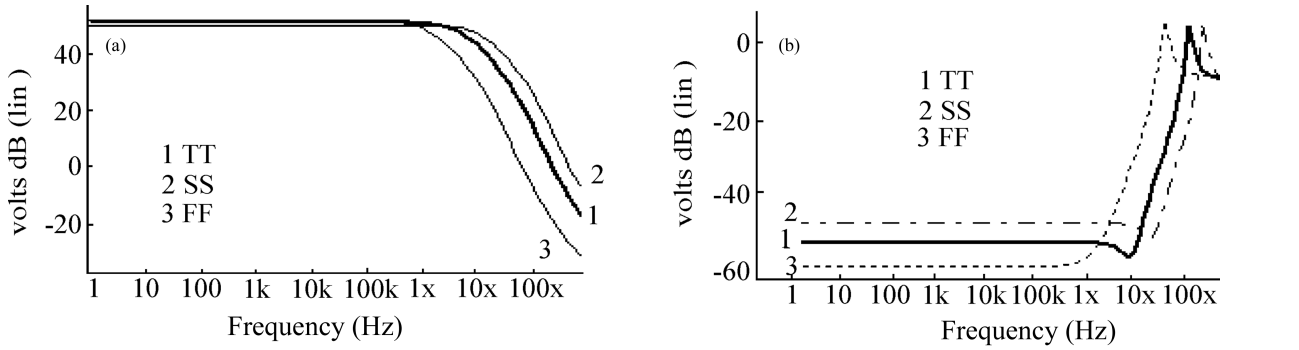

Fig.7. AC characteristics of PWM comparator: (a) DC gain; (b) PSRR.

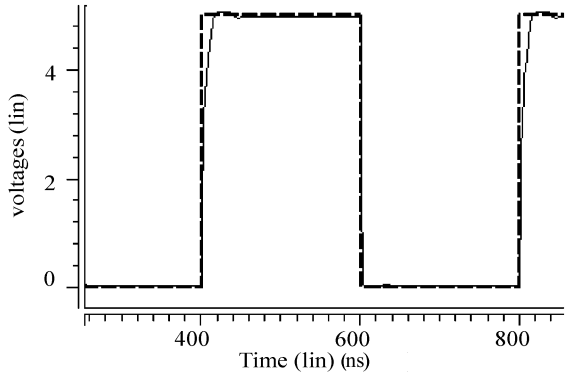

Fig.8. Transient simulated results.

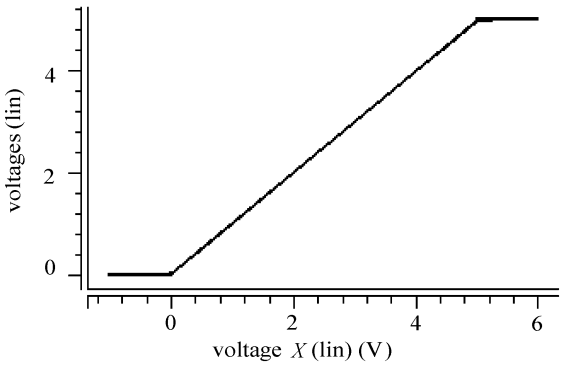

Fig.9. Results in the common mode input range.

According to Eq.(4), rail-to-rail circuit regulates the input stage total biased current to realize the total trans-conductance to be constant, the comparator performance improved.

The comparator output stage adopts the basic difference structure without constant-current source, shown in Fig.6, M19, M20 are the differential input, M18, M17 compose the image load, M20, M17 are the typical class-AB output architecture, and therefore realizing rail-to-rail voltage output. At the same time, every MOS in output stage is chosen as $(\frac{W}{L})_{17} = (\frac{W}{L})_{18} = (\frac{W}{L})_{19} = (\frac{W}{L})_{20} = \frac{30\,\mu\text{m}}{1\,\mu\text{m}}$, which means they are matching with each other, and do the small signal analysis to get the gain expression as

$$A_{\text{V}} = g_{\text{m19,20}}\left(r_{\text{O19,20}} | r_{\text{O17,18}}\right). \tag{5}$$

Based on BSIM3V3 model of CSMC 0.5 μm CMOS process, PWM comparator characteristic is simulated using Hspice, under the condition that power voltage V_{DD} is 5 V, temperature is 25 °C (room temperature). Analyzing the circuit with AC model TT, SS, FF, the simulated results is shown in Fig.7. The comparator DC gain is shown in Fig.7, TT 50 dB, SS 51 dB, FF 49 dB; PSRR in TT, SS, FF is 52, 47, 58 dB respectively, which indicates that process error has little effect on PWM comparator DC open loop gain and PSRR.

Transient simulated waveform is shown in Fig.8. The rise and fall transfer time delay of the comparator is 44 and 5 ns respectively, analyzing the circuit with TT model, and the total time delay is 24.5 ns. The comparator positive slew rate and negative slew rate is 360 and –3600 V/μs respectively. The simulated result suggests that rise delay is longer than fall delay. Because of the reason that M17 and M20 in the output stage have the same W/L and the different mobility between holes in PMOS and electronics in NMOS leading to the different driving ability between these two kinds of transistors. The designed comparator is mainly applied in audio, working under low frequency state, 250 kHz. On the basis of the simulated results, we can conclude that, when the frequency is low the comparator is of shorter transfer delay, the quicker response. Figure 9 is the simulated dc characteristic, and ICMR range is from 0 to 5 V, at the same time output swing reaches the full range. Hence, output signal of the comparator can thoroughly drive the following audio logic circuit, and thereby ensure the fidelity of the audio signals.

The comparator waveform, at normal state, with sine wave (frequency 10 kHz and amplitude in the range of 1.3–3.7 V) and triangle wave (frequency 250 kHz and amplitude in the range of 1.2–3.8 V) as the input waves, is shown in Fig.10 (a). We intercept a passage of simulated wave and present its amplification in Fig.10 (b), and the imaginary line is the sampled PWM wave. To avoid the signal distortion after sampling, the amplitude of sine wave should be lower than that of triangle wave, and we regulate the gain of preamplifier to avoid over regulation for the large amplitude signals. Moreover, the layout of input different transistors pair should be considered to reduce the comparator offset voltage.

5. Design results and discussion

Based on CSMC 0.5 μm N-well DPDM CMOS process, the proposed high efficiency class-D audio power amplifier is simulated, silicon verified and measured. When the load is the equivalent loudspeaker 8 Ω, V_{DD} = 3.6 V, input signal is 10 kHz

Table 1. Power and efficiency measured results with different power supplies.

Power supply (V)	Input signal frequency (kHz)	Load (Ω)	THD+N (%)	Output power (W)	Conversion efficiency (%)
2.5	1	4	1.0	0.42	75.7
3.6	1	4	1.0	1.06	80.4
5.0	1	4	1.0	2.08	85.8
2.5	1	8	1.0	0.26	83.5
3.6	1	8	1.0	0.59	86.3
5.0	1	8	1.0	1.19	90.1

Table 2. THD+N measured results with different power supplies.

Power supply (V)	Input signal frequency (kHz)	Load (Ω)	Output power (W)	THD+N (%)
2.5	1	8	0.20	0.20
3.6	1	8	0.50	0.19
5.0	1	8	1.00	0.18

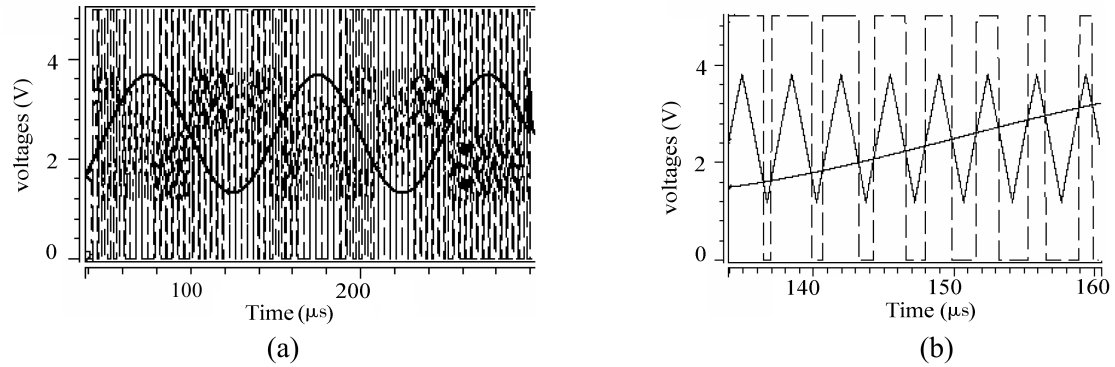

Fig.10. Output waves of PWM comparator: (a) Comparator output; (b) Amplified output waves.

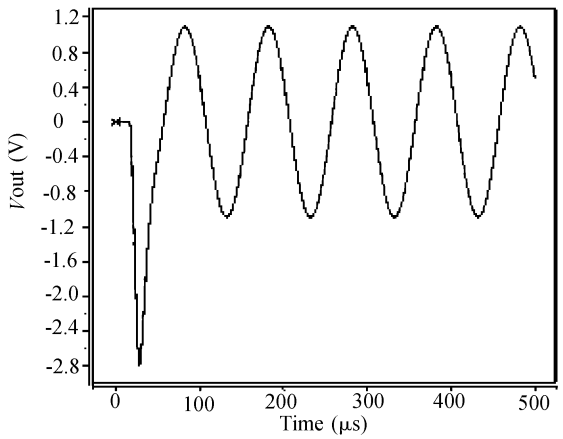

Fig.11. Simulated result of the entire circuit.

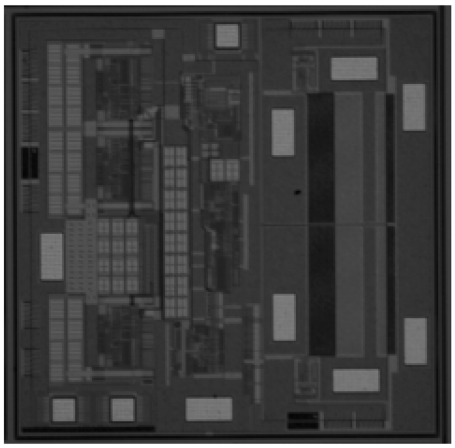

Fig.12. Micro-photo of the class-D amp.

300 mV differential sine wave with the phase difference of 180 °C, the simulated results of class-D audio power amplifier in the 0.5 μm CMOS process typical model is presented in Fig.11, the stabilized output sine wave signal is complete, THD+N is 0.154%.

Table 1 is the output power and efficiency measured result of the proposed class-D audio power amplifier, with kinds of voltage and load 4, 8 Ω, respectively, and the maximum conversion efficiency is up to 90%, which is twice of that of conventional class-AB under the same condition. Table 2 is the THD+N measured results with different power supply with 8 Ω load and 1 kHz input signal, and the THD+N is less 0.20%. When the output power is reach to 2.5 W, the conversion efficiency is about 85%. The power supply is in the range of 2.5–5.5 V, PSRR is about –75 dB. When power supply is 3.6 V, the quiescent current with no load is 2.8 mA and shutdown current is 0.5 μA, which can satisfy the low power condition. Figure 12 is the micro-photo of class-D audio power amplifier chip base on CSMC 0.5 μm N-well DPDM CMOS process, and the effective area is 1.47×1.52 mm^2.

Reference [5] proposed a 2.5 W, 250 kHz PWM class-D audio power amplifier based on BiCMOS process with power supply 2.5–6.5 V and maximum efficiency 86% with 8 Ω load (800 mW), while the values 2.5–5.5 V and 90% efficiency respectively with an 8 Ω load (800 mW) for the proposed class-D audio power amplifier in the paper, which is better.

6. Conclusion

This paper proposed a high efficiency PMOS CMOS class-D audio power amplifier based on feedback close-loop configuration, adopting full differential pre-amp and full differential feedback, and proposes a rail-to-rail comparator with hysteresis architecture as the PWM comparator. The entire circuit is simulated, verified and measured based on CSMC 0.5 μm CMOS process. The maximum conversion efficiency is up to 90%, the range of power supply is 2.5–5.5 V, and THD is less than 1% with 10 kHz frequency; for good performance this amplifier can be used in various kinds of small and medium power audio amplification system.

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