A 3.96 GHz phase-locked loop for mode-1 MB-OFDM UWB hopping carrier generation*

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Abstract: A fully integrated phase-locked loop (PLL) is presented for a single quadrature output frequency of 3.96 GHz. The proposed PLL can be applied to mode-1 MB-OFDM UWB hopping carrier generation. An adaptive frequency calibration loop is incorporated into the PLL. The capacitance area in the loop filter is largely reduced through a capacitor multiplier. Implemented in a CMOS process, this PLL draws 13.0 mA current from a single 1.2 V supply while occupying 0.55 mm^2 die area. Measurement results show that the PLL achieves a phase noise of –70 dBc/Hz at 10 kHz offset and –113 dBc/Hz at 1 MHz offset. The integrated RMS jitter from 1 kHz to 10 MHz is 2.2 ps. The reference spur level is less than –68 dBc.

Key words: phase-locked loop; adaptive frequency calibration; loop filter; CMOS; UWB
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1. Introduction

Being driven by market demands, different wireless communication systems are continuously emerging. The ultra-wideband (UWB) system is the one that has attracted much attention for its advantages of short-range, high-data-rate (>100 Mb/s), and high-security communication. The unlicensed band of 3.1–10.6 GHz is divided into 14 sub-bands, each with a spacing of 528 MHz, for the multi-band orthogonal frequency-division multiplexing (MB-OFDM) system[1]. These sub-bands are grouped into five groups. In particular, the lowest three bands in the first band group (3.432, 3.96, and 4.488 GHz) are allocated to first generation devices (mode 1 or mandatory mode) for MB-OFDM UWB systems.

Recently, many frequency synthesizers for direct-conversion UWB systems have been reported[2–4]. The possible ways of performing frequency generation in a UWB system are discussed in Ref. [2]. In mode 1 operation, there exists a common factor of 264 MHz among the three carriers. In a single PLL implementation, one simple approach is to set the base frequency to 4.224 GHz[5] and use a series of divide-by-2 dividers and SSB-mixers for the creation of the desired deviation. The main problem of this architecture is that the image tone will be at the adjacent sub-band center since a deviation of 264 MHz is used. The synthesizer architecture proposed in Ref. [3] can alleviate the image contamination problem. It employs a fixed 3.96 GHz PLL and generates a deviation of 528 MHz using a divide-by-7.5 regenerative frequency divider to translate the carrier frequency in a SSB mixer, as shown in Fig. 1. In this paper, a fully integrated 3.96 GHz CMOS PLL for a mode-1 MB-OFDM UWB frequency synthesizer will be presented, which is based on the architecture proposed in Ref. [3].

2. PLL architecture

The performance of the PLL is one of the key factors determining the performance of the proposed synthesizer. According to Ref. [3], the proposed PLL should work at 3.96 GHz with quadrature outputs. A block diagram of the proposed PLL architecture is shown in Fig. 2. Because a single output frequency is being generated and there is no frequency switching, the integer-N architecture with fixed-N value

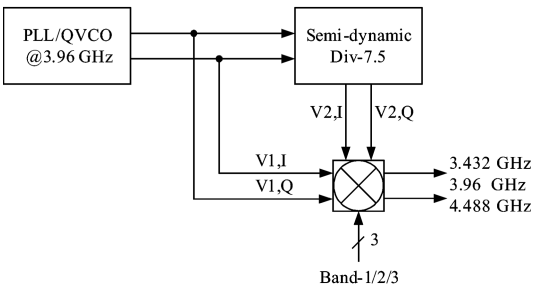

Fig. 1. Block diagram of direct frequency synthesizer with semi-dynamic dividers.

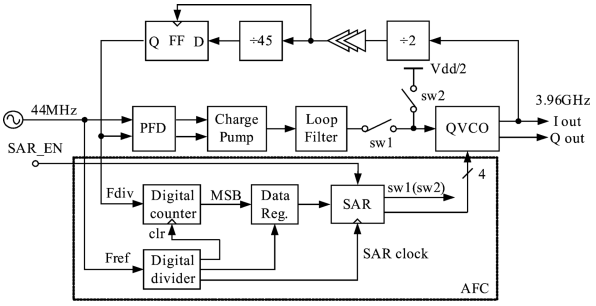

Fig. 2. Proposed PLL diagram for 3.96 GHz carrier signal generation.

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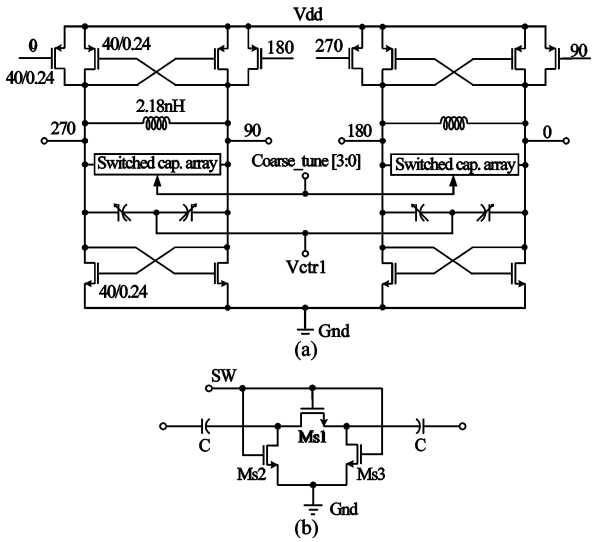

Fig. 3. (a) Schematic of the QVCO; (b) Switched capacitor cell.

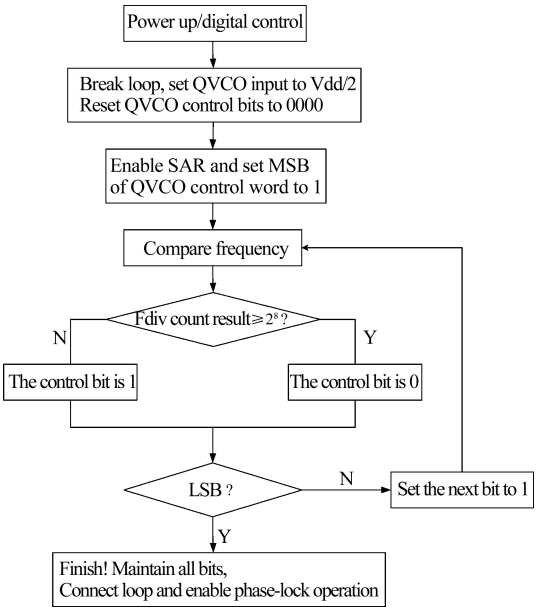

Fig. 4. Binary search diagram of SAR.

is chosen. As shown in the figure, the proposed PLL consists of a phase frequency detector (PFD), a charge pump (CP), a loop filter (LPF), a quadrature VCO (QVCO), a divider chain, and an adaptive frequency calibration (AFC) block. All the building blocks are integrated on a single chip in CMOS technology. Of all the implementation features, a low phase noise and low reference spur PLL design will be focused on.

3. Circuit implementation

3.1. QVCO

To generate quadrature signals at 3.96 GHz, a QVCO is implemented, as shown in Fig. 3(a)[6]. The QVCO consists of two cross-coupled LC VCOs with four pMOS coupling transistors. Here the sizes of coupling transistors are selected to be equal to the sizes of negative resistive transistors. The tail current source is omitted to eliminate its thermal noise contribution to the VCO phase noise. Omitting the current source will cause an increased sensitivity to the power supply, which can be solved by large decoupling capacitors connecting the power line and ground. Also, the power consumption can be limited by the W/L ratios of the negative resistive transistors.

The inductors in the LC tanks are implemented by using on-chip differential spirals. The varactor is a MOS type made of a gate and a n-diffusion in a n-well. The PVT, parasitic capacitance, and the accuracy of the inductor modeling will all affect the oscillation frequency. To compensate for the possibility of all the uncertainties, 4-bit switched capacitor arrays are added for each VCO tank. This digital tuning scheme divides a wide tuning range into 16 smaller bands, and the VCO gain decreases accordingly. One advantage, which comes from the small value of the VCO gain, is reduced sensitivity to the noise generated by the PLL's building blocks. The overlapping ratio between two adjacent bands slightly exceeds 50% to enable the desired output frequency point to fall near the middle of the tuning range. In order to reduce the effect of the MOS switches on the LC tank, the improved switched capacitor cell for each array is shown in Fig. 3(b). The nMOS transistor Ms1 is used as a switch to have the bottom plates of each pair of MIM capacitors either floating or connected to each other at a virtual ground in the differential mode. Additional nMOS transistors Ms2 and Ms3 are used to assure the DC potential of the switch transistor's channel during the on-state. The QVCO is designed to have a simulated overall frequency tuning range of 3.5–4.5 GHz.

3.2. AFC

As shown in Fig. 2, an AFC loop is incorporated in the proposed PLL to search for an optimum QVCO frequency band automatically. To simplify the design, an all digital AFC, including a counter-based frequency comparator and a successive approximation register-controlled (SAR) scheme, are used. The SAR algorithm sets the QVCO control bits one by one from the MSB to LSB, which is explained in Fig. 4. Each time the PLL is powered on, the phase-locked loop is broken, and the 4-bit QVCO control word is set to 0000 (corresponding to the highest QVCO frequency). After the SAR is enabled, the MSB is preset to 1. During each half calibration period (2^8 reference periods), the rising edges of the divided QVCO clock signal are counted and the MSB of the counting result in the 9-bit counter is checked at the end of this period. If the MSB equals 1, the divided QVCO clock signal frequency is larger than that of the reference. Otherwise, the divided QVCO clock signal frequency is smaller. Then the MSB of the QVCO control bits is changed or maintained accordingly. This process is carried on to the next bit until the LSB is preset and revised. After all the control bits are set to the proper value, they are maintained and the phase-lock operation is enabled.

The proposed counter-based frequency comparator is easy to implement in CMOS logic. The SAR calibration algorithm and circuit implementation are similar to that in Ref. [7]. To ensure sufficient calibration accuracy, the elapsed time in each calibration step is set to be 2^9 reference periods. The

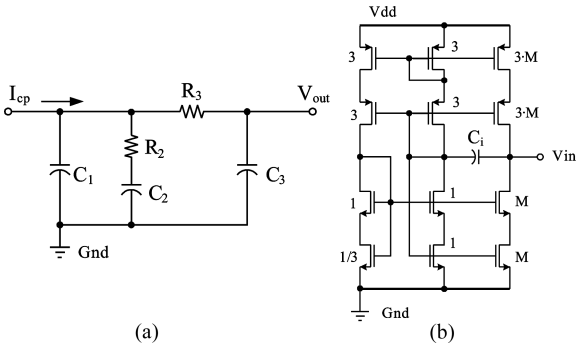

Fig. 5. (a) Third-order loop filter topology; (b) Implementation of the capacitor C_2.

total calibration time for the 4-bit control word is calculated to be $(4 + 1) \times 2^9$ reference periods, a value around 58 μs for a 44 MHz reference frequency. This does not matter since the PLL is designed to generate a single output frequency, i.e., 3.96 GHz, and it does not have strict settling time requirements.

3.3. LPF

For additional attenuation of the reference spur and other unwanted spurs, the proposed PLL uses a classical third-order loop filter (LPF) topology shown in Fig. 5(a). The expression for the loop filter impedance is shown to be

$$Z(s) = \frac{sT_1 + 1}{s(C_1 + C_2 + C_3)(sT_2 + 1)(sT_3 + 1)}. \quad (1)$$

The time constants, which determine the poles and zeros of the filter transfer function, can be expressed as

$$T_1 = R_2C_2, \quad (2)$$

$$T_2T_3 = \frac{R_2R_3C_1C_2C_3}{C_1 + C_2 + C_3}, \quad (3)$$

$$T_2 + T_3 = \frac{R_3C_3(C_1 + C_2) + R_2C_2(C_1 + C_3)}{C_1 + C_2 + C_3}. \quad (4)$$

However, to sufficiently suppress the in-band phase noise of the PLL and the reference spur, the loop bandwidth of the PLL open-loop gain is usually set to be less than 1/50 of the reference frequency. Such a small bandwidth usually makes the main capacitor C_2 too large to be integrated on the chip. To save the chip area occupied by C_2 while maintaining a small bandwidth, the cascaded self-biased capacitor multiplier (CSBCM) proposed in Ref. [8] is adopted to implement the capacitor C_2 in a more efficient way. As shown in Fig. 5(b), this capacitor multiplier is a simple structure with only 12 transistors. The fact that no bias circuitry is needed leads to a low-noise and low-power performance. According to Ref. [8], the capacitance C_2 could be replaced by the capacitor multiplier using the following equation:

$$C_2 = (1 + M)C_i. \quad (5)$$

To calculate the parameters of the loop filter, the PLL system parameters have to be given. In this design, the QVCO gain is 475 MHz/V, the divider modulus is 90, the charge pump

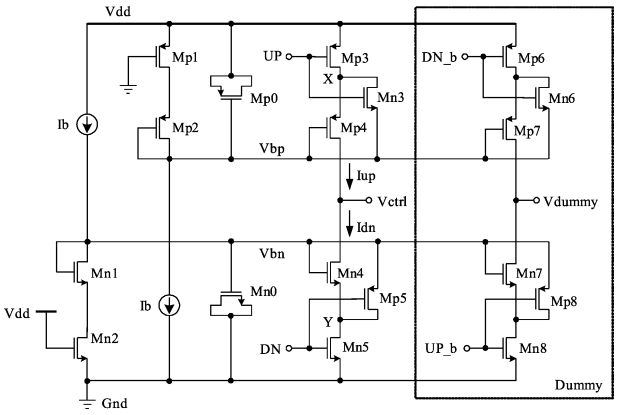

Fig. 6. Charge pump schematic.

current is 200 μA, the phase margin is around 55°, the ratio of the two non-zero poles in the loop filter is set to be 0.4, and the PLL bandwidth is set to be approximately 629 kHz. Based on these values, the parameters of the loop filter are summarized as follows: C_1 = 9.77 pF, M = 11, C_i = 17.23 pF, C_3 = 2.20 pF, R_2 = 3.89 kΩ, R_3 = 16.50 kΩ. As shown in Eq. (1), this loop filter topology poses one zero and two non-zero poles in the frequency response. The zero is located at 198 kHz, while the first pole is at 2.79 MHz. An additional pole is added at 6.98 MHz for reference spur rejection. It is worth noting that the QVCO input capacitance is parallel to the capacitor C_3; so the component C_3 should be at least four times as large as the QVCO input capacitance to avoid the PLL loop instability.

3.4. CP

The charge pump (CP) circuit shown in Fig. 6 is based on the design in Ref. [9]. The switches Mp3 and Mn5 control the current flow to the charge pump's output. In order to attenuate any switching errors that may reach the sensitive output node Vctrl, these switches are placed on the source side of the current source devices, Mp4 and Mn4. The gate voltages of Mn1 and Mp2 are adjusted to minimize the up/down charge mismatch when the phase lock is achieved. Transistors Mn3 and Mp5 are employed to ensure a fast turn-off of transistors Mp3 and Mn5. In the traditional design in Ref. [9], the source of nMOS transistor Mn3 is connected to ground; thus the voltage of node X may drop as low as ground, which may cause reverse current in Mp4. Similarly, the source of pMOS transistor Mp5 is connected to V_{dd}, and this may cause reverse current in Mn4. In the proposed design, the source of nMOS Mn3 and the source of pMOS Mp5 are tied to V_{bp} and V_{bn}, respectively. In this way, reverse current flowing in Mp4 and Mn4 can be avoided. To drive the switching transistors of the charge pump, inverting and non-inverting buffers are placed between the charge pump and the PFD (not shown in Fig. 6). The right part of Fig. 6 is a dummy branch to balance the load of the driving signals.

3.5. PFD and divider

The PFD compares both the phase and the frequency differences between the reference signal and the VCO feed-

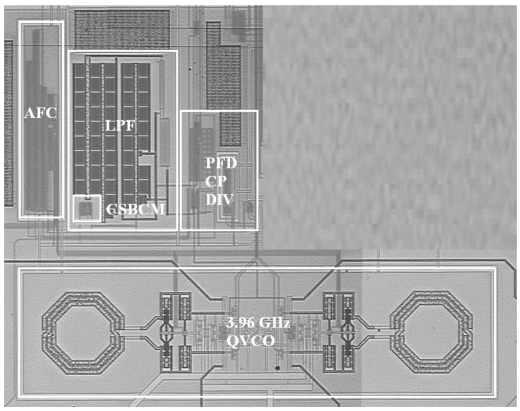

Fig. 7. Die photograph.

back signal. In order to minimize the abnormal operation of the PFD, true single-phase clock (TSPC) D-flip–flops are used since their intrinsic delays are smaller than those of conventional ones. The PFD circuit adopts the topology proposed in Ref. [10]. It consists of two simplified TSPC D-flip–flops and one NOR gate.

The main divider in the feedback path of the 3.96 GHz PLL has an integer ratio equal to $N = 90$. Factorizing in prime numbers gives the required divider ratios of the divider subcells: $N = 90 = 2 \times 3 \times 3 \times 5$. Since the first divide-by-2 section work at a rather high frequency and the input amplitude is not large, source-coupled logic (SCL) is used. The function of dividing the frequency by 2 is accomplished by two latches based on SCL. The SCL divide-by-2 circuit has two input ports but four output ports, so a dummy divide-by-2 circuit is added at the divide-by-2 circuit output to preserve the symmetry. The power rail of this dummy circuit is connected to ground to save its power consumption. High speed SCL dividers often consume large power. For low power consideration, the following three divider stages adopt dynamic TSPC D-flip-flops in a cascade. This FF is simple and they can be configured for divide-by-3 and divide-by-5 stages with CMOS logic. For better phase noise performance, a TSPC FF synchronizer clocked by the output of the CML divider is added at the divider output to eliminate the noise from the divider chain[6]. Also, a cascade of three CMOS logic inverters is inserted in the divider chain as shown in Fig. 2 to convert the logic swing from CML to CMOS.

4. Simulation and experimental results

This fully integrated PLL is fabricated in 0.13 μm CMOS technology and operates from a 1.2 V supply. The die photograph is shown in Fig. 7. The die occupies an area of about 0.55 mm^2. Each building block is encircled by double guard rings to minimize the digital noise coupling from the substrate to the sensitive analog/RF blocks. Some prudent layout techniques are used to maintain the symmetry of the QVCO.

The function of the AFC block was verified through a transistor level simulation. To accelerate the simulation speed, the QVCO block and the divider chain are replaced by behavioral modeling using verilog-A language[11]. Figure 8 shows

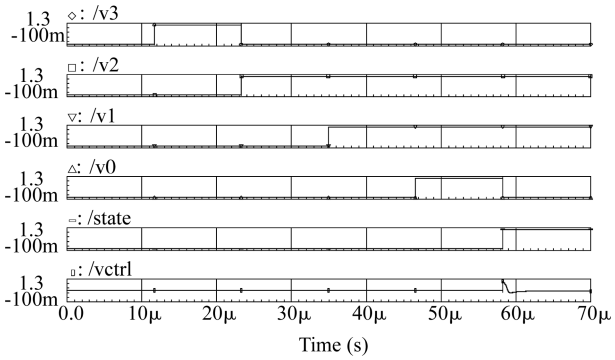

Fig. 8. Simulated timing diagram of the proposed AFC.

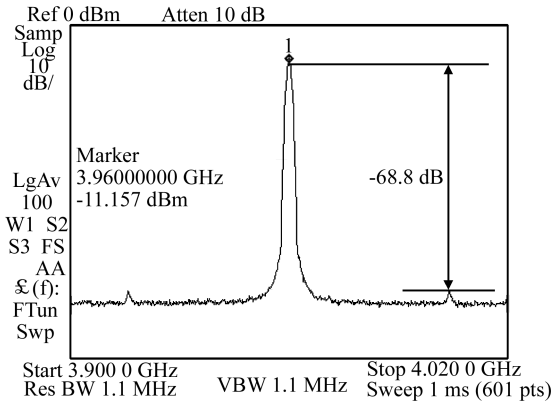

Fig. 9. Measured output spectrum of the locked PLL.

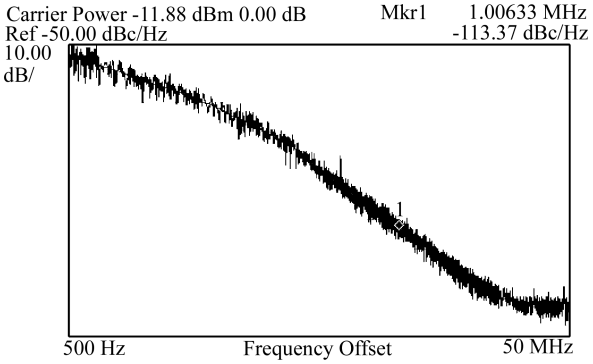

Fig. 10. Measured phase noise performance.

the simulation waveform for the proposed AFC. The signal bus v<3:0> represents the 4-bit QVCO control word. The signal "state" is the output of the SAR that controls the switches in Fig. 2. It indicates that AFC has finished its function when this signal goes from low to high. The signal "vctrl" is the voltage control signal connecting to the QVCO input. As can be seen in Fig. 8, after a time span of 58 μs, the PLL enters into a closed loop operation and soon locks to the desired frequency with the control voltage stabilizing at near half the supply voltage (V_{dd}/2). This result agrees well with the initial calculation.

The performance of the PLL was measured by using an Agilent E4440A spectrum analyzer.The output of the PLL was transmitted off-chip from the drain of an on-chip open-drain transistor connecting to the LC tank of the QVCO. Figure 9 shows the 3.96 GHz carrier output frequency along with the reference spurs. As can be seen, the proposed PLL locks to the desired frequency. The reference spurs are approximately –68.8 dB below the carrier. Figure 10 shows the phase noise

Table 1. Performance summary and comparison.

Reference	Ref. [12]	Ref. [13]	This work
Technology	0.18 μm CMOS	0.18 μm CMOS	0.13 μm CMOS
Supply (V)	1	1.8	1.2
Current Diss. (mA)	27.5	9	13
Reference Freq. (MHz)	10	10	44
Output Freq. (GHz)	5.45–5.65	5.47–5.65	3.96
Quadrature output	Yes	No	Yes
Phase noise (dBc/Hz)	–111 @ 1 MHz	–90 @ 100 kHz, –110.8 @ 1 MHz	–70 @ 10 kHz, –113 @ 1 MHz
Spurs (dBc)	< −80 @ 11 MHz	< −75	< −68.8
Size (mm^2)	0.99	0.61	0.55

performance of the 3.96 GHz output. The measured spot phase noise is –70 dBc/Hz at 10 kHz offset and –113 dBc/Hz at 1 MHz offset. The integrated RMS jitter from 1 kHz to 10 MHz is 2.2 ps.

Table 1 summarizes the measured performance of the proposed frequency synthesizer and presents a performance comparison with other frequency synthesizers recently reported for the 3–5 GHz clock signal generation application. It should be noticed that the AFC block used in the proposed PLL adds CMOS switches between the LPF and the QVCO. These nonideal switches will inevitably introduce some digital coupling noise to the voltage control line of the QVCO, which is very sensitive. So it could be concluded qualitatively that the performance of the QVCO due to the use of AFC will be degraded by several dB. However, the performance of the proposed PLL is still comparable to those published recently in the literature.

5. Conclusion

A 3.96 GHz PLL with an AFC loop has been implemented successfully. Each building block in the proposed PLL has been optimized for optimal performance. A capacitor multiplier is utilized in the loop filter to reduce the area of a large integrating capacitor. The PLL operates with a 1.2 V supply voltage and consumes 13 mA current. The phase noise is measured to be –113 dBc/Hz at 1 MHz frequency offset. The size of the PLL is 0.55 mm^2. Along with a semi-dynamic divide-by-7.5 regenerative divider, the proposed PLL can be used for mode-1 MB-OFDM UWB hopping carrier generation.

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