Effect of a reset-MOSFET in a high-speed comparator

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Abstract: A high-speed comparator design based on regeneration architecture, which can be used in a flash ADC, is presented. A threshold-limit-speed effect (TLSE) which limits the speed of the comparator was discovered and studied in detail. The size of the reset-MOSFET was optimized to resolve the TLSE and make the comparator work at the maximal speed. The results were confirmed by simulation and the corresponding circuit was realized in a flash ADC design in SMIC 0.18-μm CMOS technology. The test result shows that the comparator can work well at 2 GHz and can even work up to 2.8 GHz while the power dissipation is 3.2 mW.

Key words: comparator; high speed; TLSE; CMOS; ADC
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1. Introduction

High speed ADCs are key components of analog/digital interfaces. For the speed of the ADC, the comparator is the decisive component. A block diagram of a high speed comparator is shown in Fig. 1.

Latch and regeneration architecture has often been used in high speed comparator designs[1−3]. In this paper, a reset-MOSFET for a high-speed comparator is discussed. It is normally thought that a large reset-MOSFET can make the comparison faster. However, an overlarge one will cause a threshold-limit-speed effect (TLSE), which will slow down the comparison speed. The size of the reset-MOSFET was therefore optimized to resolve the TLSE and make the comparator work at the maximal speed.

Based on the discussion, a high-speed comparator has been designed and realized in a flash ADC design in SMIC's 0.18-μm CMOS technology. Measurement of the chip showed that the comparator circuit worked very well at 2 GHz and it could even work up to 2.8 GHz when the power dissipation was 3.2 mW.

2. Reset-MOSFET in a voltage comparator

In a high speed comparator, regeneration latches are often used[2]. The schematic of a voltage comparator is shown in Fig. 2.

When clk is "1", m1, m2, and m5 are on. The comparator turns the input voltages v_{in1} and v_{in2} to different currents through m3 and m4, and makes the comparison when the clk is "0" and m5 turns off.

It seems that m5 is only a reset-MOSFET in the comparator shown in Fig. 2. But actually, m5 plays a very important role in the comparison.

2.1. Theoretical analysis

The comparison speed of the circuit shown in Fig. 2 is determined by an overdrive recovery at nodes X and Y and by the regeneration speed of m6–m9[5]. The recovery time constant between nodes X and Y is:

$$\tau_{rec} \approx 2R_{5on}C_{tot}, \tag{1}$$

where C_{tot} is the parasitic capacitance seen at each of the nodes X and Y, and R_{5on} is the on-resistance of m5.

The regeneration time constant is:

$$\tau_{reg} \approx \frac{C_{tot}}{g_{m67} + g_{m89}}. \tag{2}$$

When the clock turns to "1", m5 turns on. The on-resistance of m5 is:

$$R_{5on} = \frac{L}{K'W(V_{GS} - V_T)}. \tag{3}$$

So it is normally thought that, as in Ref. [5], increasing the gate width of m5 can decrease R_{5on} and speed up the comparison. It seems that the wider m5 is, the higher the speed is.

But in the real situation, the comparison result does not obviously improve as m5's width increases because of the side effect brought about by the width increase.

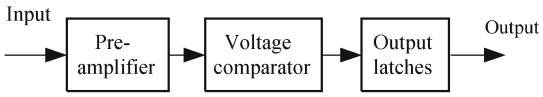

Fig. 1. Block diagram of a high speed comparator.

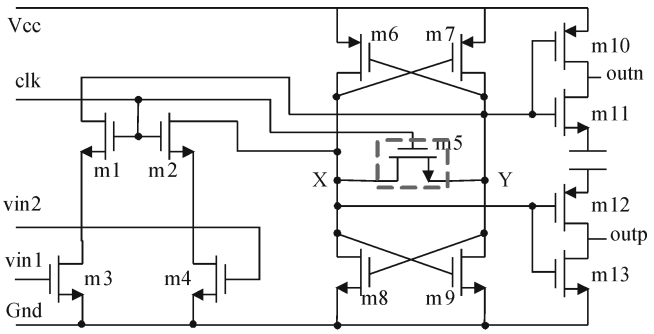

Fig. 2. Schematic of a voltage comparator.

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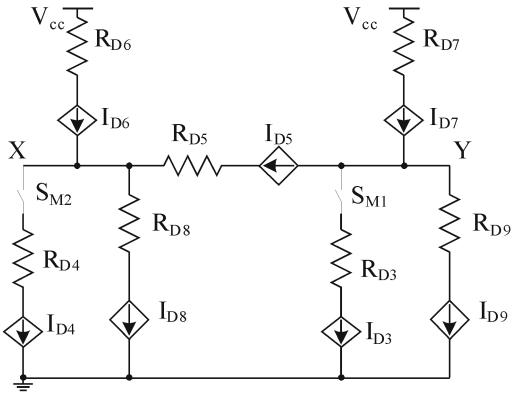

Fig. 3. Large-signal equivalent circuit at nodes X and Y.

When the clock turns from "0" to "1", m5 turns on. In the ideal condition, nodes X and Y in Fig. 1 would turn to the same mid-voltage. But in reality, it is impossible for the nodes X and Y to do this because of the on-resistance and I_{ds} of m5. This has an obvious effect on the comparison speed, which will be shown in Section 2.2.

The large-signal equivalent circuit at nodes X and Y is shown in Fig. 3.

It is hard to analyze all the different regions of the MOSFETs m3 to m9 when two input signals are changing. But one situation could show why nodes X and Y cannot turn to the same mid-voltage. When clk is "1", and supposing that $V_Y > V_X$ and m3, m4, m6–m9 all work in the saturation region, there is:

$$I_{D5} = I_{D7} - I_{D9} - I_{D3} = I_{D4} + I_{D8} - I_{D6}, \tag{4}$$

$$I_{D7} = K'_7 \frac{W_7}{2L_7} (V_X - V_{cc} - V_{TP})^2 = \frac{1}{2}\beta_7 (V_{cc} - V_X + V_{TP})^2, \tag{5}$$

$$I_{D9} = \frac{1}{2}\beta_9 (V_X - V_{TN})^2, \tag{6}$$

$$I_{D3} = \frac{1}{2}\beta_3 (V_{in1} - V_{TN})^2. \tag{7}$$

If $\beta_7 = \beta_9 = \beta$, $V_{TN} = -V_{TP} = V_T$, then

$$I_{D5} = I_{D7} - I_{D9} - I_{D3} = \frac{1}{2}\beta (V_{cc} - 2V_T)(V_{cc} - 2V_X) - \frac{1}{2}\beta_3 (V_{in1} - V_T)^2. \tag{8}$$

In the same way, it gives

$$I_{D5} = I_{D4} + I_{D8} - I_{D6} = \frac{1}{2}\beta_4 (V_{in2} - V_T)^2 - \frac{1}{2}\beta (V_{cc} - 2V_T)(V_{cc} - 2V_Y). \tag{9}$$

Adding Eqs. (8) and (9), it becomes

$$2I_{D5} = \frac{1}{2}\beta_4 (V_{in2} - V_T)^2 - \frac{1}{2}\beta_3 (V_{in1} - V_T)^2 + \frac{1}{2}\beta (V_{cc} - 2V_T)(2V_Y - 2V_X) = \Delta I_{in} + \beta (V_{cc} - 2V_T) V_{XY}, \tag{10}$$

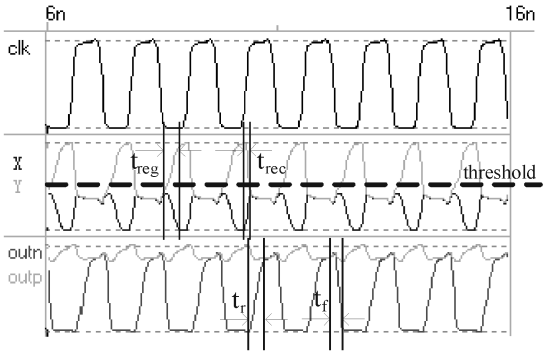

Fig. 4. Outputs with inaccurate threshold.

where ΔI_{in} is the different current caused by the different inputs v_{in1} and v_{in2}.

Also, $V_{XY} = I_{D5} R_{5on}$, and then there is:

$$V_{XY} = I_{D5} R_{5on} = \frac{1}{2}[\Delta I_{in} + \beta (V_{cc} - 2V_T) V_{XY}] R_{5on}. \tag{11}$$

From Eq. (11), there is:

$$V_{XY} = \frac{\Delta I_{in}}{\frac{2}{R_{5on}} - \beta (V_{cc} - 2V_T)}. \tag{12}$$

Equation (12) shows that the voltage difference between nodes X and Y, i.e., V_{XY}, decreases when the width of the reset-MOSFET increases. This proves that nodes X and Y in Fig. 2 are not able to turn to the same mid-voltage during actual working.

2.2. Threshold-limit-speed effect (TLSE)

The V_{XY} is worth of in-depth discussion.

An effect named TLSE caused by MOSFETs m10 to m13 should be discussed first.

The "not" gates composed of m10 to m13 supply the thresholds to nodes X and Y. If the threshold is not accurate for nodes X and Y, one of the outputs outn and outp is not stable. This means that one of them will rise and fall before it restores the corresponding logic voltage level, as shown in Fig. 4.

The output latches are used to latch the outputs following the voltage comparator. In order to latch the right outputs of the voltage comparator, the minimum clock period for the latches is:

$$t_{ltch} = t_r + t_f + t_{set}, \tag{13}$$

where t_r and t_f are the rise and fall times of the outn and outp in Fig. 4, and t_{set} is the setup time that the latches follow the voltage comparator.

If the threshold of the "not" gate is accurate for the nodes X and Y, the outputs outn and outp would be more stable, as shown in Fig. 5.

The minimum clock period for the latches is:

$$t'_{ltch} = t_{edge} + t_{set}. \tag{14}$$

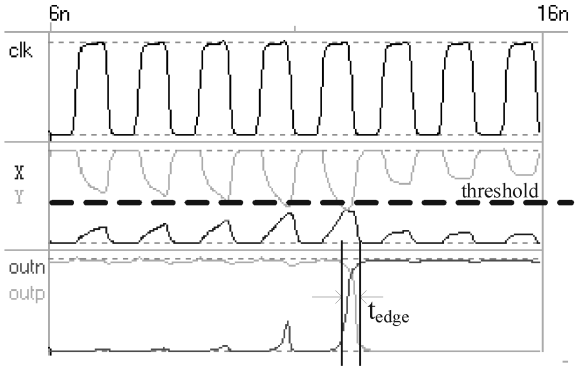

Fig. 5. Outputs with accurate threshold.

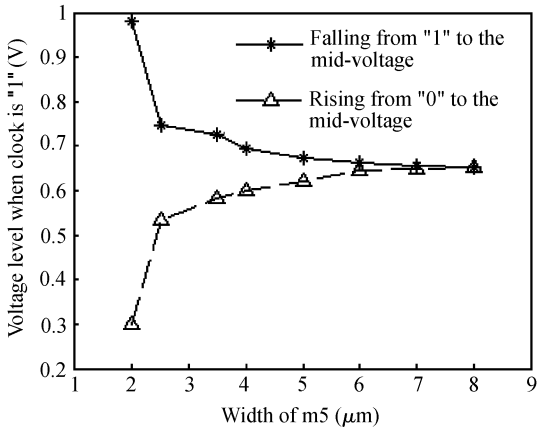

Fig. 6. Voltage level when the clock is "1" versus the width of m5.

Comparing Eqs. (13) and (14), $t'_{\rm ltch} < t_{\rm ltch}$, it is seen that an accurate "not" gate threshold can speed up the comparison. This TLSE is not obvious at a low speed, but more obvious at a high speed, such as 2–3 GHz, which will be shown in the simulation later.

2.3. Optimization of the reset-MOSFET

The TLSE shows that $V_{\rm XY}$ should not be very small, because a small $V_{\rm XY}$ makes it hard for the threshold to be accurate enough. It means the size of m5 is not the wider the better.

The voltage of nodes X and Y versus the different widths of m5 when $\Delta I_{\rm in}$ is fixed in Eq. (12) is shown in Fig. 6.

As shown in Fig. 6, when the clock turns to "1", one of nodes X and Y falls from "1" to the mid-voltage and the other one rises from "0" to mid-voltage. $V_{\rm XY}$, which is the difference between nodes X and Y, decreases as the width of m5 increases, as shown in Eq. (12).

The threshold of the "not" gate is:

$$V_{\rm thr} = \frac{V_{\rm cc} + V_{\rm tp} + V_{\rm tn}\sqrt{\beta_{\rm n}/\beta_{\rm p}}}{1 + \sqrt{\beta_{\rm n}/\beta_{\rm p}}}. \tag{15}$$

If $\beta_{\rm n} = \beta_{\rm p}$, $V_{\rm tn} = -V_{\rm tp}$, and $V_{\rm cc} = 1.8$ V, then $V_{\rm thr} = V_{\rm cc}/2 = 0.9$ V. But in the real fabrication process, it is impossible to be exactly accurate. Suppose $\beta_{\rm n}/\beta_{\rm p}$ is not equal to 1, but to 1.1 because the process error is 10%, and $V_{\rm TN} = -V_{\rm TP} = V_{\rm T} = 0.5$ V, giving $V_{\rm thr} = 0.89$ V. This means that the threshold error $\Delta V_{\rm thr}$ is about 10 mV.

Considering the process error in the real fabrication process, the $V_{\rm XY}$ should at least be:

$$V_{\rm XY} > 2\Delta V_{\rm thr} \approx 20\,{\rm mV}\,({\rm error} = \pm 10\%)\,. \tag{16}$$

This could make it easier for the threshold to be accurate, as shown in Fig. 5. Combining this with Eqs. (3) and (12), a new method to speed up the comparison has been proposed-reducing the width of m5.

It seems that reducing the width of m5 increases $\tau_{\rm rec}$ in Eq. (1), which is not good for the speed. Actually, properly increasing $\tau_{\rm rec}$ helps to reduce the swing range of nodes X and Y and keeps a more suitable $V_{\rm XY}$ for the "not" gate. Certainly, the width of m5 cannot be too small. A too small width makes $\tau_{\rm rec}$ too large to work at high speed. So, reducing the width of m5 properly to achieve a suitable $V_{\rm XY}$ as shown in Eq. (16) could speed up the comparison. The optimal size of m5 is that which makes $V_{\rm XY}$ just a little larger than $2\Delta V_{\rm thr}$ in Eq. (16) caused by the process error.

From Eqs. (5) and (12), it seems that increasing the width of m6 to m9 can also increase $V_{\rm XY}$. But the gain of the circuit consisting of m3 to m7 is equal to[6]

$$A_{\rm v} \approx g_{\rm m34} R_{\rm 5on}. \tag{17}$$

So, increasing the width of m6 to m9 has not made any contributions to the gain. In contrast, reducing the width of m5 could increase the gain, which is expected from the input sensitivity.

3. Realization of the comparator and the simulation result

Based on the discussion, a comparator that consists of a three-stage amplifier, a voltage comparator, and an output latches has been designed. The three-stage amplifier could reduce the input capacitance, which is expected at high speed[7].

The circuit of the complete comparator is shown in Fig. 7.

When the sampling clock is 3 GHz, the working waveforms at different widths of m5 are shown in Fig. 8. The output latches could not latch the right outputs because outn and outp in Fig. 8(a) are not stable, caused by TLSE. Contrary, the latches latch the right outputs in Fig. 8(b).

A diagram of input sensitivity versus sampling frequency at different frequencies of input signals is shown in Fig. 9.

The simulation shows that the speed of this comparator can reach up to 3 GHz.

4. Layout and the experimental result

The complete comparator was realized in a flash ADC design in SMIC 0.18-μm CMOS technology and occupies an active area of 60×10 μm^2. The layout of the comparator in the ADC is shown in Fig. 10(a) and a photograph of the comparator is shown in Fig. 10(b).

During testing, the output of the comparator is observed from the MSB of the ADC. Figure 11(a) shows the output and

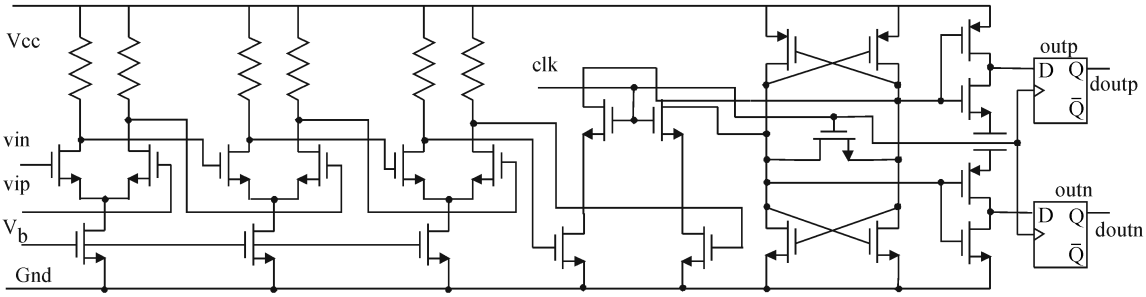

Fig. 7. Schematic of the complete comparator.

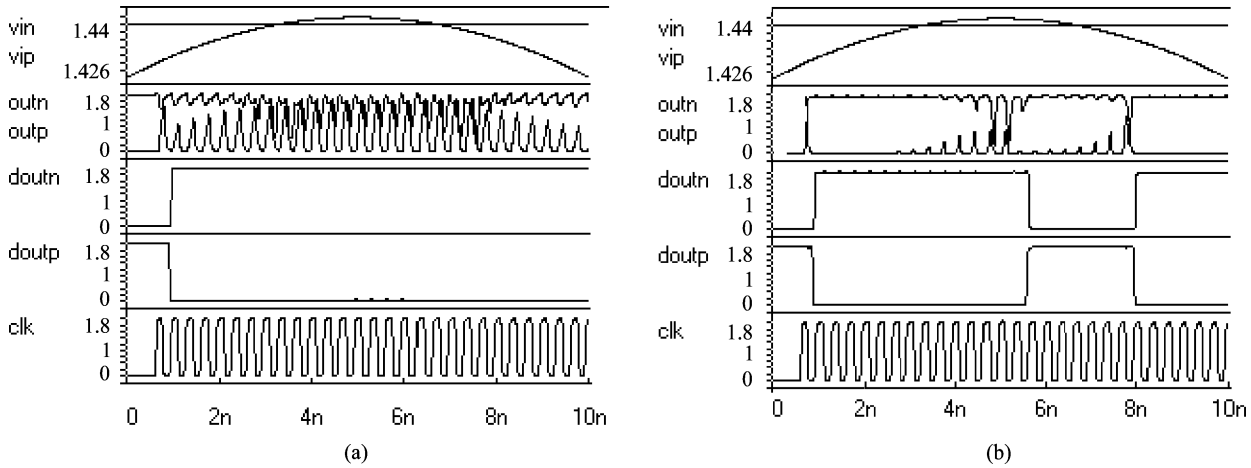

Fig. 8. Waveform of the complete comparator: (a) $W_5 = 20\ \mu$m; (b) $W_5 = 5\ \mu$m.

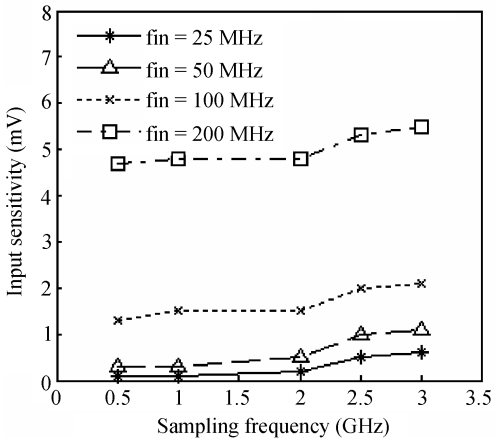

Fig. 9. Input sensitivity versus sampling frequency.

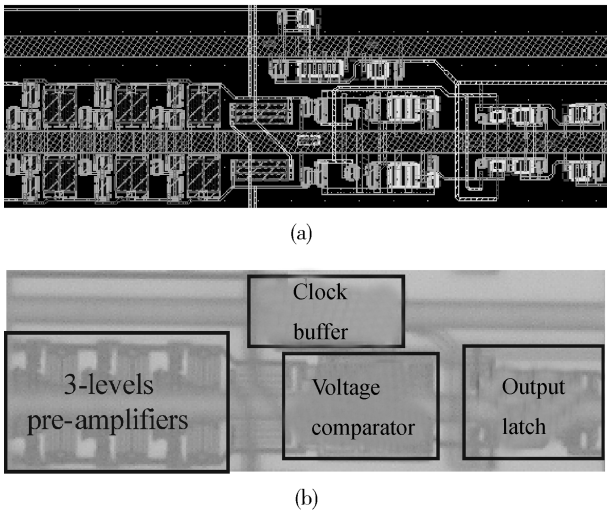

Fig. 10. (a) Layout of the comparator; (b) Photograph of the comparator.

the input sampling clock at a sampling clock of 2 GHz when the input signal is 1 GHz. In Fig. 11(b), the sampling clock is 2 GHz while one input signal is a sine wave of 100 MHz and the other is a DC voltage. In the actual testing, the peak of the sine wave is a little higher than the DC voltage. Figure 11(b) shows that the output turns to "1" every 20 clock cycles.

If one input signal is a sine wave and the other is a DC voltage at the mean of the sine wave, the output would be a square wave. In this condition, the test result shows that the sampling rate could reach 2.8 GHz.

The experimental results show that both the rise and fall times are 180 ps. The input offset error is less than 4 mV and the input sensitivity is less than 5 mV when the input frequency is less than 200 MHz.

A comparison between this design and some other comparators in a similar processes is listed in Table 1.

5. Conclusion

The significant effect of the reset-MOSFET on the speed of the comparator has been discussed. The TLSE has been discovered and resolved by decreasing the size of the reset-MOSFET, but not by increasing the size, as is shown in traditional analyses. An improved 2 GHz comparator has been presented. Simulation and actual testing have shown that this comparator can work well. Such a comparator has been successfully used in a flash ADC.

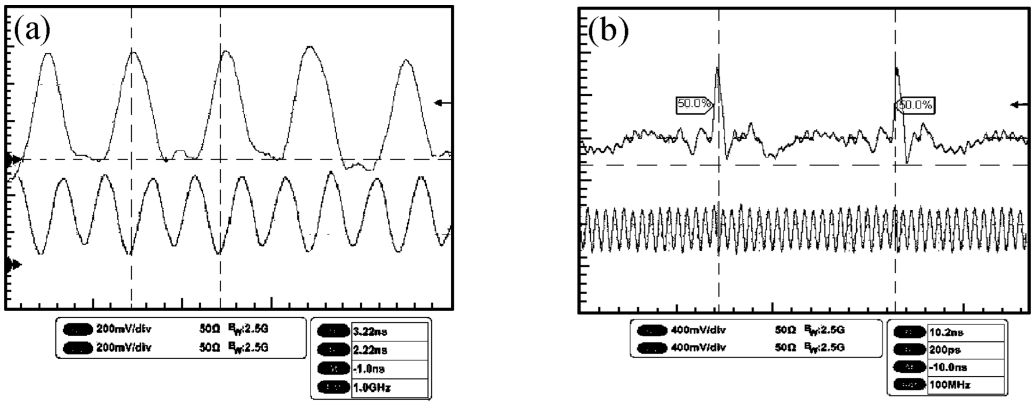

Fig. 11. Experimental results: (a) f_s = 2 GHz and f_{in} = 1 GHz; (b) Sampling at the limit inputs.

Table 1. Performance comparison.

Reference	Technology	Area (μm^2)	Max sampling frequency (GHz)	Offset (mV)	Input sensitivity (mV)	Power (mW)
Ref. [3]	0.18 μm CMOS	N/A	1.25	Close to zero	15	3 @ 1.25 Gsample
Ref. [4]	0.18 μm CMOS	N/A	1	N/A	< 4.5	N/A
Ref. [7]	0.35 μm CMOS	2100	1	< 200	N/A	0.18 @ 100 Msample
This design	0.18 μm CMOS	600	2.8	< 4	< 5	3.2 @ 2.8 Gsample

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