Influence of layout parameters on snapback characteristic for a gate-grounded NMOS device in 0.13-μm silicide CMOS technology*

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Abstract: Gate-grounded NMOS (GGNMOS) devices with different device dimensions and layout floorplans have been designed and fabricated in 0.13-μm silicide CMOS technology. The snapback characteristics of these GGNMOS devices are measured using the transmission line pulsing (TLP) measurement technique. The relationships between snapback parameters and layout parameters are shown and analyzed. A TCAD device simulator is used to explain these relationships. From these results, the circuit designer can predict the behavior of the GGNMOS devices under high ESD current stress, and design area-efficient ESD protection circuits to sustain the required ESD level. Optimized layout rules for ESD protection in 0.13-μm silicide CMOS technology are also presented.

Key words: electrostatic discharge; gate-grounded NMOS; snapback characteristic; layout parameters

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1. Introduction

Gate-grounded NMOS (GGNMOS) devices are the most vulnerable element to an electrostatic discharge (ESD) event due to the thin gate oxide and low drain breakdown voltage in submicron CMOS technology. The gate, source, and bulk of a GGNMOS device are connected to ground. The ESD protection mechanism of this device is based on snapback characteristics[1, 2]. The devices under ESD stress are operated in unconventional regions，such as high operation voltage and current. The characteristic I–V curve of a typical NMOS is plotted in Fig. 1. The I–V curve can be divided into four regions. Region 1 and region 2 are the linear and saturation regions respectively, described by the standard MOS equations. Region 3 is the avalanche breakdown region while region 4 is the snapback region. The standard MOS equations are no longer valid in these two regions. The NMOS ESD protection devices operated in region 1 and region 2 are under normal conditions and go to region 3 and region 4 under ESD stress.

Figure 1 also shows a snapback curve of a typical GGNMOS transistor obtained by the transmission line pulse (TLP) technique. The GGNMOS snapback parameters in the curve, such as V_{t1}, V_h, I_{t2}, R_{on}, are critical for measuring the ESD failure threshold voltage (ESDV) level of ESD protection devices. (I_{t1}, V_{t1}) is the trigger point, which decides when the ESD protection device turns on. (I_h, V_h) is the holding point; V_h shall ensure proper voltage clamping, low V_h provides a low-impedance discharge path. R_{on} is the snapback turn-on resistor, and can be expressed as[3]

$$R_{on} = \frac{\partial V_{ds}}{\partial I_{ds}}. \tag{1}$$

(I_{t2}, V_{t2}) is the second breakdown point, and ESDV level is represented by the second breakdown current I_{t2}. From the TLP-measured results, the human body mode (HBM) ESD level voltage can be approximated as[4, 5]

$$V_{\text{HBM ESD Level}} = (1500 + R_{on})I_{t2}. \tag{2}$$

So, from the snapback characteristic of the GGNMOS device, the designer can predict the HBM ESD level of the GGNMOS device without fabrication.

The ESD protection device should be designed in such a way that the snapback voltage V_{t1} is smaller than the thin gate oxide breakdown voltage (BV_{ox}), but it should be larger than the supply voltage (VDD) with a safety margin to avoid any unintentional triggering of the ESD protection device due to noise or voltage overshoot. The holding voltage V_h needs to be small to reduce the power dissipation in the ESD event. Of course, it must be larger than the supply voltage to prevent latchup. The snapback turn-on resistor R_{on} should be minimized to ensure the ESD device can sustain a very high current

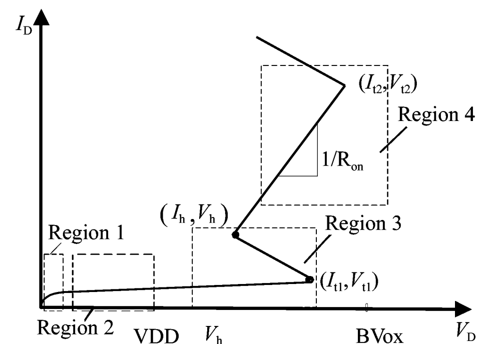

Fig. 1. I–V curve of an NMOS device.

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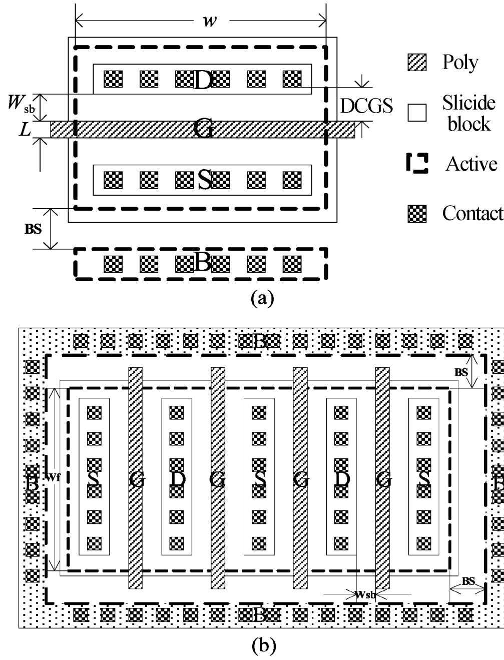


Fig. 2. (a) Layout of the single-finger GGNMOS device; (b) Layout of the multi-finger GGNMOS device.

capability and to prevent thermal breakdown. From Eq. (2), the secondary breakdown current I_{t2} is related to the ESD robustness, so it needs to be large to improve the ESD protection level. For multi-finger GGNMOS devices, the secondary breakdown voltage V_{t2} must be designed as larger than V_{t1} to improve the ability of uniform turn-on.

In this paper, a lot of CMOS devices with different device dimensions and layout floorplans have been drawn and fabricated to find the relationships between snapback parameters and layout parameters of GGNMOS devices in 0.13-μm silicide CMOS technology. The snapback characteristic of GGNMOS devices is investigated by using the TLP technique. The relationships between snapback parameters and layout parameters of GGNMOS devices are analyzed in detail. These relationships can help the circuit designer predict the behavior of GGNMOS devices under high ESD current stress, and design area-efficient ESD protection circuits to sustain the required ESD level[3, 5]. Optimized layout rules for ESD protection in 0.13-μm silicide CMOS technology are also presented.

2. Test structure of the GGNMOS device

Lots of GGNMOS devices with different layout parameters have been drawn and fabricated in a standard silicide 0.13-μm CMOS technology in this investigation. All these devices are fabricated with a silicide-blocking layer to block silicide diffusion on the drain and source region. The silicide is only formed under the contact of drain and source terminals.

The main layout parameters which affect the ESD robustness of GGNMOS devices are channel length (L), channel width (W), the spacing from drain contact to poly-gate edge (DCGS), silicide block layer width (W_{sb}) and the spacing from source contact to substrate diffusion (BS) as shown in Fig. 2(a). To sustain the required ESD protection level, a large

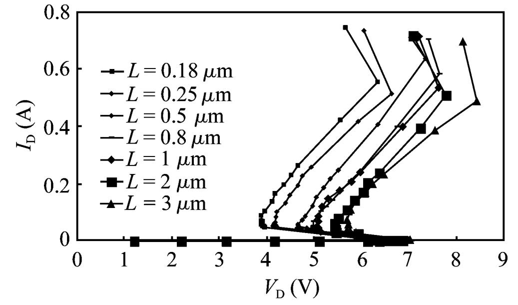


Fig. 3. TLP measurement data of GGNMOS devices with different channel lengths.

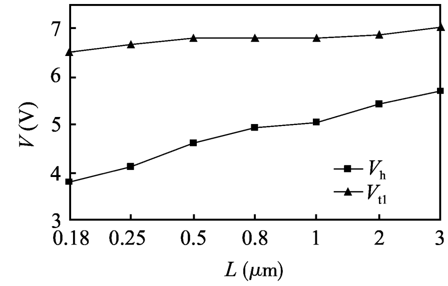


Fig. 4. V_h and V_{t1} as functions of the channel length of the GGNMOS devices.

GGNMOS device could be designed using multiple fingers to reduce the total layout area and the non-uniform turn-on effect, as shown in Fig. 2(b). The channel length (L), unit-finger width (W_f), the silicide block layer width (W_{sb}), the spacing from source contact to substrate diffusion (BS), and the finger number (M) are 0.5 μm, 50 μm, 2 μm, 2 μm, and 4, respectively.

3. TLP test results and analysis

The TLP technique is widely used to measure the snapback behavior of GGNMOS during high ESD stress. In this paper, the rise time and the pulse width of the TLP pulses are 10 ns and 100 ns, respectively. These TLP measured results will be shown and analyzed in the following sections.

3.1. Channel length (L) of single finger GGNMOS

The TLP measurement data of GGNMOS devices with different channel lengths are shown in Fig. 3. The layout floorplan and other layout parameters are kept the same, (W = 50 μm, W_{sb} = 2 μm, DCGS = 2.5 μm, BS = 2 μm). Figure. 4 illustrates the holding voltage V_h and the snapback voltage V_{t1} as functions of the channel length of the GGNMOS devices. According to these results, the holding voltage V_h is proportional to the channel length. The increment of snapback voltage V_{t1} is small when the channel length increases[6].

As shown in Fig. 5, the second breakdown current I_{t2} drops a little when the channel length is varied from 0.18 to 0.25 μm. When the channel length is larger than 0.5 μm, the I_{t2} value of the GGNMOS device is decreased as channel length increases.

The turn-on resistance R_{on} of the GGNMOS device can be extracted from the TLP characteristics after snapback has

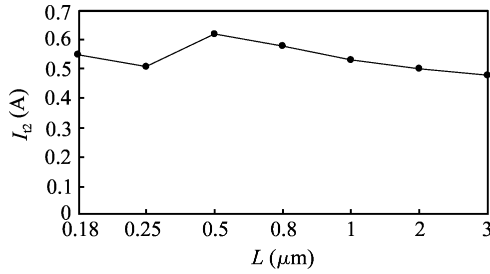


Fig. 5. Dependence of I_{t2} on channel length of the GGNMOS devices.

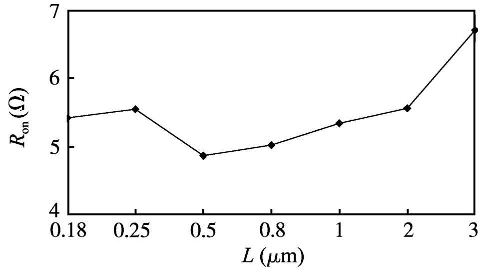


Fig. 6. R_{on} of the GGNMOS device is extracted from the TLP characteristics after snapback has occurred.

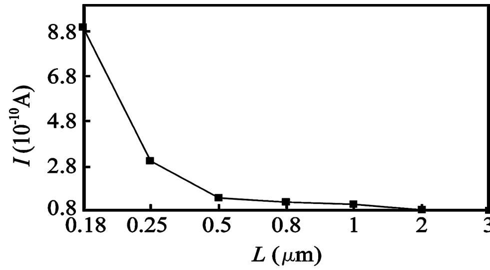


Fig. 7. Leakage current of GGNMOS devices with different channel lengths.

occurred, as shown in Fig. 6. From these results, R_{on} is slightly reduced from 5.42 to 4.87 Ω for a channel length between 0.18 and 0.5 μm. When the channel length is increased from 0.8 to 3 μm, the turn-on resistance of the GGNMOS device is improved from 5.03 to 6.7 Ω.

From the experimental results of I_{t2} value and R_{on}, the shortest channel length GGNMOS device should give better ESD performance. But as shown in Fig. 7, the leakage current across the GGNMOS devices increases with shorter channel length. So, the best choice is not to use the shortest channel length, but instead adopt a device with a larger channel length. Therefore, in light of the influence of R_{on} and I_{t2}, the optimum channel length for the best ESD performance is about 0.5 μm in this 0.13-μm silicide CMOS technology.

3.2. Channel width (W) of single finger GGNMOS

According to the TLP data shown in Fig. 8, the single finger GGNMOS shows an obvious width dependence of I_{t2}. In Fig. 8, the I_{t2} value of the GGNMOS device increases when the device channel width increases. We redraw the relationship between channel width and I_{t2} when I_{t2} is measured in mA/μm, as shown in Fig. 9. When channel width increases, although the I_{t2} value of the GGNMOS device is increased, the current sustainable ability per channel width of the GGNMOS device is decreased. This is due to the non-uniform turn-on effect among the long channel width of large-dimension devices[7, 8]. According to the data of Fig. 8, for single finger GGNMOS, if the finger width W_f is larger than W_{max} = 50 μm, the non-uniform turn-on effect will be obvious. So, in order to reduce the non-uniform turn-on effect, more fingers are drawn and connected in parallel to form large-dimension GGNMOS devices.

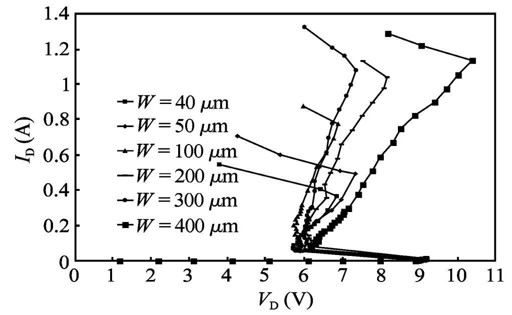


Fig. 8. TLP measurement data of single finger GGNMOS devices with different channel widths (W = 40, 50, 100, 200, 300, 400 μm; L = 0.5 μm; W_{sb} = 2 μm; BS = 2 μm).

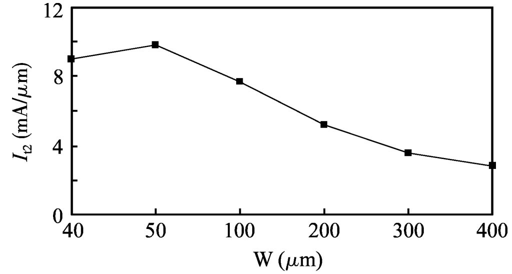


Fig. 9. Dependence of I_{t2} on the channel width.

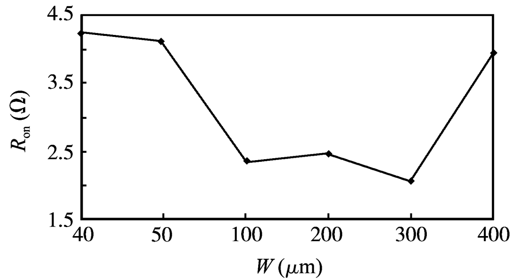


Fig. 10. Influence of R_{on} on the channel width.

The turn-on resistances of single finger GGNMOS devices with different channel widths, but with otherwise the same layout parameters, are shown in Fig. 10. The turn-on resistance of the GGNMOS device with a channel width of 50 μm (R_{50}) is 4.11 Ω. If the GGNMOS device with long channel width can be uniformly turned on, the formula $R_{on-long} = R_{50}/(W/50)$ should stand[3]. But from the data of Fig. 10, the experimental result of turn-on resistance R_{on} is far from the ideal resistance. Furthermore, the turn-on resistance R_{400} of the GGNMOS device with 400 μm channel width increases to 3.95 Ω. This implies that GGNMOS devices with longer channel width cannot be uniformly turned on during ESD stress.

3.3. Spacing from drain contact to poly-gate edge (DCGS) and the silicide block layer width

As shown in Fig. 2, the spacing from the drain contact to

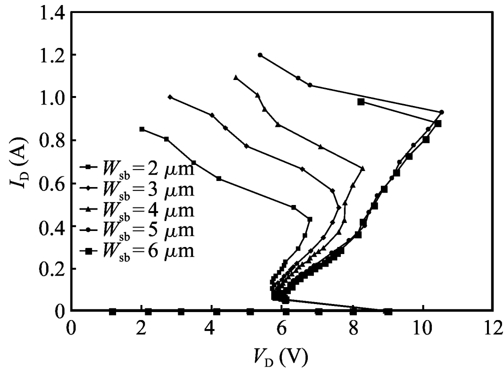


Fig. 11. TLP measurement data of single finger GGNMOS devices with different silicide block widths (W_{sb} = 2, 3, 4, 5, 6 μm; W = 50 μm, L = 0.5 μm, BS = 2 μm).

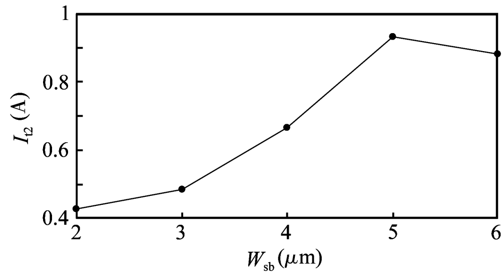


Fig. 12. Dependence of I_{t2} on W_{sb}.

poly-gate edge (DCGS) is equal to the spacing of SAB to contact plus the silicided block layer width (W_{sb}). So, increasing the W_{sb} parameter is equal to increasing the DCGS parameter.

According to the TLP data shown in Fig. 11, the variation of V_h and V_{t1} is not obvious when the W_{sb} parameters vary from 2 to 6 μm. As shown in Fig. 12, the increase in W_{sb} improves the I_{t2} value of GGNMOS devices. However, when the variation of the W_{sb} parameter reaches a certain level, the increment of I_{t2} eases off.

Figure 13 shows the turn-on resistance of GGNMOS devices with different W_{sb} parameters. From these results, when the W_{sb} parameter increases from 2 to 5 μm, the GGNMOS device with a larger W_{sb} parameter has a larger turn-on resistance. The increase of turn-on resistance leads to an increase in V_{t2} to greater than V_{t1}. Like to I_{t2}, the turn-on resistances of GGNMOS devices with W_{sb} parameter of 5 μm, 6 μm are nearly the same, as shown in Fig. 13.

3.4. Spacing from the source-active to the substrate diffusion (BS) of single finger GGNMOS

The spacing from the source-active to the substrate diffusion has been illustrated in Fig. 2 and marked as "BS". The layout floorplan and all other layout parameters are kept as the same (W = 50 μm, L = 0.5 μm, W_{sb} = 2 μm), and only the BS parameters are varied from 1 to 5 μm. As shown in Fig. 14, the I_{t2} value and turn-on resistance are nearly the same. So, an improvement of ESD capability is not obvious when BS increases from 1 to 5 μm. Further increasing the BS parameter will probably improve the snapback characteristic of the GGNMOS device, but it also will greatly increase the probability of the latch-up effect occurring in the I/O circuits.

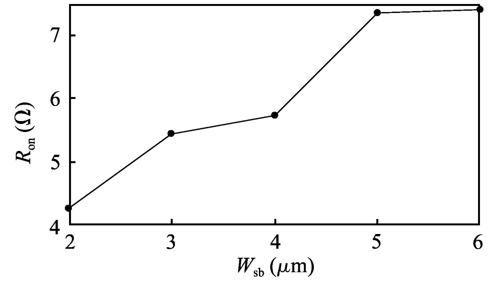


Fig. 13. R_{on} dependence of the silicided block layer width (W_{sb}).

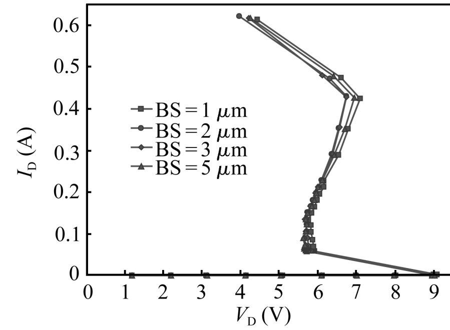


Fig. 14. TLP measurement data of single finger GGNMOS devices with different BS spacings (W = 50 μm, L = 0.5 μm, W_{sb} = 2 μm).

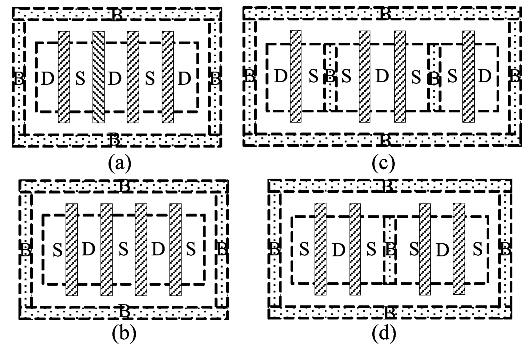


Fig. 15. Layout floorplans of the multi-finger GGNMOS devices.

3.5. Multi-finger NMOS layout floorplan

To study the non-uniform turn-on effect of multi-finger GGNMOS devices, four layout floorplans of multi-finger GGNMOS have been drawn in Fig. 15[8, 9]. Each multi-finger GGNMOS device has four parallel fingers, and every finger is drawn with a unit-finger width of 50 μm. The total channel widths of these multi-finger GGNMOS devices are 200 μm, and the other layout parameters are kept the same (L = 0.5 μm, W_{sb} = 2 μm, BS = 2 μm). In Figs. 15(a) and 15(b), typical layout structures of a multi-finger MOSFET without any additional pick-up guard ring inserted into the source region are seen. The difference between the layouts of Figs. 15(a) and 15(b) is the layout floorplan of the source and drain. In Fig. 15(c), there are two additional pick-ups inserted into the central source region, while in Fig. 15(d), there is one additional pick-up inserted into the central source region.

The TLP measurement data of multi-finger GGNMOS devices with different layout floorplans are shown in Fig. 16. From these results, the variation of the layout floorplan of multi-finger GGNMOS devices cannot reduce the gap between V_{t2} and V_{t1}. The turn-on resistance R_{on} and I_{t2} values of these

Table 1. Dependence of HBM level with different layout floorplans.

Layout floorplan	Total width (μm)	Unit-finger width (μm)	Layout area (μm^2)	R_{on} (Ω)	I_{t2} (A)
BDGSGDGSGDB	200	50	1415	1.35	1.26
BSGDGSGDGSB	200	50	1221	1.77	1.30
BDGSBSGDGSBSGDB	200	50	1765	1.87	1.26
BSGDGSBSGDGSB	200	50	1418	1.34	1.48

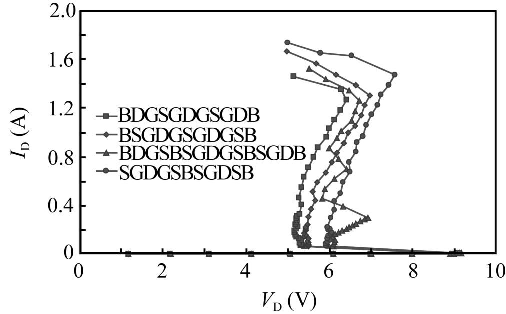


Fig.16. TLP measurement data of multi-finger GGNMOS devices with different layout floorplans.

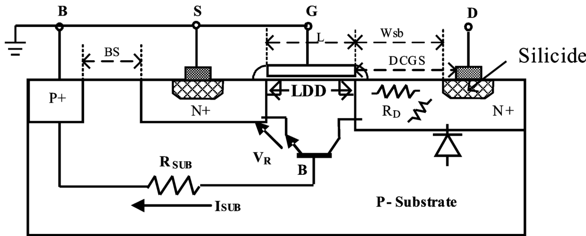
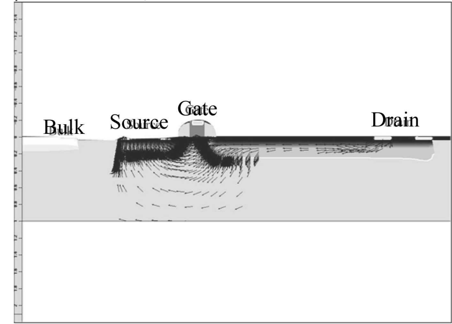


Fig. 17. Cross section for a GGNMOS device showing the currents in the parasitic LNPN bipolar transistor.

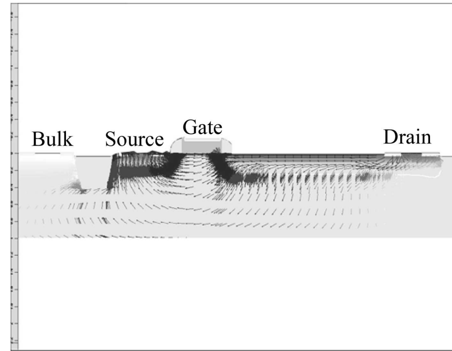
devices are listed and compared in Table 1. According to the data of Table 1, the BSGDGSBSGDGSB layout floorplan has the smallest turn-on resistance R_{on} and the maximum I_{t2}. So, this device can achieve the best HBM ESD capability. As illustrated in Fig. 16, several snapback phenomena have occurred in the BDGSBSGDSBSGDB layout floorplan. The calculation of the turn-on resistance R_{on} for this device is based on the last snapback curve.

4. Discussions

A cross-section of a GGNMOS device is shown in Fig. 17. As a positive ESD stress appears at drain, the DB junction is reverse-biased all the way to its breakdown. Avalanche multiplication takes place and generates electron–hole pairs. Hole current I_{SUB} flows into the ground via substrate and builds up a potential across the lateral parasitic substrate resistance R_{SUB}, the voltage drop across R_{SUB} raises the local substrate potential V_R. As V_R increases, the BS junction turns on, eventually triggering the parasitic LNPN bipolar device. For the parasitic bipolar device, the drain terminal of the GGNMOS device acts as the collector, the source terminal acts as the emitter, and the P-substrate terminal acts as the base. Since a high electrical field is no longer needed to maintain the current level through impact ionization alone, the drain voltage decreases and snapback happens.



(a)



(b)

Fig.18. TCAD simulation results of current distribution for the GGNMOS with different channel lengths: (a) $L = 0.18$ μm; (b) $L = 0.5$ μm.

4.1. Influence of the channel length

As shown in the cross section shown in Fig. 17, the channel length is seen as the equivalent base width of the parasitic lateral NPN bipolar transistor. As channel length decreases, the current gain β of the parasitic bipolar transistor is improved, and then the discharge capability of the ESD current is improved. However, this trend is only suitable for larger scale non-silicide CMOS technology[1, 2]. As illustrated in Fig. 4, the V_h value is proportional to channel length. Lower V_h values imply lower power dissipation in the GGNMOS device under ESD stress. The V_{t1} value slightly increases as the channel length increases.

For the I_{t2} value, it has always been assumed that the minimum channel length device shows the highest I_{t2} value in non-silicide CMOS technology[10]. But in this 0.13-μm silicide CMOS technology, the I_{t2} value is degraded with channel length, as shown in Fig. 5. To explain this phenomenon, a TCAD device simulator (MEDICI) has been used. The DC device simulation has been based on a 0.13-μm silicide CMOS technology with a channel width of 50 μm. The layout parameters are kept the same (W_{sb} = 2 μm, BS = 2 μm) except channel length. DC simulation was performed for drain voltages from 0 to 10 V. Figure18 shows the simulation results of

current distribution for the GGNMOS with different channel lengths (L = 0.18 μm, L = 0.5 μm). From these simulation results, when the channel length is equal to 0.18 μm, the great mass of the ESD current flows along the channel surface under gate oxide. Only a small current flows through the substrate. The turn-on region in the parasitic bipolar transistor is focused on the side of the drain diffusion. When the channel length is equal to 0.5 μm, besides the ESD current flowing along the channel surface, there is a lot of ESD current flowing through the substrate. The turn-on region in the parasitic bipolar transistor will be moved from the side of the drain diffusion to the bottom of the drain diffusion in the GGNMOS device structure. This means that this GGNMOS device can sustain higher ESD discharge currents.

For GGNMOS devices with LDD structure, the turn-on resistance is defined as the sum of the two terms: one is the parasitic series resistor of the drain and source terminal, and another is the dynamic turn-on resistance of the parasitic bipolar device. The dynamic turn-on resistance of the parasitic bipolar device plays a major role. When the channel length varies from 0.18 to 0.5 μm, the turn-on area of the parasitic bipolar transistor will increase, and then the dynamic turn-on resistance will decrease. Therefore, the turn-on resistance will decrease as the channel length increases from 0.18 to 0.5 μm.

4.2. Influence of the channel width

As discussed above, the non-uniform current distribution effect occurs in the GGNMOS device with large channel width. As mentioned in previous work[7], the single finger GGNMOS device can be seen as lots of small parasitic bipolar segments connected in parallel. For low channel widths, the turn-on of the parasitic bipolar segments is nearly simultaneous. Therefore, an increase in channel width can improve the current sustainable ability per channel width of the GGNMOS device. But if the channel width is larger than $W_{\max}$ = 50 μm, some bipolar segments turn on early, and cause damage before the other bipolar segments turn on. So, the non-uniform current distribution will be obvious.

4.3. Influence of the silicide-blocking layer width

In previous research[3], the ESD current discharge capability of the silicide-blocking GGNMOS device is higher than that of the silicide GGNMOS device. The reason for this phenomenon is that the high resistance of the silicide-blocking layer leads to a large distribution resistor along the drain diffusion region, as shown in Fig. 15. This resistor can be seen as the ballast resistance series with drain terminal. The advantage of this series ballast resistance is limiting the ESD discharge current in a GGNMOS device to achieve better ESD protection performance. During the ESD event, a large current flows along the surface of channel. This current will generate a hot point at the LDD structure. The ESD current limit can avoid early heat breakdown at the LDD structure of the GGNMOS device.

As $W_{\rm sb}$ increases, the series ballast resistance at the drain terminal will increase. The GGNMOS device with larger $W_{\rm sb}$ will have a larger ballast resistance serried with the drain terminal, while the p–n junction at the bottom of drain diffusion has a smaller sheet resistance. Therefore, more ESD discharge current will flow through the bottom of drain diffusion to the substrate. TCAD simulation results illustrate this phenomenon in Fig. 19. But too large a $W_{\rm sb}$ will lead to a larger voltage drop in the drain diffusion region. This voltage will cause breakdown of the p–n junction underneath the contact of the drain terminal. This could explain the reason why the value of $I_{\rm t2}$ varies little for a GGNMOS device with $W_{\rm sb}$ = 5 μm, 6 μm, as shown in Fig. 12. Besides this, the increase of $W_{\rm sb}$ will increase the layout area consumption of the GGNMOS device. Considering the trade-off between layout area consumption and ESD performance, the optimized value of 5 μm will be chosen for the GGNMOS device in this 0.13-μm silicide CMOS technology.

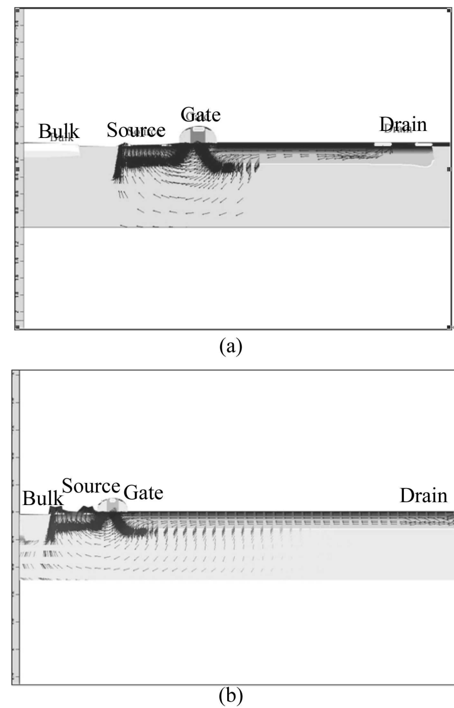


Fig.19. TCAD simulation results of current distribution for a GGNMOS with different $W_{\rm sb}$ parameters: (a) $W_{\rm sb}$ = 2 μm; (b) $W_{\rm sb}$ = 5 μm.

4.4. Influence of the multi-finger GGNMOS layout floorplan

As is well known, the non-uniform turn-on effect often reduces the ESD protection performance, even if the GGNMOS device has a large enough layout dimension. Figure 20 shows a layout view and cross-section view of GGNMOS devices with different layout floorplans. From these cross-section views, there are four parasitic bipolar transistors in four multi-finger GGNMOS devices. As shown in Fig. 17, the channel region of the GGNMOS device acts as the base of the parasitic bipolar. There is the parasitic substrate resistance under the channel region in the substrate. This parasitic resistance acts as the input base resistance of an individual parasitic bipolar, which determines the turn-on of the parasitic bipolar.

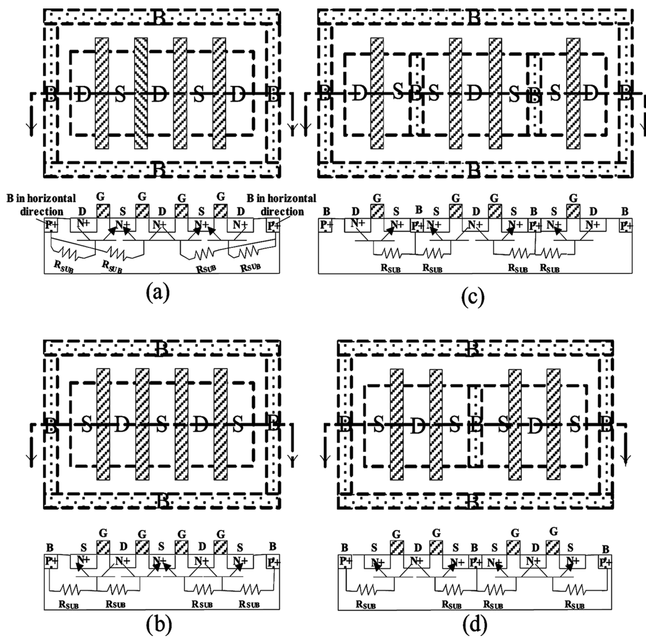


Fig. 20. (a) Layout view and cross section view of a GGNMOS device with layout floorplan of BDGSGDGSGDB; (b) Layout view and cross section view of a GGNMOS device with layout floorplan of BSGDGSGDGSB; (c) Layout view and cross section view of a GGNMOS device with layout floorplan of BDGSBSGDGSBSGDB; (d) Layout view and cross section view of a GGNMOS device with layout floorplan of BSGDGSBSGDGSB.

For different layout floorplans, the parasitic substrate resistance of each parasitic bipolar is different. The central fingers with larger parasitic substrate resistance will turn on earlier than the other fingers of the GGNMOS device. The more fingers of the GGNMOS device that are triggered on, the smaller the value of turn-on resistance R_{on} is. So, the value of turn-on resistance R_{on} indicates the turn-on ability of the multi-finger GGNMOS device.

For the BDGSGDGSGDB layout floorplan, the parasitic substrate resistance connects with the pick-ups in the horizontal direction. This is the greatest difference between this layout floorplan and the other layout floorplan. This substrate resistance is determined by the channel width. So, the turn-on resistance R_{on} of this layout plan is medium value in these layout floorplans.

For the BSGDGSGDGSB layout floorplan, the distance between the central channel region and pick-up is longer than the device discussed above. Two central fingers in this device are turned on first. Therefore the turn-on resistance of this device is larger than the first layout floorplan device.

For the BDGSBSGDGSBSGDB layout floorplan, the experiment results are quite different from the previous research in Ref. [11], and three snapback phenomena are found in the experiment results, as illustrated in Fig. 16. It is believed that the non-uniform effect would occur along the channel width direction.

For the BSGDGSBSGDGSB layout floorplan, from the experiment results, it has the smallest turn-on resistance and the maximum I_{t2}. So, if the layout area is not the critical parameter, the BSGDGSBSGDGSB layout floorplan is recommended in this 0.13-μm silicide CMOS technology.

5. Conclusion

In this paper, lots of GGNMOS devices with different layout parameters and different layout floorplans are drawn and fabricated in the 0.13-μm silicide CMOS process. From these experiment results and analysis, the influence of layout parameters and layout floorplans on the snapback characteristic for GGNMOS devices has been discussed in detail. The conclusions are listed as follows:

(1). As channel length increases, V_h will linearly increase, while the dependence of V_{t1} value on channel length is rather weak. In light of the influence of R_{on} and I_{t2} value, the optimum channel length for the best ESD performance is about 0.5 μm in this 0.13-μm silicide CMOS technology.

(2). For a single finger GGNMOS device, when channel width increases, although the I_{t2} value of the GGNMOS device is increased, the current sustainable ability per channel width of the GGNMOS device is decreased. So, if the finger width W_f is larger than W_{max} = 50 μm, more fingers are drawn and connected in parallel to form large-dimension GGNMOS devices.

(3). The silicide-blocking GGNMOS device has a much higher ESD robustness. Increasing the W_{sb} parameter will improve the value of I_{t2} and the turn-on resistance R_{on}, but too large a W_{sb} will lead to early ESD failure. Considering the trade-off between layout area consumption and ESD performance, an optimized value of 5 μm will be chosen for the GGNMOS device in this 0.13-μm silicide CMOS technology.

(4). When BS parameters vary from 1 to 5 μm in this 0.13-μm silicide CMOS technology, the ESD capability of GGNMOS devices is not obviously improved. A minimum layout spacing should be kept to avoid latch-up occurring.

(5). Different layout floorplans of multi-finger GGNMOS device are drawn and discussed. Compared to the other layout floorplans, the BSGDGSBSGDGSB layout floorplan can achieve the best ESD protection ability in this 0.13-μm silicide CMOS technology.

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