# A wafer-level 3D packaging structure with Benzocyclobutene as a dielectric for multichip module fabrication

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**Abstract:** A new wafer-level 3D packaging structure with Benzocyclobutene (BCB) as interlayer dielectrics (ILDs) for multichip module fabrication is proposed for application in the Ku-band wave. The packaging structure consists of two layers of BCB films and three layers of metallized films, in which the monolithic microwave IC (MMIC), thin film resistors, striplines and microstrip lines are integrated. Wet etched cavities fabricated on the silicon substrate are used for mounting active and passive components. BCB layers cover the components and serve as ILDs for interconnections. Gold bumps are used as electric interconnections between different layers, which eliminates the need to prepare vias by costly dry etching and deposition processes. In order to get high-quality BCB films for the subsequent chemical mechanical planarization (CMP) and multilayer metallization processes, the BCB curing profile is optimized and the roughness of the BCB film after the CMP process is kept lower than 10 nm. The thermal, mechanical and electrical properties of the packaging structure are investigated. The thermal resistance can be controlled below 2 °C/W. The average shear strength of the gold bumps on the BCB surface is around 70 N/mm$^2$. The performances of MMIC and interconnection structure at high frequencies are optimized and tested. The *S*-parameters curves of the packaged MMIC shift slightly showing perfect transmission character. The insertion loss change after the packaging process is less than 1 dB range at the operating frequency and the return loss is less than –8 dB from 10 to 15 GHz.

**Key words:** wafer-level; benzocyclobutene; embedded MMIC and passives; RF application

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## 1. Introduction

Along with the development of current electronic packages becoming multifunctional, high density and miniature, packaging technology has evolved from dual-in-line technology, surface mount technology and ball grid arrays to 3D multichip modules (MCM). 3D MCM packages promise to reduce interconnect delays by reducing interconnect length, which results in a reduction of interconnect associated parasitic capacitance and inductance. The vertical interconnection technology adopted in the 3D package is smaller and lighter. These advantages meet with the needs of radio frequency (RF) applications which must address specific requirements, such as low loss and low parasitic interconnections. RF devices remain costly due to the high cost of fabrication and packaging processes. MMIC interconnections often require high-precision machining due to the small wavelengths involved. Wire bonding is a common technology used for interconnection, but it has the disadvantage of high electrical signal loss. Thus, a low-cost compact reliable technique for integrating ICs with RF devices is of great interest.

For the application of MCM in high frequency ranges, the properties of the interlayer dielectric material are important for packaging performance. BCB is selected as the dielectric material for its low dielectric constant (2.65), low dissipation factor (0.0008) and low curing temperature (250 °C). These characteristics are effective for high-frequency systems. The technology of utilizing BCB as an ILD has already been realized in the multilayer MCM package structure in some examples in the literature[1–4]. In these works, an MCM packaging structure was achieved by using via dry etching in BCB to realize interconnection and, due to the high cost of dry etching and the development of the BCB material, photosensitive BCB was extensively used in the high frequency MCM package. However, in these cases the vertical interconnection between layers was achieved by sputtering and electroplating. Such processes are simple but can not meet the requirements of a high aspect ratio via (HARVi). As the aspect ratio of a standard photosensitive BCB via is in the range of 1 : 4, a large via is needed when the BCB thickness increases above 10 $\mu$m[5]. As a result, different techniques have been proposed for HARVis in polymers. One approach is to use gold bump plating followed by BCB film coating. But this way can only be implemented on the pads of the substrate instead of the dies because of the electroplating process. Furthermore, a very thin die (< 30 $\mu$m) is needed to match the height of the metal stud of HARVi[6,7]. Another approach is to prefabricate gold stud bumps on the substrate with a wire-bonding

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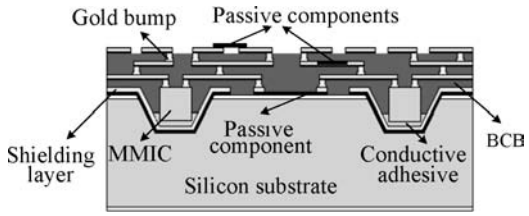



Fig. 1. Diagrammatic sketch of the packaging structure.

machine, similar to our previous work[8]. However, this approach is not compatible with wafer-level package technology.

In this paper, a novel wafer-level MCM packaging technology is proposed, as shown in Fig. 1. Gold bumps and spun-on BCB films are used as HARVis and ILDs, which eliminates the need for dry etching. The fabrication process was as follows: first, the micro-machined cavities were formed on silicon substrate. Next, the MMICs were embedded in these recessed cavities. After that, gold stud bumps were planted as multi-layer vertical interconnections and BCB films covered the multichip modules as ILDs. Because of the cavities, the BCB has to be thick enough to planarize the slots around the chips and at the same time reduce the capacitive coupling between the two layers sufficiently as well.

The wafer-level MCM mentioned above proposes a new concept for integrating active and passive devices on BCB film with chips embedded in silicon substrate for Ku-band wave applications. This MCM packaging structure consists of two layers of BCB films and three layers of metallized films, in which the MMIC, thin film resistors, striplines and microstrip lines are integrated. In the following sections, the performances of MMIC transmission lines will be tested and the influence of the package on the circuit at high working frequencies will be optimized.

## 2. Packaging process

The flow chart of the project is shown in Fig. 2. First of all, according to the application requirements, the design proposal is presented. This step contains the design of the substrate, interconnection and embedded components. The following step is to finish the process flow and test the performance of the finished packaging structure. The detailed process will be discussed in subsequent sections.

### 2.1. Preparation of silicon substrate

A basic photolithographic process and anisotropic etching in 50 °C, 40 wt% potassium hydroxide (KOH) were used to form the cavities on the silicon substrate for the embedded chip. The silicon etching rate was approximately 10 $\mu$m/h. According to the chip thickness and allowing for the silver epoxy which was used to attach the chip, the etching depth of the silicon substrate was set at 110 $\mu$m, as shown in Fig. 3(a). A 500 Å TiW layer was sputtered on the silicon to improve adhesion. Then a 1000 Å gold layer was sputtered as a seed layer. The contact pads and ground plane were patterned by another photolithographic process and then electroplated to 3 $\mu$m, as shown in Fig. 3(b). Finally the remaining seed layer was removed by ion beam etching.

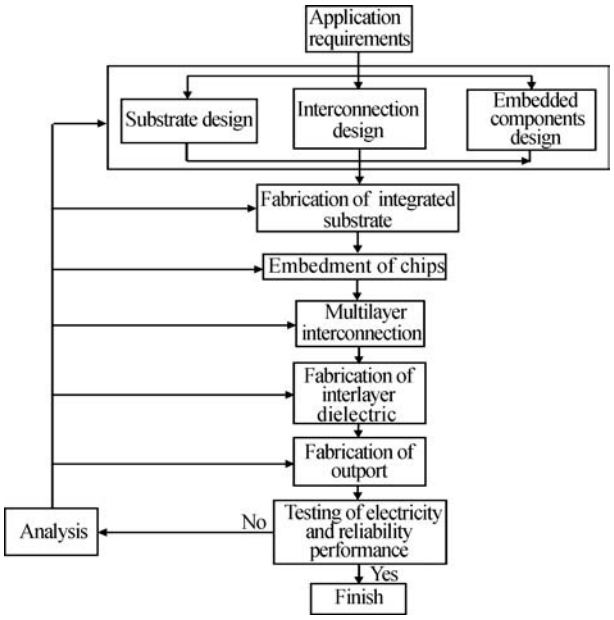



Fig. 2. Flow chart of the packaging process.

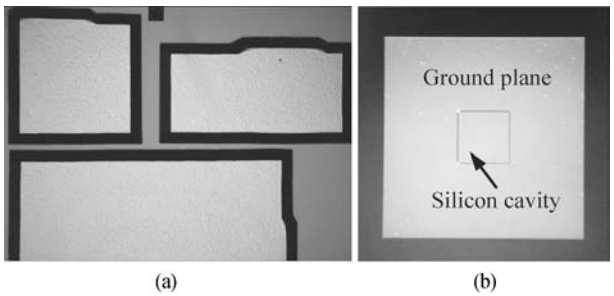



Fig. 3. Planform of silicon substrate: (a) After KOH etching; (b) With ground plane.

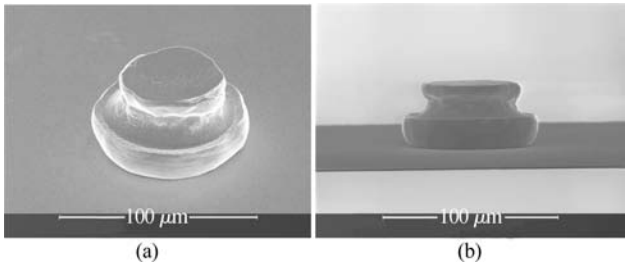



Fig. 4. Pressed gold bump: (a) Top view; (b) Lateral view.

### 2.2. Bump fabrication

The interlayer interconnection was through gold bumps followed by dielectric film covering. The gold bumps were formed by a wire-bonding machine on the contact pads. The tail filaments were pressed to a column by a special capillary at a height of 25 $\mu$m and 80 $\mu$m in diameter, as shown in Fig. 4.

### 2.3. Coating and solidification of BCB film

The BCB coating process includes surface preparation, spin-coating, baking, and thermal curing. The thin film BCB layer ($\leqslant$ 10 $\mu$m) is easy to fabricate. But once the BCB thickness exceeds 20 $\mu$m, BCB solidification and surface treatment

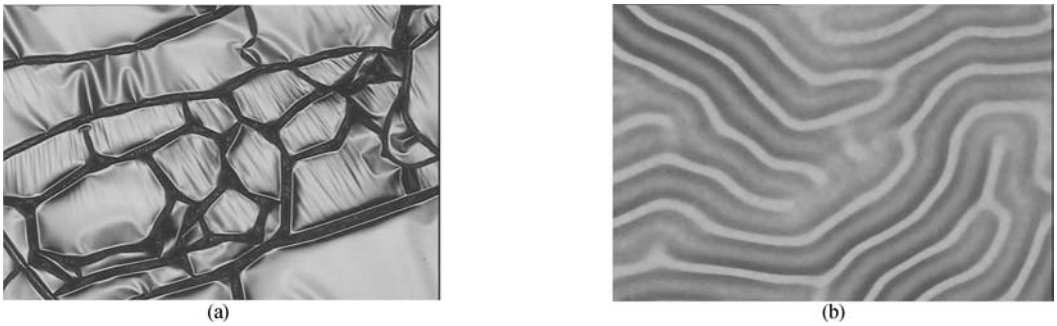



Fig. 5. 30 $\mu$m thick BCB layer: (a) Cracked surface; (b) Wrinkled surface.

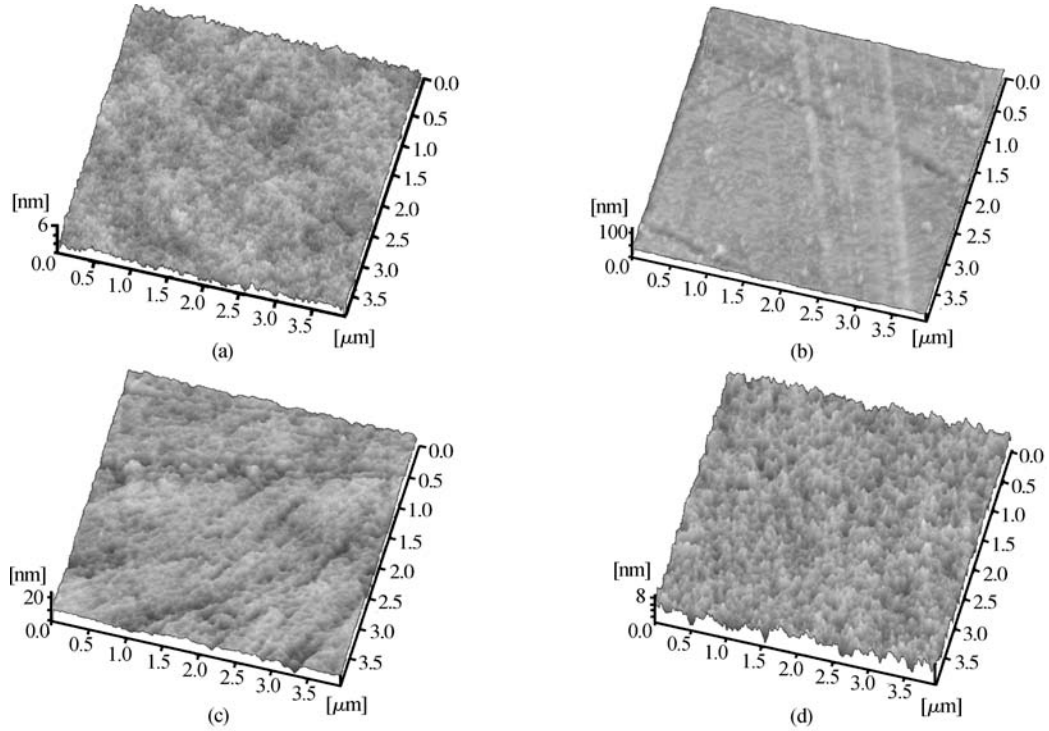



Fig. 6. Roughness of BCB surface: (a) Standard cure without CMP $R_z$ = 5.89 nm; (b) $T_C$ = 205 °C , $t_C$ = 40 min, $R_z$ = 65.71 nm; (c) $T_C$ = 205 °C , $t_C$ = 60 min, $R_z$ = 12.39 nm; (d) $T_C$ = 205 °C , $t_C$ = 80 min, $R_z$ = 8.60 nm.

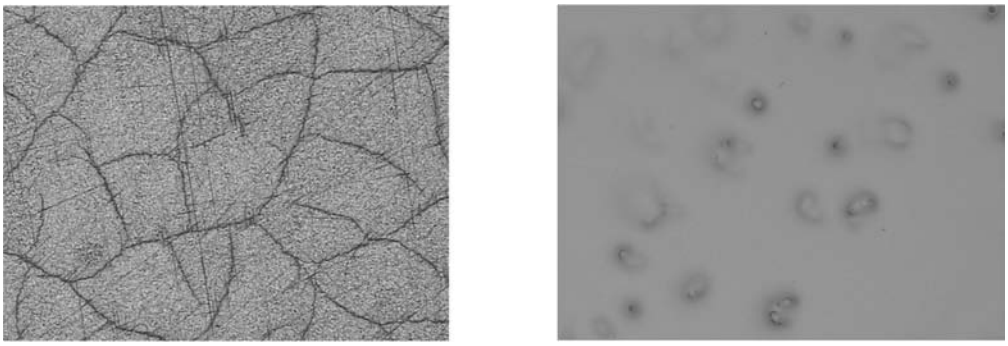
becomes difficult, especially in the multilayer BCB coating process. There are two main problems to confront. Firstly, if the cure temperature is too high, a large number of cracks will be generated on the BCB surface ($\geqslant$ 20 $\mu$m), as shown in Fig. 5(a). Secondly, if the soft bake process is performed on a hotplate, the rapid temperature change will lead to a large number of wrinkles on the BCB surface, as shown in Fig. 5(b).

The first BCB layer was spun at 1000 rpm for 20 s and a thickness of about 30 $\mu$m BCB was achieved. To drive out any residual solvent, the wafer was soft baked in an oven for 20 min at 100 °C after the spin-on process. The cure process was performed on an enclosed hotplate with flowing nitrogen to avoid oxidation. The last step was a hard cure for 60 min, slowly ramping up to 200 °C in a nitrogen atmosphere. With this routine, an 80% conversion was achieved. This partially cured BCB has enough unreacted bonds on the surface for enhanced metal-to-BCB adhesion. After the final metal deposition, the entire multilevel structure was full cured at 250 °C for 60 min. Due to the high coefficient of thermal expansion (CTE) of BCB, special care is necessary to achieve good adhesion to the gold coated silicon substrate.

### 2.4. CMP of BCB film

In order to remove the top coating of BCB film and achieve a wafer-level package (WLP), precise chemical mechanical planarization (CMP) technology is employed. Atomic force microscopy (AFM) and ellipsometry of BCB films before and after the CMP process show that a higher down pressure and speed during the polishing process will lead to a higher removal rate at the expense of higher surface roughness, non-uniformity and scratch density. As the cure temperature of BCB increases beyond 200 °C, the CMP removal rate decreases drastically.

The quality of the cured BCB film will influence the BCB removal rate and surface quality. The typical suggested temperature-time profile for BCB cure is 250 °C, 1 h in a box oven or furnace. The roughness of the BCB surface can reach 5.89 nm measured by AFM, as shown in Fig. 6(a). In the subsequent experiment, it is found that the standard BCB cure process (250 °C, 1 h) is not appropriate for the multilayer



(a) (b)

Fig. 7. BCB surface after the CMP process: (a) Scratched surface; (b) Defective surface.

metallization and CMP processes, so the BCB cure condition should be optimized.

In order to increase the quality of the BCB film, several ways are introduced to optimize the BCB cure profile for the following CMP step. The general solution is to change the cure time and the cure temperature. On the one hand, if the cure time goes beyond that needed, the BCB film will become too hard to remove, leading to a large number of scratches after the CMP process, as shown in Fig. 7(a). On the other hand, if the cure time is not long enough, the solvent in BCB will not be removed completely and the BCB film will have a defective surface after CMP process, as shown in Fig. 7(b).

Three kinds of cure profiles are tested to find the optimized one. For the cure temperature ($T_C$), because the BCB film is less likely to generate cracks after the cure process at 205 °C, $T_C$ is fixed at this temperature. For the cure time, the three times tested are 40, 60 and 80 min respectively. The results of BCB roughness after the CMP process measured by AFM are shown in Fig. 6.

According to the AFM results, it can be seen that the longest cure time leads to the minimum roughness, so the cure parameters are set at $T_C$ = 205 °C, $t_C$ = 80 min. Operating under this cure profile can achieve high quality BCB film after the CMP process. The roughness of the BCB surface can reach 8.6 nm, which is suitable for the subsequent metallization process.

### 2.5. Multilayer BCB coating

The multilayer coating process strongly relies on the planarizing property of BCB. A good planar surface determines the quality of subsequent interconnection steps. The structure of three metallization layers and two BCB layers has been fabricated, as shown in Fig. 8. The light lines are gold metal lines and dark areas in between are the BCB layers. A metallized via can be seen in the center region of the bottom BCB layer. The thicknesses of the bottom and top BCB layers are 25 $\mu$m and 30 $\mu$m respectively.

### 2.6. Final interconnections and redistribution

One difficulty of this process is to improve the adhesion between the BCB and metal layers. The most commonly used techniques for improving the adhesion is surface treatment of the BCB film, such as $O_2$ plasma. Because the adhesion between the BCB and metal layers depends on their properties, one method to enhance adhesion is to optimize the thickness of the adhesion layer. Another method is to change the adhesion layer with different metals. Three kinds of metals could be used as a seed layer, TiW, Ti and Cr, and all of the adhesion layers are performed by magnetron sputtering. Three kinds of thickness, 200, 500 and 800 Å, are prepared for each kind of adhesion layer respectively. Before the seed layer is deposited, $O_2$ plasma is performed on the BCB surface to improve the adhesion between the seed layer and BCB film. Finally, gold is plated to achieve 3 $\mu$m thick photo-defined interconnections, as shown in Fig. 9.

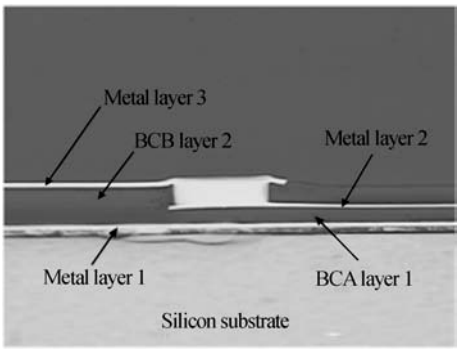



Fig. 8. Cross section of multilayer interconnection.

In order to test the adhesion of the 9 kinds of samples (as shown in Table 1), tape and wet etching tests are performed. The tape tests are done by sticking scotch tape to the metal and trying to peel the metal off the wafer. This is done on multiple parts of the wafer (from the edge to the center). The wet etching test is done in hot 40 wt% KOH for 3 h at 50 °C.

According to the test results shown in Table 1, the oxidized BCB surface has the best adhesion because Cr normally bonds with oxygen to form chromium oxide bonds. The adhesion between BCB and metal becomes weaker as the seed layer thickness increases. As a result, we choose 200 Å Cr film as the adhesion layer in the following experiments.

## 3. Measurements

### 3.1. Shear strength test

In order to investigate the mechanical reliability of the

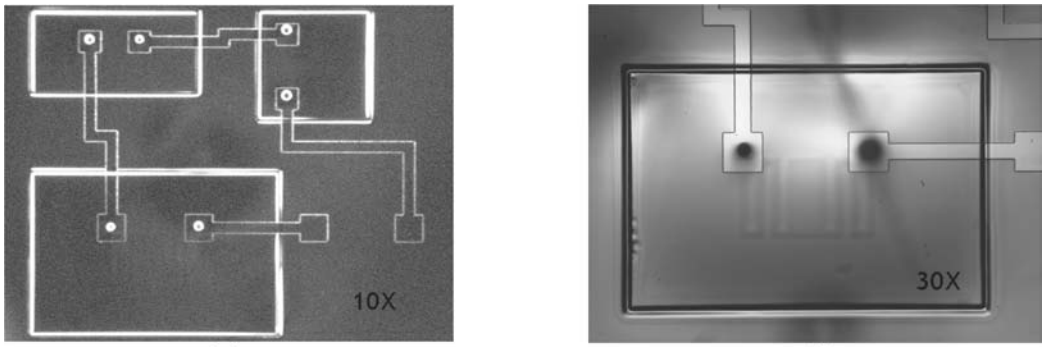



Fig. 9. Top metal line redistribution: (a) 10× zoom; (b) 30× zoom.

Table 1. Summary of adhesion layer experiments and test results.

| Sample | Seed layer | Adhesion layer (Å) | Au layer (Å) | Surface treatment | Tape test | Wet etching |
|---|---|---|---|---|---|---|
| 1 | TiW/Au | 200 | 1000 | $O_2$ plasma | pass | drop |
| 2 | TiW/Au | 500 | 1000 | $O_2$ plasma | fail | drop |
| 3 | TiW/Au | 800 | 1000 | $O_2$ plasma | fail | drop |
| 4 | Ti/Au | 200 | 1000 | $O_2$ plasma | pass | pass |
| 5 | Ti/Au | 500 | 1000 | $O_2$ plasma | pass | pass |
| 6 | Ti/Au | 800 | 1000 | $O_2$ plasma | fail | drop |
| 7 | Cr/Au | 200 | 1000 | $O_2$ plasma | pass | pass |
| 8 | Cr/Au | 500 | 1000 | $O_2$ plasma | pass | pass |
| 9 | Cr/Au | 800 | 1000 | $O_2$ plasma | pass | drop |

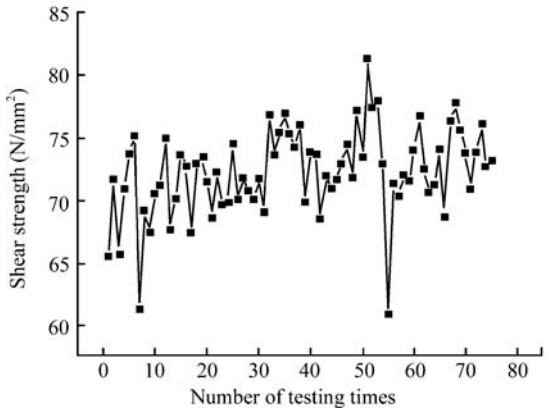



Fig. 10. Shear strength test of gold bumps.

packaging structure, the shear strength of the gold bumps on the BCB surface is tested. The test load is 100 g and the test speed is 100 $\mu$m/s. The average shear strength of eighty samples is about 71.9 N/mm$^2$, as shown in Fig. 10. The lower limit is 60 N/mm$^2$ which meets the requirement of reliability of gold bumps.

### 3.2. Thermal dissipation test

In order to evaluate the thermal dissipation behavior of this packaging structure, two types of thermal test chip are designed and fabricated in which thin resistance and diode are integrated for a thermal resistance test. The thermal resistance of this packaging structure can be controlled within 2 °C/W. The temperature of the power module (1.1 W) can be controlled below 80 °C with a heat sink. The detailed test structure was described in our previous work[9].

### 3.3. Measurements of transmission properties in RF range

In order to test the transmission properties of this multilayer interconnection structure, the packaging structure is applied to a low noise amplifier (LNA) chip to evaluate the effect of the package. The operating range frequency of the LNA is from 10 to 15 GHz. Two layers of 25 $\mu$m thick BCB are used and a section of CPW line is fabricated for the measurement of scattering parameters. The microstrip on the top layer is designed to be 50 $\mu$m wide, as shown in Fig. 11.

$S$-parameters are measured using an Agilent 8722D network analyzer from DC to 20 GHz. The measured result after packaging is compared with the result of the bare chip. The measurement results of an embedded LNA chip are presented in Fig. 12, which shows that the insertion loss ($S_{21}$) change by the packaging structure is less than a 1 dB range at the operating frequency. The return loss ($S_{11}$) is less than –8 dB from 10 to 15 GHz. It can be concluded that the $S$-parameters change slightly after packaging.

## 4. Conclusion

A wafer-level multi-layer packaging technology with chips and passive components embedded in silicon substrate for MCM applied in the RF range is presented. BCB with a low dielectric constant is selected as the ILD. The application of gold stud bumps achieves very short interconnections that limit cost and loss to the minimum. The processing parameters of BCB coating and curing are optimized to form a steady BCB film. Furthermore, the influence of the CMP process on

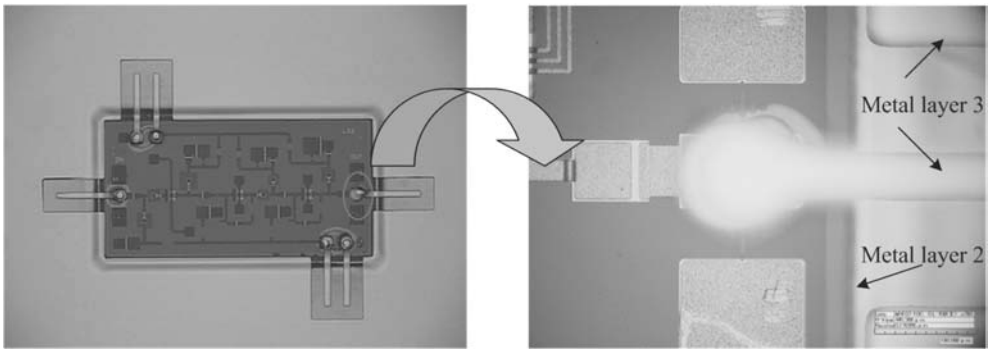



Fig. 11. Top view of the packaging structure.

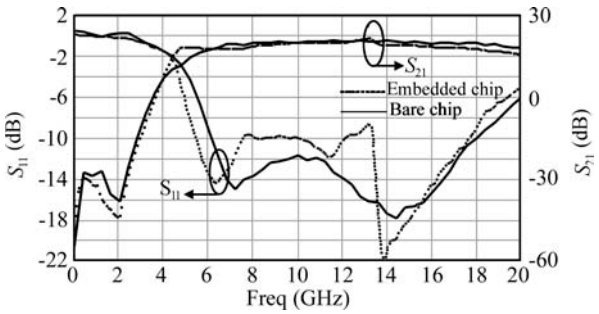



Fig. 12. $S$-parameter changes before and after being packaged.

the BCB film is researched in detail and a smooth BCB surface is achieved. The thermal, mechanical and electrical performances of this packaging structure are excellent. The thermal resistance can be controlled below 2 °C/W. Simultaneously, the temperature of the power modules (1.1 W) is steady below 80 °C. The average shear strength of the gold bumps on the BCB surface is above 70 N/mm$^2$. The test results show good transmission properties of this packaging structure up to 20 GHz. For an LNA chip, the insertion loss ($S_{21}$) change after the packaging process is less than a 1 dB range at the operating frequency, and the return loss ($S_{11}$) is less than –8 dB from 10 to 15 GHz.

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