Analysis of trigger behavior of high voltage LDMOS under TLP and VFTLP stress

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Abstract: The physical mechanisms triggering electrostatic discharge (ESD) in high voltage LDMOS power transistors (> 160 V) under transmission line pulsing (TLP) and very fast transmission line pulsing (VFTLP) stress are investigated by TCAD simulations using a set of macroscopic physical models related to previous studies implemented in Sentaurus Device. Under VFTLP stress, it is observed that the triggering voltage of the high voltage LDMOS obviously increases, which is a unique phenomenon compared with the low voltage ESD protection devices like NMOS and SCR. The relationship between the triggering voltage increase and the parasitic capacitances is also analyzed in detail. A compact equivalent circuit schematic is presented according to the investigated phenomena. An improved structure to alleviate this effect is also proposed and confirmed by the experiments.

Key words: electrostatic discharge; transmission line pulsing; very fast transmission line pulsing; lateral double-diffused metal–oxide–semiconductor transistor

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1. Introduction

LDMOS transistors are widely used as output drivers in multiple applications in smart power IC designs，such as switching power supplies, amplifiers, and automotive applications[1, 2]. In these applications, ESD (electrostatic discharge) poses a grave threat to these ICs. Increasingly, such devices are used to avoid unexpected ESD damage in the internal circuit of ICs. However, LDMOS (lateral double-diffused metal–oxide–semiconductor transistor) devices are generally not robust enough under ESD events due to deep snapback behavior caused by current crowding and the inhomogeneous trigger of the parasitic bipolar transistors[3]. Protecting these high voltage devices against ESD has become a challenge, particularly for very fast transients as observed during a CDM (charge device model) event.

It is well known that the snapback triggering voltage V_t of MOS devices and SCR devices can be influenced by the rise time t_{rise} of ESD stress pulses. As t_{rise} decreases, triggering voltage V_t also decreases due to the increase of displacement current caused by parasitic capacitances[4, 5]. However, the high voltage LDMOS reveals a different behavior, that triggering voltage increases when t_{rise} decreases under very fast transient ESD stress conditions, and a high triggering voltage is unfavorable for ESD protection. The unique ESD breakdown mechanism of high voltage LDMOS structures under very fast transients has been reported in Ref. [6]. However, detailed analysis of this phenomena and an improved method are both less documented. In this paper, the ESD failure mechanisms of high voltage LDMOS structures under TLP and VFTLP are discussed. In order to explain this unique phenomenon, a simple equivalent circuit schematic is also developed. The ESD characteristics of the LDMOS transistor under TLP and VFTLP stress are investigated by Sentaurus Device using a set of macroscopic physical models related to previous studies[7]. The analytical results are compared with the simulation results and they agree well with each other. Moreover, an improved structure is presented and confirmed by the experiments.

2. Device structure and simulation

A simplified cross section of the LDMOS devices (> 160 V) investigated in this paper is shown in Fig. 1. The structure is fabricated in a P-Substrate with N-Well, N-Drift and P-Body diffusion. The P-Substrate bulk contact is shortened with the source terminal. In order to improve the breakdown voltage, a poly silicon field plate is added by extending the gate poly. Two-dimensional simulation structure is illustrated in Fig. 2. When the device is under ESD stress, the source, bulk and gate are shorted together as a ground terminal and a positive TLP current pulse is applied on the drain terminal. The rise time of transients generated using TLP is 10 ns, while the rise time for VFTLP is 100 ps. It can be seen from Fig. 3 that V_t (triggering voltage) of the LDMOS is 191 V under VFTLP conditions, an

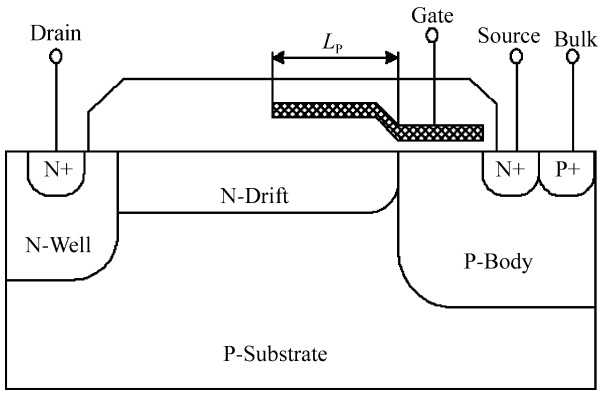

Fig. 1. Simplified cross section of the studied device.

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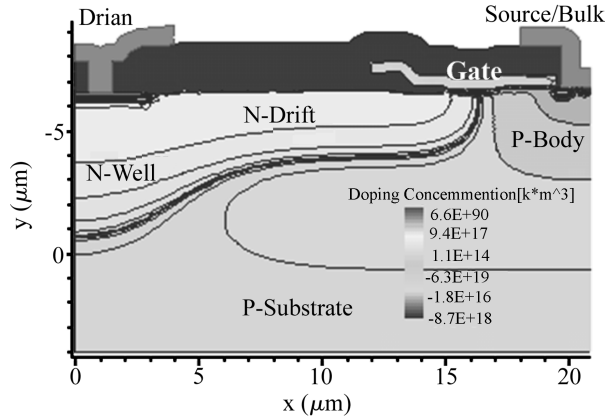

Fig. 2. Simulation structure and doping distribution of LDMOS.

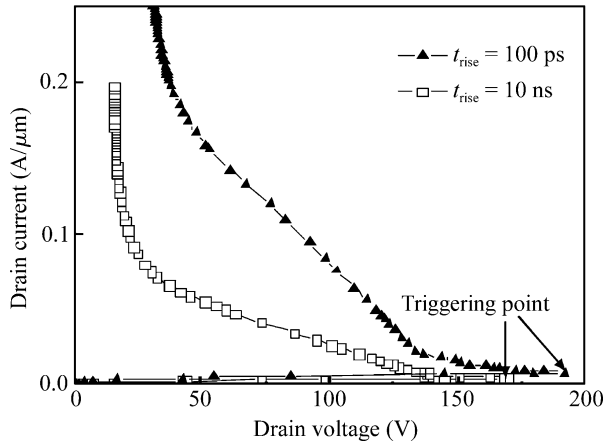

Fig. 3. Simulated I–V characteristics of the traditional LDMOS under TLP and VFTLP.

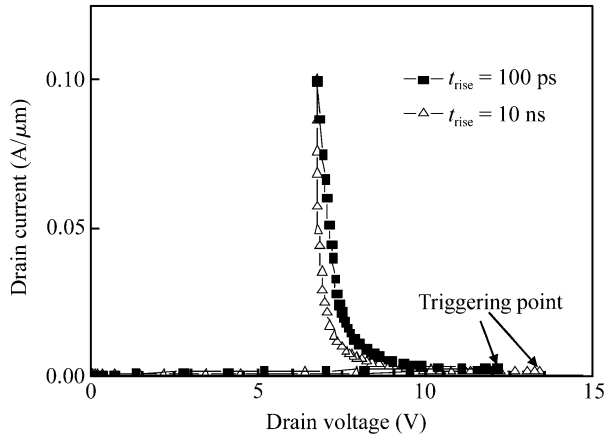

Fig. 4. Simulated I–V characteristics of NMOS under TLP and VFTLP.

increase of 20 V compared with TLP conditions.

In order to better describe the phenomenon, another simulation of a low voltage gate ground NMOS (the breakdown voltage is about 13 V) under TLP and VFTLP is also done using the same TCAD simulation models. Consequently, we get a completely different result. The triggering voltage V_t of the NMOS is 13.37 V for TLP and 12 V for VFTLP as shown in Fig. 4. It is obvious that the triggering voltage reduces by

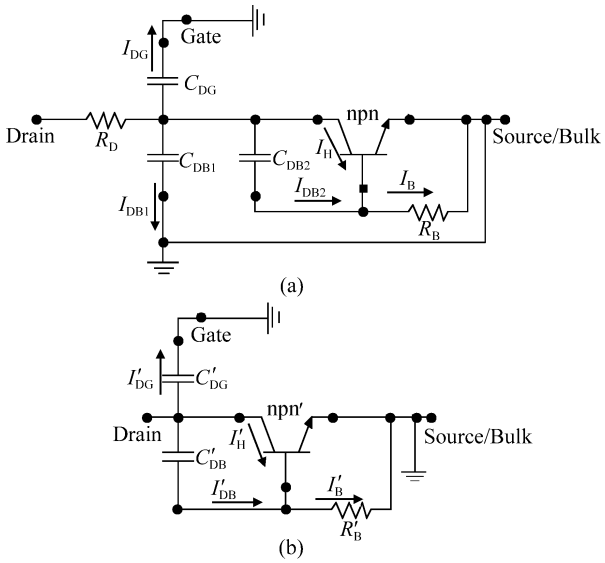

Fig. 5. Equivalent circuit of (a) high voltage LDMOS and (b) low voltage NMOS under transient stress.

1.37 V when the rise time of the TLP pulse varies from 10 ns to 100 ps.

3. Analysis and discussion

Novel compact equivalent circuit schematics which can be used to explain the above simulation results are presented in Fig. 5 for LDMOS (Fig. 5(a)) and NMOS (Fig. 5(b)) under ESD conditions. The situations at the trigger point of the parasitic bipolar transistors are sketched here. In addition to the parasitic bipolar transistors, the equivalent circuits also depict the parasitic capacitances related to the drain terminals. As shown in Fig. 5(a), C_{DG} is the parasitic capacitance between the gate and N-drift, which cannot be ignored, and it is affected by the lengths of field plate (L_P) and N-drift. C_{DB1} and C_{DB2} are the junction capacitances between the N-drift and P-substrate, N-drift and P-body respectively. R_D is the equivalent resistance of the N-drift region while R_B is a small resistor of the region under the source region in the P-body. Relative to the LDMOS device structures, NMOS transistors are more simple and only have two main capacitances related to the drain terminal: C'_{GD} (the parasitic capacitance between gate and drain), C'_{DB} (the junction capacitance between gate and substrate), as can be seen in Fig. 5(b).

3.1. Snapback effect in gate ground NMOS

As the drain voltage increases due to the ESD event being applied for the drain, the drain-substrate junction becomes more reverse biased until it goes into avalanche breakdown. From Fig. 5(b), if the effects of parasitic capacitances are not considered, $I'_B = I'_H$, where I'_H is the triggering current due to impact ionization of drain–substrate (collector/base of parasitic transistor npn′). As the base–emitter voltage ($I'_B R'_B$) of npn′ reaches about 0.7 V, the transistor npn′ turns on. The drain voltage at this point is the triggering voltage V_t and $V_t = V_{BV}$ (V_{BV} is the breakdown voltage of the device). However, the influences caused by the parasitic capacitances become more important when the rise time of the ESD stress pulse is faster.

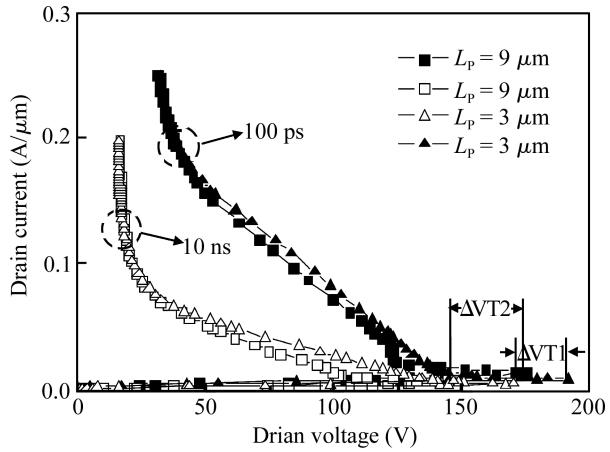

Fig. 6. I–V characteristics of LDMOS with t_{rise} and L_P available.

So attention should be paid to the displacement currents I'_{DB} ($I'_{DB} = C'_{DB} \times dV/dt$) and I'_{DG} ($I'_{DG} = C'_{DG} \times dV/dt$); I'_{DB} is the more important one under VFTLP stress. According to the equation $I'_H = I'_B - I'_{DB}$, V_t reduces because a relatively small impact ionization current is needed to turn the parasitic bipolar transistor on[8].

3.2. Snapback effect in LDMOS

When it comes to the high voltage LDMOS under ESD stress, the situation is a bit more complicated. When ESD stress is applied to the drain, the N-drift-substrate junction of the LDMOS (collector/base of parasitic transistor npn) is reverse biased. As the voltage across the junction reaches its breakdown voltage, $I_B = I_H$, which is generated in the depletion layer due to impact ionization, causes a voltage drop ($I_B R_B$) across the R_B resistor if the capacitive effect is not considered. The parasitic bipolar transistor npn is triggered when the voltage drop is greater than about 0.7 V, and the triggering voltage can be calculated by

$$V_t = V_{BV} + I_B R_D. \quad (1)$$

This is the reason why triggering voltage is higher than breakdown voltage in LDMOS devices[9]. Also, unlike the gate ground NMOS, the triggering voltage increases when the rise time reduces. From Fig. 5(a), the displacement currents I_{DB1}, I_{DB2} and I_{DG} are caused by the capacitances C_{DB1}, C_{DB2} and V_{DG} respectively when the transient characteristic is considered. The increase of I_{DB2} causes a reduction of the breakdown voltage (ΔV_{BV}); meanwhile, the voltage drops as the resistance R_D increases by ΔV_{RD} because of increased currents I_{DB1}, I_{DB2} and I_{GD}. Accordingly, the drain–source voltage increases because ΔV_{RD} is larger than ΔV_{BV}.

To sum up, both the drift region resistance R_D and parasitic capacitance cause the increase of V_t under fast transient conditions. Moreover, the increasing amount of V_t is proportional to the parasitic capacitive size.

The following operations are used to support the above conclusions. The capacitance C_{DG} becomes greater when the length of field plate L_P (as shown in Fig. 1) is increased from 3 to 9 μm. Figure 6 displays the simulated snapback characteristic results of the devices. ΔV_{t1} is the difference between triggering voltages of the LDMOS device with 3 μm L_P under TLP and VFTLP conditions, while ΔV_{t2} is the corresponding voltage of the LDMOS device with 9 μm L_P. The increment of V_t is greater when the device has a larger parasitic capacitance C_{DG} under fast transient conditions, as seen in Fig. 6. It is worth noting that both breakdown voltage and triggering voltage decrease when L_P becomes longer.

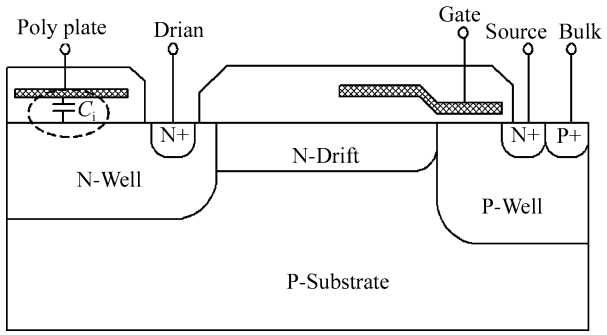

Fig. 7. A novel high voltage LDMOS with a poly plate.

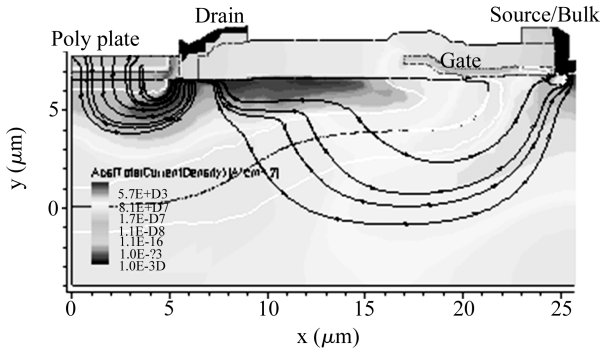

Fig. 8. 2D current density distribution and current flow lines of the novel device in the triggering step.

4. A novel LDMOS device structure

In many cases, the increase of triggering voltage under fast transient stress is not expected for ESD protection. In order to alleviate the increment of triggering voltage without changing the breakdown voltage, a novel improved structure with a poly plate above the N-Well is proposed, as shown in Fig. 7. The proposed LDMOS is fabricated by using 1-μm high-voltage (HV) CDMOS IC technology, same as the traditional structure. The substrate is P-Type silicon, whose resistivity is 25 Ω·cm and the N-Drift length is 13 μm.

As shown in Fig. 7, there is a new parasitic capacitance, C_i. When the novel LDMOS is used as an ESD protection device, the source, gate, bulk and poly plate are shorted together as a grounded terminal and the drain is the other terminal. The function of the capacitance is to reduce the displacement current which flows through the low concentration N-Drift region, when the device suffers from fast transient stress. Figure 8 displays the simulated 2D current density distribution and current flow lines of the novel device in the triggering step.

Figure 9 shows the TLP results of the novel LDMOS with the poly plate. The increment of trigger voltage ΔV_t is only 8 V for the novel structure under TLP and VFTLP, and the simulation results are in qualitative agreement with the experimental results, as shown in Fig. 10.

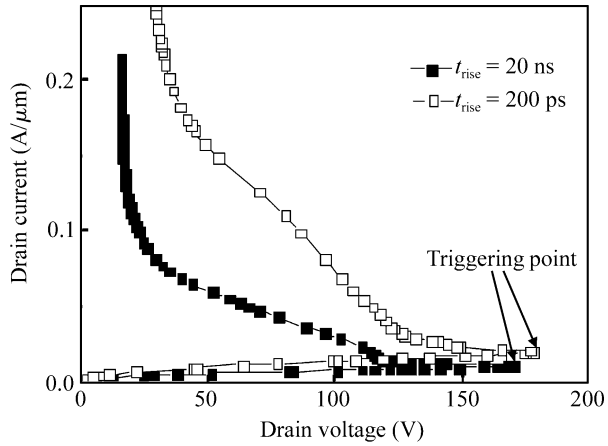

Fig. 9. Simulated I–V characteristics of the proposed LDMOS under TLP and VFTLP.

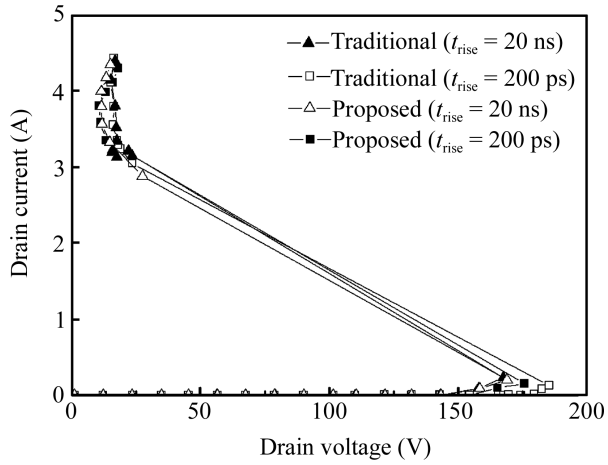

Fig. 10. TLP-measured I–V curves of traditional and proposed LDMOS devices (the width of the devices is 15 μm).

5. Conclusion

In this paper, we have found that the parasitic capacitances and drift resistor play an important role in the triggering voltage increment when fast transient ESD stress is applied on a high voltage LDMOS. An equivalent circuit schematic has been proposed to explain this novel phenomenon. Additionally, an improved structure which is suitable to reduce the growth of triggering voltage under fast TLP rise times has been presented. The simulation characteristics of the device are in qualitative agreement with the experimental results.

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