A high-performance low-power CMOS AGC for GPS application

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Abstract: A wide tuning range, low power CMOS automatic gain control (AGC) with a simple architecture is proposed. The proposed AGC is composed of a variable gain amplifier (VGA), a comparator and a charge pump, and the dB-linear gain is controlled by the charge pump. The AGC was implemented in a 0.18 μm CMOS technology. The dynamic range of the VGA is more than 55 dB, the bandwidth is 30 MHz, and the gain error is lower than $\pm$1.5 dB over the full temperature and gain ranges. It is designed for GPS application and is fed from a single 1.8 V power supply. The AGC power consumption is less than 5 mW, and the area of the AGC is 700 $\times$ 450 μm^2.

Key words: linear-in-dB; comparator; variable gain amplifier; automatic gain control
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1. Introduction

Automatic gain control (AGC) is an essential function in modern wireless communication systems because the power received through the wireless channel is unpredictable. The AGC is employed in GPS systems to maintain a desired output signal amplitude with an input signal of variable strength. Therefore, AGC circuits have been proposed in CMOS technologies to attain large integration and chip-cost reduction.

Conventional closed-loop analog AGCs use feedback loops to adjust the gain of the variable gain amplifier (VGA) to get the desired output signal strength. In such AGC loops, the input signal is amplified by the VGA. The comparator compares the signal extracted from the strength of the output by the peak detector with a reference voltage to set a control signal in the output. The loop filter averages the control signal to generate a dc signal to vary the gain of the VGA. By this feedback loop, this circuit can automatically sense the strength of the output signal and modify the gain of the VGA to maintain a stable output signal strength.

The conventional AGC loop uses a peak detector, which can be considered as an RMS-DC converter. The limitations[1] of these circuits are given by the useful frequency range and by process and temperature variations, especially when a low supply voltage CMOS process is used.

This paper proposes a simple architecture to realize a precise automatic gain control loop suited for large scale integration. The architecture proposed does not require a precise rectifier function or a CMOS active filter, and the variable gain amplifier is controlled by a charge pump. The paper describes the proposed AGC architecture and the circuit design of the key function blocks.

2. AGC architecture

The block diagram of the proposed AGC circuit is presented in Fig. 1. It is mainly composed of a variable gain amplifier block, a comparator bank and a charge pump[1]. When an input signal comes into VGA and is amplified it will output an instantaneous dc level to compare with the reference voltage ($V_{\rm ref}$). When the dc level from the VGA is higher than $V_{\rm ref}$, the charge-pumping circuit will discharge the loop capacitor to decrease the dc level of the control-voltage node. On the other hand, the charge-pumping circuit will charge the loop capacitor to increase the dc level of the control-voltage so as to raise the gain of the VGA chain. Thus a small signal will be amplified, and a large signal will be shrunk. Finally, the AGC can output a constant-amplitude signal in its operating range, regardless of the input signal's amplitude.

Since a closed-loop operation is used in the AGC circuit, stability and settling time must be considered. The settling time is neither too long nor too short; if the settling time is too short, the loop circuit changes rapidly and causes frequency distortion with the variation of input signal which lead to error codes. It may be that the control voltage change does not follow the loop input signal variation, resulting in the output signal magnitude exceeding the AGC scope, which also cause error codes at long settling times. In Ref. [2], it is shown that the settling time of the AGC will remain constant when the characteristic of "gain versus control voltage" in the VGA is linear in the dB domain. Therefore, how to make a VGA with a linear-in-dB

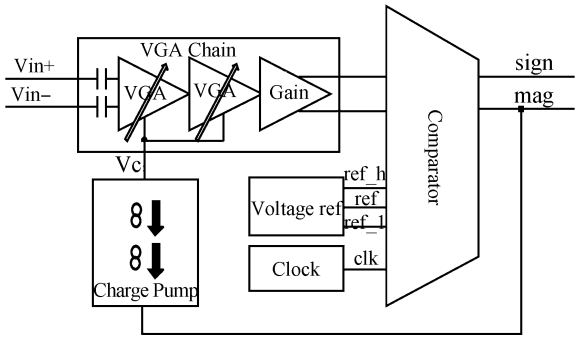

Fig. 1. Automatic gain control circuit architecture.

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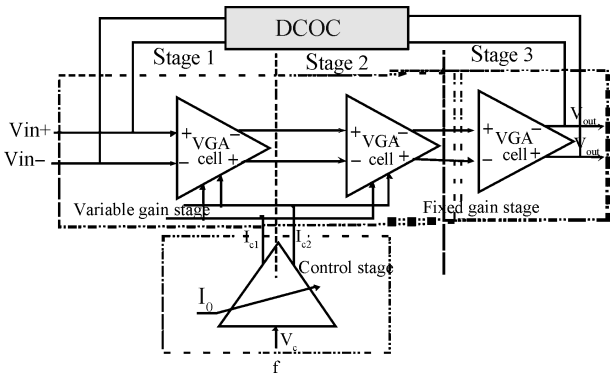

Fig. 2. Block diagram of the overall VGA.

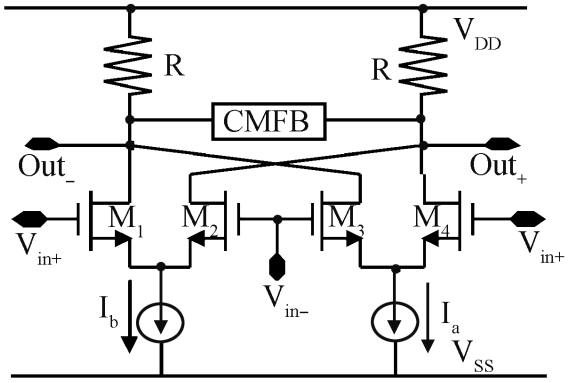

Fig. 3. Core circuit of the variable gain amplifier.

characteristic has become a research topic, especially in CMOS technology.

2.1. Variable gain amplifier

The VGA is the main part of an AGC. Exponential gain control is required to achieve a wide dynamic range and to maintain the AGC loop settling time independent of the input signal level. However, it is difficult to realize this exponential function due to its inherent square law characteristics in CMOS technology. Therefore, the decibel linear gain variation characteristics are realized by the circuit implementation in recent CMOS-based analog VGA designs. This paper adopts an approximated exponential function to implement the VGA circuit.

The VGA block used is shown in Fig. 2. It is composed of three stages, a gain control circuit and a DC offset circuit. DCOC is used to eliminate the DC offsets introduced by themselves and the previous stages. The first two stages are the variable gain amplifier and the last stage is a fixed gain amplifier. The control stage generates two currents, I_{C1} and I_{C2}, which are functions of the control voltage to make the gain become linear-in-dB along with the control voltage V_c.

Figure 3 shows the circuit schematic of the variable gain amplifying block[3] that is adopted for the proposed VGA, including the common-mode feedback circuit. The block is composed of a Gilbert cell type amplifier. It best meets the receivers which require low noise, large gain for a small input signal and large continuous gain turning range. The differential gain can

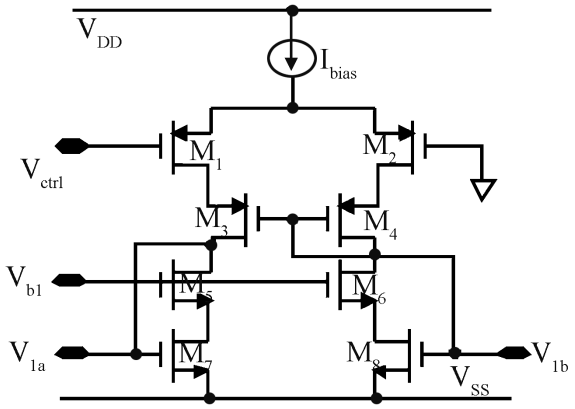

Fig. 4. Control stage circuit.

be expressed as

$$\text{gain} = R(g_{m1} - g_{m2}) = R(\sqrt{2\beta_1 I_b} - \sqrt{2\beta_2 I_a}). \quad (1)$$

By turning its biasing currents I_a and I_b, its transconductance can be varied and hence its gain. The biasing currents of the VGA are varied by a simple gain controller, Fig. 4[3]. The controller is mainly composed of a differential pair. The currents, which flow in two current sources M7&8, are controlled by M1&2. M3&4 are added to improve the VGA's gain in decibels which changes more linearly with the control voltage. The gates of M1&2 are connected to V_{ctrl} and ground respectively. By varying the V_{crl} from 0 to 1.5 V, the gain of the VGA sweeps from minimum to maximum. The dynamic range of the VGA gain can be written as

$$\text{DR (dB)} = 20\lg\frac{V_{out,max}}{V_{out,min}} = 20\lg\frac{\sqrt{aI_{bias}}}{\sqrt{I_{a,min}} - \sqrt{I_{b,max}}},$$

$$I_a + I_b = aI_{bias},$$

where a is a multiple of the mirror current.

In VGA designs, a temperature-insensitive gain control characteristic over a wide temperature and gain range is desired. For example, in GPS application, the gain should have minimal deviation over a temperature range from –40 to 90 °C. Considering the proposed VGA (including the control circuit), the gain can be rewritten as

$$\text{gain} = R(g_{m1} - g_{m2}) = Ru_nC_{ox}$$

$$\times\left[\left(\frac{W}{L}\right)_{1,2}(V_{GS1} - V_{TH1}) - \left(\frac{W}{L}\right)_{3,4}(V_{GS3} - V_{TH3})\right]. \quad (2)$$

We can think of R as being equal to the PMOS transistor's r_{ds} resistor. In our CMOS technology, the resistor (r_{ds}), the mobility (μ), and the threshold voltage (V_{th}) decrease with temperature. Consequently, according to Eq. (2), we can counteract the temperature coefficients of the bracket inside and outside to decrease the temperature effect versus the gain curve through setting a proper W/L value.

Since the linearity is dominated by the last stage of cascade amplifiers, a good linearity amplifier should be placed at the last stage. The fixed gain amplifier[4] (Fig. 5) has an open-loop

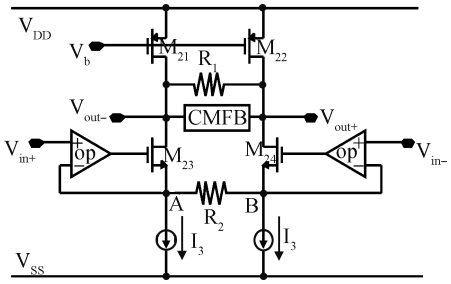

Fig. 5. Fixed gain amplifier.

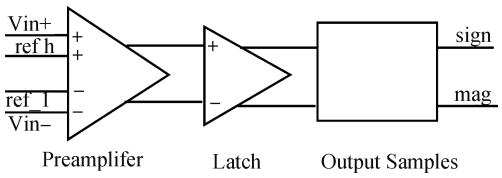

Fig. 6. Architecture of the proposed comparator.

structure, which consists of a V–I converter (input op-amps, M23 & M24, and R_2) and a resistive load (R_1). M23 and M24 operate in source follower configuration; the differential input voltage $V_{\rm in} = V_{\rm in+} - V_{\rm in-}$ is copied over the series impedance of the two nonlinear transconductance $g_{\rm m1}$(of M23 & M24) and the linear degeneration resistor R_2. The $g_{\rm m1}$ linearity is improved by the closed-loop structure, including the input op-amps, which uses a single differential pair for large bandwidth and low noise level.

The fixed gain amplifier dc-gain G, is calculated as follows:

$$G = \frac{R_1}{R_2 + \dfrac{1}{g_{\rm m1}(1+A_0)}} \frac{A_0}{1+A_0} \cong \frac{R_1}{R_2}. \tag{3}$$

where A_0 is the input op-amp dc-gain.

In this design, the variable gain amplifier can achieve a 28 dB variable gain range. The first VGA cell is the same as the second one, and the VGA adopts the first two stages in cascade so that 56 dB of gain variation can be obtained.

2.2. Comparator

Transmit delay and sensitivity are two important characteristics of the comparator. In the AGC system, the comparator is used to compare the VGA output instantaneous dc level with the reference voltage; limited sensitivity and a large transmit delay cause error to the whole system. In order to reduce the error, the VGA system needs a high-speed, high-sensitivity comparator.

The high-speed comparator presented in this paper is made up of three stages: a preamplifier stage, a latch and output stage, as shown in Fig. 6. In order to achieve high conversion speed, a double fully differential circuit structure with MOS diode resistors as its load was used, as shown in Fig. 7. The advantage[5−7] of this architecture is that the comparison between input and reference voltage is continuous and there is no need to allow for settling time for the difference between input and reference voltage before amplification. This architecture amplifies the

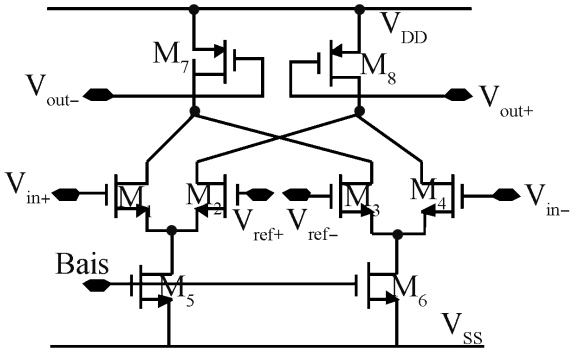

Fig. 7. Preamplifier schematic.

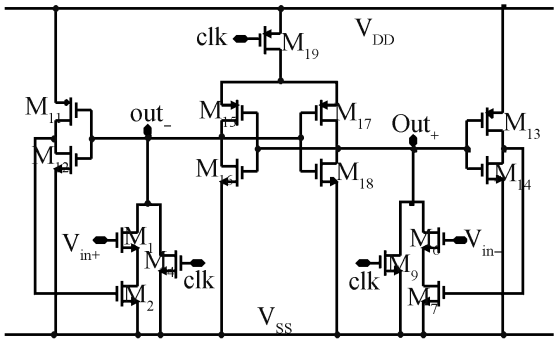

Fig. 8. Schematic of latch stage.

differences of $V_{\rm in+} - V_{\rm ref+}$ and $V_{\rm ref-} - V_{\rm in-}$ respectively and then adds them together. To achieve high speed, the preamplifier should be devised with a wide bandwidth and small gain. However, a comparator with too small a gain is not capable of effectively reducing the offset. The preamplifier proposed in this paper can obtain a good compromise between bandwidth and gain.

The proposed latch illustrated in Fig. 8 consists of a cross-coupled pair of NMOS and PMOS transistors, which are connected to the supply voltage through the clock enabled transistor M19. Its operation can be explained as follows: when clk is high, the latch is in its reset state. In this state, transistor M19 turns off, there is no current path in the latch, and M4, M9 simultaneously turn on; outputs are low. When clk is low, M19 will turn on, and M4, M9 turn off. If $V_{\rm in+}$ is bigger than $V_{\rm in-}$, the node out$_-$ maintains its low level, and the inverter M17, M18 gives out$_+$ a high level. When clk is low, M2 turns on and M7 turns off, in spite of the relationship between $V_{\rm in+}$ and $V_{\rm in-}$, the output node out$_-$ stays low and the out$_+$ stays high.

2.3. Charge pump

The charge-pumping circuit (Fig. 9) will discharge or charge the loop capacitor to change the dc level of the control-voltage so as to adjust the gain of the VGA chain. When $V_{\rm c}$ is low (i.e. $V_{\rm cb}$ is high) transistor M2, M4 turn on, M1, M3 turn off, which makes M7, M8 turn off, the capacitor C discharge, so $V_{\rm ctrl}$ decreases. When $V_{\rm c}$ is high, M2, M4 turn off; at the same time, M1, M3 turn on. Due to the transistor M1, which make PMOS M7, M8 turn on, the charge-pump circuit charge capacitor C and the $V_{\rm ctrl}$ voltage increase.

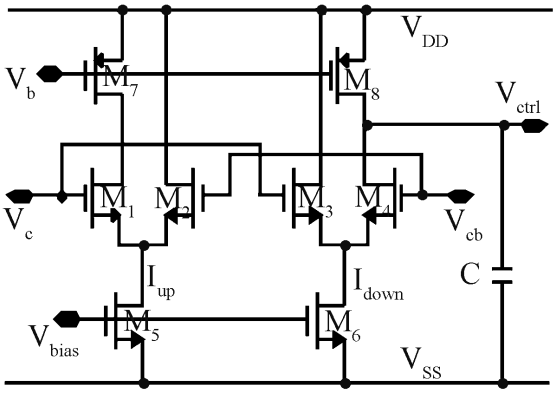

Fig. 9. CMOS charge-pump circuit.

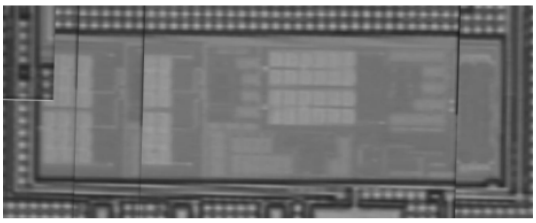

Fig. 10. Micrograph of the AGC.

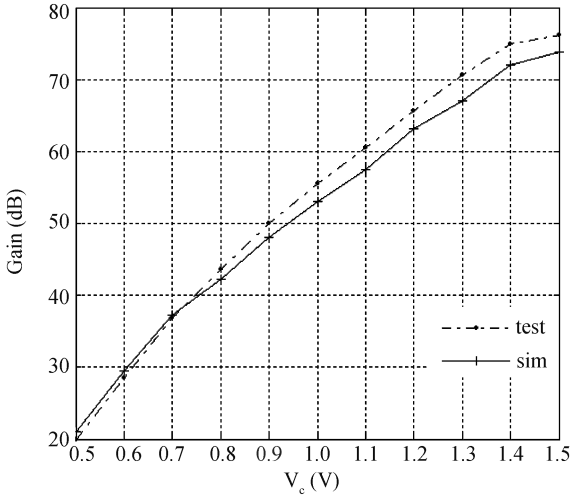

Fig. 11. Gain versus control voltage curve of the proposed VGA.

3. Measurement results

The proposed AGC is fabricated in 0.18 μm CMOS technology with a supply voltage V_{DD} = 1.8 V. Figure 10 shows a micrograph of the AGC, which occupies 700 × 450 μm^{2}die size.

The gain of the VGA was measured and is plotted in Fig. 11 as a dB-linear function of the control voltage. The maximum gain of the VGA is 75 dB, and the gain control range is about 55 dB. The measurements in Fig. 12 match simulation results well. Figure 12 shows the measured gain versus control voltage at temperatures of $-40, 27, 90$ °C, respectively, and the gain error is less than $\pm$1.5 dB over the full temperature and gain ranges. The measured frequency responses of the three-stage

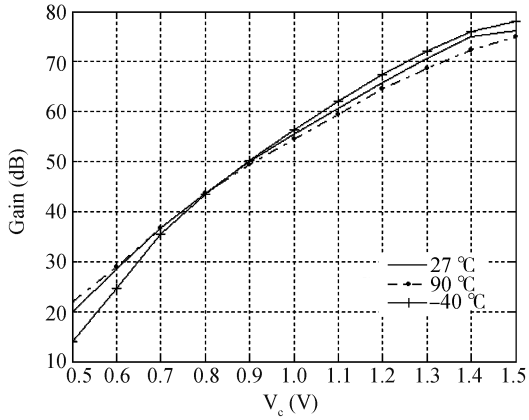

Fig. 12. Gain control curve at different temperatures.

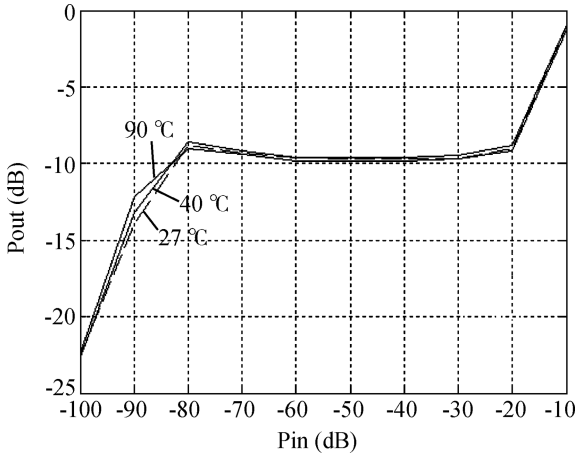

Fig. 13. Measured AGC curves.

Table 1. Summary AGC performances.

Parameter	Value
Technology	0.18 μm CMOS
Supply voltage	1.8 V
Frequency response	30 MHz
VGA gain range	20–75 dB
Gain error (-40 to 90 °C)	$\pm$1.5 dB
Control voltage range	0.5–1.45 V
Power consumption	5 mW

VGA verifying the circuit can pass the required bandwidth of 130 kHz to 30 MHz, and the bandwidth remains constant around 30 MHz independent of the VGA gain.

In Fig. 13, the measured results show that the output power of the AGC amplifier is given as a function of the input power. Automatic gain control in the range is larger than 50 dBm. Table 1 gives the measurement result summary of the AGC.

4. Conclusion

This paper presents an automatic gain control circuit based on a comparator and a charge pump, which control the gain of the variable gain amplifier. The proposed architecture is very simple and can be implemented with basic cells, simultaneously obtaining high performance characteristics. The dynamic range of the variable gain amplifier is more than 55 dB and the

bandwidth is 30 MHz. The AGC output power is −9.8 dBm and the AGC working range is larger than 50 dBm. It is designed for a receiver of GPS application and is fed from a single 1.8 V power supply. Its power consumption is 5 mW and the area of the AGC is $700 \times 450\ \mu m^2$.

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