Noise-canceling and IP3 improved CMOS RF front-end for DRM/DAB/DVB-H applications

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Abstract: A CMOS RF (radio frequency) front-end for digital radio broadcasting applications is presented that contains a wideband LNA, I/Q-mixers and VGAs, supporting other various wireless communication standards in the ultra-wide frequency band from 200 kHz to 2 GHz as well. Improvement of the NF (noise figure) and IP3 (third-order intermodulation distortion) is attained without significant degradation of other performances like voltage gain and power consumption. The NF is minimized by noise-canceling technology, and the IP3 is improved by using differential multiple gate transistors (DMGTR). The dB-in-linear VGA (variable gain amplifier) exploits a single PMOS to achieve exponential gain control. The circuit is fabricated in 0.18-μm CMOS technology. The S_{11} of the RF front-end is lower than -11.4 dB over the whole band of 200 kHz–2 GHz. The variable gain range is 12–42 dB at 0.25 GHz and 4–36 dB at 2 GHz. The DSB NF at maximum gain is 3.1–6.1 dB. The IIP3 at middle gain is -4.7 to 0.2 dBm. It consumes a DC power of only 36 mW at 1.8 V supply.

Key words: RF front-end; noise-canceling; DMGTR; dB-in-linear; DRM/DAB/DVB-H; CMOS
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1. Introduction

The demand for the integration of multiple standards into a single portable terminal is growing, together with the proliferation of wireless communication standards. Multi-standard radio front-ends should be compatible with various wireless communication standards covering the frequency range from several hundred kilohertz to several gigahertz. Digital radio mondiale (DRM)[1], digital audio broadcasting (DAB) and digital video broadcasting (DVB-H) have been introduced as digital standards for radio broadcasting in different frequency bands. DRM covers the frequency range from 148 kHz to 27 MHz, with the latest version DRM+ up to 108 MHz. DAB covers two different bands, band III (174–240 MHz) and band L (1.452–1.492 GHz). DVB-H covers the frequency range from 174 MHz to 862 MHz. Challenges in the implementation of such receivers come from their wideband nature[2]. An RF front-end must have high enough linearity to prevent it being blocked by out-of-band interference. Flexible analog filters with corner frequencies from several kHz to tens of MHz are required before the function of the ADC (analog-to-digital converter) in order to avoid aliasing and to select the desired channel.

Unfortunately, it is difficult for conventional techniques used to design such an RF and analog baseband circuit to meet the demand of the specifications. Most previous designs have less integration scaling with the three kinds of digital broadcasting standards[3]. In particular, there is as yet no monolithic RF front-end in the DRM band in the world. Direct-conversion receivers are a good candidate to realize wideband radios as they have the highest potential to reduce cost, size and power[4], but they still suffers from high NF and DC offset problems. Meanwhile, the RF frequency range is from kHz to GHz in DRM/DAB/DVB-H applications, and the frequency synthesizer in a direct-conversion receiver must have a tuning range corresponding to the RF signal, which is difficult to realize in PLL design.

In this paper, a dual-conversion low-IF (DLF) architecture is proposed; a common RF front-end with low noise and high linearity is shared by the DRM, DAB or DVB-H signals.

2. System design

The DLF DRM/DAB/DVB-H receiver architecture is shown in Fig. 1. The main objectives in choosing receiver architecture are wide dynamic range, high sensitivity, fewest off-chip components, and lowest power consumption. Our RF front-end comprises a low noise amplifier (LNA), an RF quadrature mixer (Mixer1) and a VGA, which up-converts the DRM signals and down-converts the DAB/DVB-H signals to the first IF (IF1) of 35 MHz. A two-stage poly-phase filter following the RF mixer partly rejects the image. Strictly the first

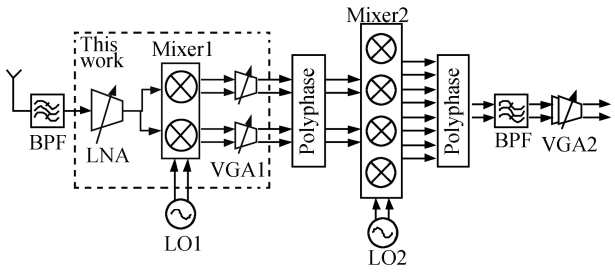

Fig. 1. Simplified DRM/DAB/DVB-H radio block diagram.

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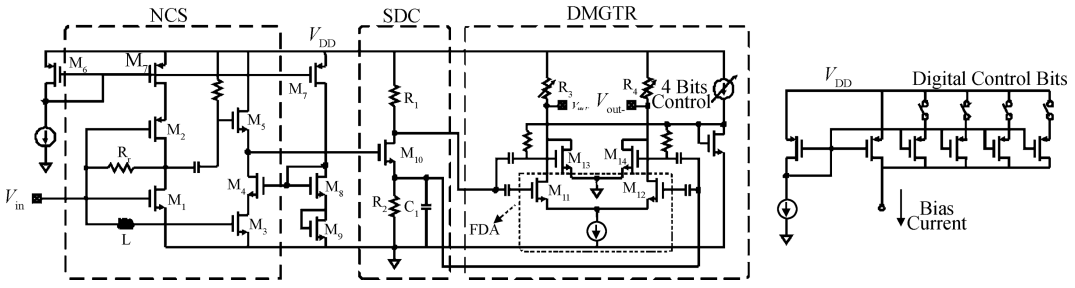

Fig. 2. Schematic of a low noise amplifier.

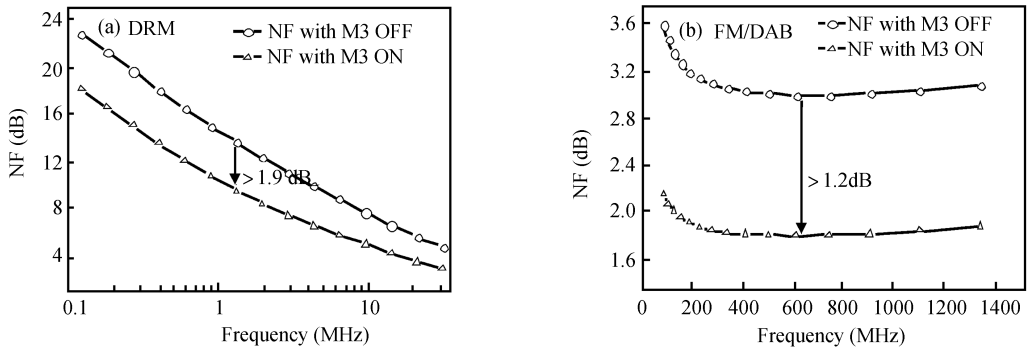

Fig. 3. Simulated NF of NCS with M3 turned ON and OFF at (a) DRM and (b) DAB/DVB-H frequency ranges.

image in this architecture need not be suppressed, because the IF mixers up-convert it into the stopband of the subsequent channel selecting bandpass filter. Nevertheless, it was decided to suppress the first image in this receiver to relax the dynamic range of the IF mixers (Mixer2). The Mixer2 down-converts the desired signal from IF1 to IF2 whose frequency is 170 kHz for DRM and 2 MHz for DAB/DVB-H, respectively. Following the down-conversion, a 4-stage wideband poly-phase filter rejects the second image entirely on-chip. All signal paths except the LNA are differential to minimize interaction between various blocks, or through the substrate.

Compared with the conventional direct conversion or low IF with I/Q output solutions, this kind of architecture is compatible with traditional AM/FM radio tuners. Moreover, it has fewer off-chip components than a super heterodyne system when the same image rejection is provided. The proposed RF front-end also satisfies to the demands of other wireless communication standards in the frequency range of 200 kHz–2 GHz exploiting noise-canceling and IP3 improved technology.

3. Circuit design

3.1. Low noise amplifier

Figure 2 shows the proposed schematic of the LNA. It comprises a noise-canceling stage (NCS)[5], a single to differential converter (SDC), and a differential multiple gate transistor stage (DMGTR)[6].

The NCS consists of a current reusing stage M_1 and M_2 with a feedback resistor R, which is parallel to a cascade stage M_3 and M_4. The noise produced by the current reusing stage is canceled by the cascade stage. Actually, the principle of NCS is that the noise and impedance matching arise from two different devices, and are decoupled. The noise can, in principle, be lowered arbitrarily without affecting the impedance match. The inductor L is used to increase the bandwidth. The simulated NF with M_3 ON or OFF is compared in Fig. 3. The NF is reduced by at least 1.2 dB with the same power dissipation and a similar bandwidth.

The SDC comprises a single NMOS transistor connected to R_1 and R_2 with the same resistance. A small capacitor C_1 is in parallel to R_2 to decrease the imbalance of the amplitude and phase due to the mismatch of the parasitic capacitance at the drain and source of M_{10}. Simulated results show that the amplitude and phase imbalance is lower than 0.5 dB and 1° in the frequency range of 200 kHz–2 GHz.

A fully differential amplifier (FDA) connected in parallel with a pseudo-differential amplifier (PDA) is usually called a DMGTR amplifier, and has been used to improve the linearity of the circuits, as shown in Fig. 1. It is well known that the third derivative (g_m'') of a differential current over the differential input voltage is a major dominant factor for the third-order nonlinearity (IM_3) in CMOS amplifiers. In DMGTR amplifiers, the negative value of g_m'' which degrades the linearity of the FDA is compensated with a positive value of g_m'' in the PDA by adjusting the bias and the size of the transistor in the PDA. The PDA for compensating the g_m'' is biased at the near threshold voltage region. Thus it does not require extra power.

3.2. Mixer

A double-balanced Gilbert mixer topology is used for the quadrature mixer. The transconductance stage employs the DMGTR[7] method to achieve a better linearity than a conventional one. Compared with the all-PDA topology in Ref. [7], the proposed mixer adopts FDA+PDA topology which shows a better common-mode rejection ratio. Meanwhile, this kind of mixer has higher voltage gain and a lower NF than a passive

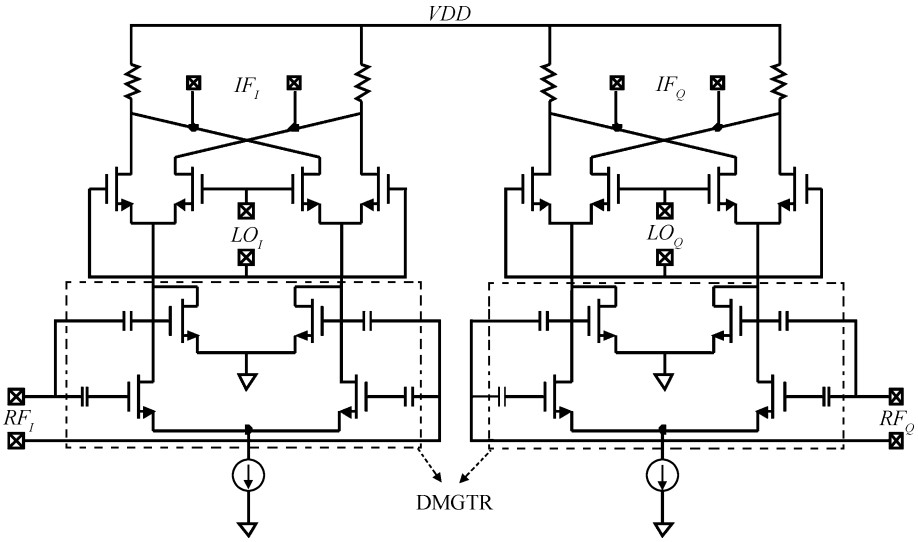

Fig. 4. Schematic of quadrature mixer.

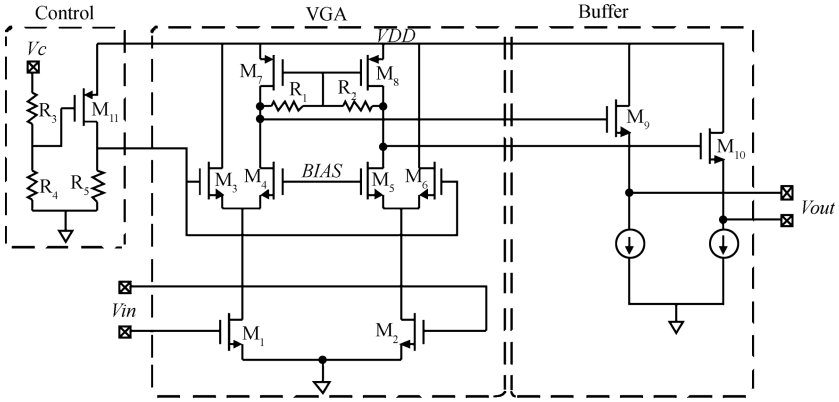

Fig. 5. Schematic of variable gain amplifier.

FET mixer. The gate sizes of the pseudo-differential transistors in Figs. 3 and 4 are 56 μm/0.18 μm, and the bias current is 95 μA. In order to reduce the deviation of the transconductance caused by the process, the bias current is controlled by 4 controlling bits as shown in Fig. 3.

3.3. VGA

Figure 5 shows the circuit schematic of the proposed signal-summing VGA with exponential gain control. This VGA employs PMOS transistors M_7 and M_8 as a load with the common-mode feedback resistors R_1 and R_2. The voltage gain is controllable by changing the gate voltage of M3 and M4. The tail current source is eliminated to enhance the linearity of the VGA. The exponential gain control circuit is shown in Fig. 5. The common-source PMOS transistor M_{11} works in the linear region. By combining the variable-gain stage and the exponential gain control circuit, the logarithmic current gain of the circuit becomes linear along with the control voltage as follows:

$$\text{Gain (dB)} = 20\lg\left(K_1 \mathrm{e}^{\frac{R_4R_5}{R_3+R_4}\mu_\mathrm{p}C_\mathrm{ox}\frac{W_{11}}{L_{11}}V_\mathrm{c}}\right), \qquad (1)$$

where K_1 can be written as

$$K_1 = \frac{R_\mathrm{L}g_\mathrm{m1}W_3/L_3}{(V_\mathrm{GS4}-V_\mathrm{TH4})\,W_4/L_4}, \qquad (2)$$

where R_3, R_4 and R_5 are the resistors in the exponential gain control circuit. μ_p, C_ox and V_th4 are process related parameters. V_c is the controlling voltage.

4. Experimental result

The RF front-end is fabricated in a 1P6M 0.18-μm CMOS process. Figure 6 shows the die photograph. The die size (without the test pad) is 900 × 700 μm^2. The total power consumption is 36 mW at 1.8 V supply including the LO buffer and the VGA output test buffer.

The measured S_{11} is shown in Fig. 7(a). It has a value of lower than –11.4 dB in the frequency range of 200 kHz–2 GHz. Figure 7(b) shows the measured voltage gain versus frequency when the controlling voltage varies from 0.3 to 1.4 V. The gain varies in the range of 12–42 dB at 0.25 GHz and in the range of 4–36 dB at 2 GHz, achieving a variable range of more than 30 dB. At high frequencies, the gain drops due to the input parasitic capacitance.

Figure 8 shows the measurement result of the two-tone intermodulation test of the conventional mixer and the proposed

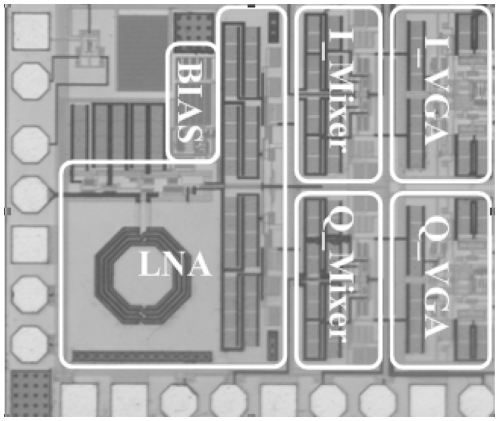

Fig. 6. Die photo of the RF front-end.

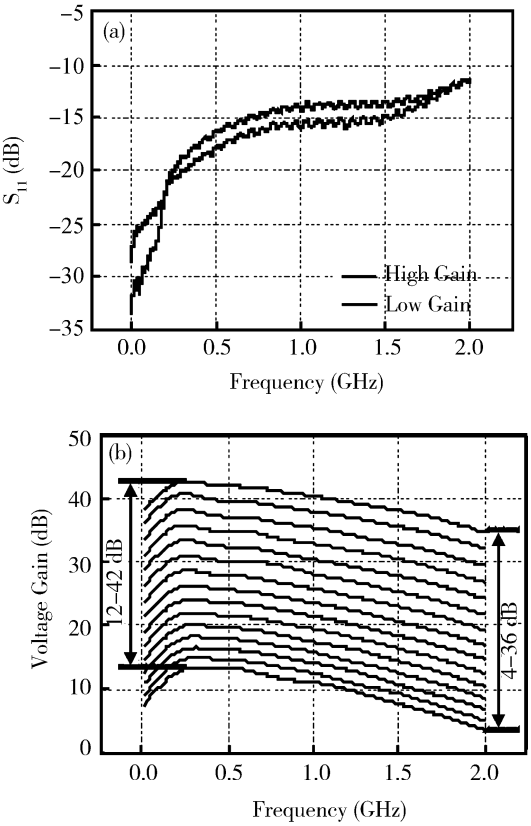

Fig. 7. (a) Measured S_{11} versus frequency. (b) Measured voltage gain versus frequency.

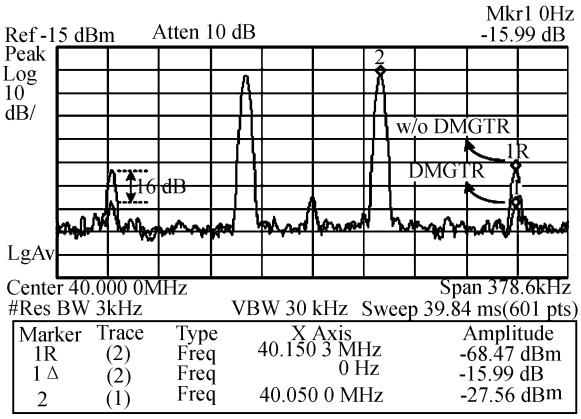

Fig. 8. Measured result of the two-tone intermodulation test of the mixer. The conventional Gilbert mixer and the proposed DMGTR mixer are compared. Measured frequency is 1 GHz.

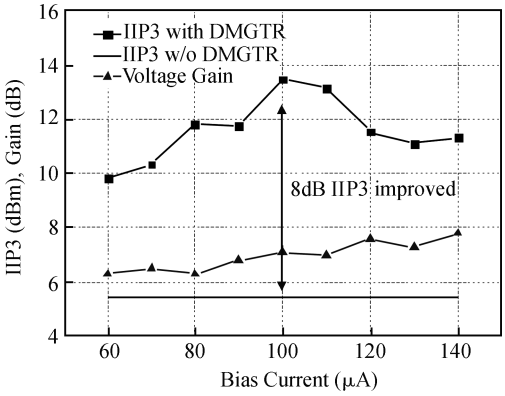

Fig. 9. Measured IIP3 versus bias current of pseudo-differential transistors of the mixer. Measured frequency is 1 GHz.

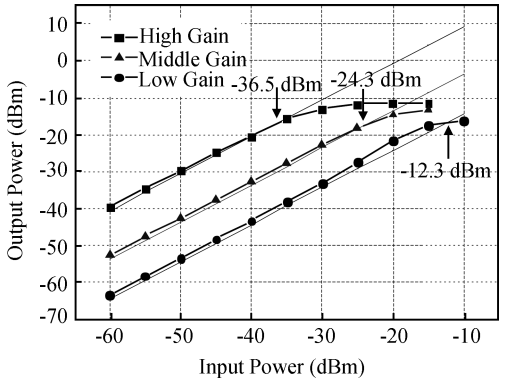

Fig. 10. Measured P_{1dB} at high gain, middle gain and low gain, at 2 GHz.

DMGTR mixer. The input power is –15 dBm and the frequency is 1 GHz. Without significantly increasing the power and NF, the DMGTR mixer decreases the IM_3 up to 16 dB, thus, the corresponding IIP3 is improved by 8 dB. Figure 9 shows the measured result of IIP3 versus the bias current of pseudo-differential transistors in the DMGTR mixer. A 60–140 μA bias current is achieved by 4 controlling bits. At least 4.4 dB improvement is obtained by IIP3. It shows a good robustness to covering the possible mass production variations. The output resistance of the mixer is 300 Ω. To convert the measured power gain (with 50 Ω load) to voltage gain (differential output to differential input), approximately 19 dB needs to be added, since the mixer is followed by an on-chip VGA with a voltage-type input. In this way, the voltage gain of the mixer is about 7 dB.

The input-referred 1 dB gain compression point (P_{1dB}) of the RF front-end is shown in Fig. 10. At a frequency of 2 GHz, the P_{1dB} is –36.5 dBm at the high-gain mode, –24.3 dBm at the middle-gain mode, and –12.3 dBm at the low-gain mode. The test results show that the linearity of the proposed RF front-end

Table 1. Performance summary and comparison.

Parameter	ISSCC, 2009[8]	ISSCC, 2008[9]	This work
Frequency (GHz)	0.4–0.9	0.5–7	0.2–2
S_{11} (dB)	<-10[a)]	<-10	<-11.4
Gain (dB)	34.4 ± 0.2 @ 0.4–0.9 GHz	19 ± 0.5 @ 0.5–7 GHz	39 ± 3 @ 200kHz–2 GHz
Gain range (dB)	N/A	N/A	30
DSB NF (dB)	3.5–4.4	4.5–5.5	3.1–6.1
IIP3 (dBm)	3.2–4.2	–3	–4.7 to 0.2
P_{1dB} (dBm)	–22 @ 800 MHz	N/A	–36.5 to –12.3 @ 2 GHz
Die area (mm^2) (excluding PADs)	0.7	0.01[b)]	0.63
Power consumption (mA)	33 @ 1.2 V	16 @ 1.2 V[b)]	20 @ 1.8 V[c)]
Technology	65-nm CMOS	65-nm CMOS	0.18-μm CMOS

[a)] $S_{11}<-10$ bandwidth is up to 6 GHz.
[b)] Active core area excludes the bias and LO generation and buffers.
[c)] The power consumption includes the LO buffers and output test buffers.

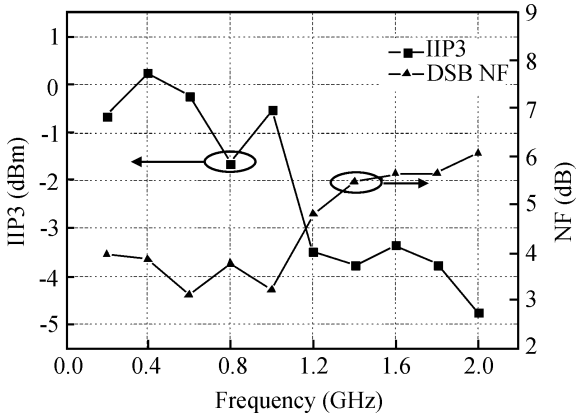

Fig. 11. Measured IIP3 and NF versus frequency.

is high enough to meet the demands of most analog and digital broadcasting standards.

The measured IIP3 and NF are shown in Fig. 11. The input power is -30 dBm, the measured IIP3 is -4.7 to 0.2 dBm from 200 kHz to 2 GHz in 1 MHz frequency span. The measured DSB NF is 3.1–6.1 dB in the whole range from 10 MHz to 2 GHz, and the NF lower than 10 MHz is not tested due to the limitations of the noise figure analyzer Agilent N8975A.

Table 1 presents a performance comparison with recent reported wideband RF frond-ends for wideband applications. Compared with Refs. [8, 9], the proposed design is based on a cheaper 0.18-μm CMOS process but achieves comparable performance in voltage gain, DSB NF and IP_3. The die area and current consumption are smaller than Ref. [8]. The reason why the bandwidth is smaller than in Refs. [8, 9] is that the f_T of the 0.18-μm CMOS process is much lower than that of the 65-nm CMOS process.

5. Conclusion

A high performance RF front-end is proposed for digital radio broadcasting in 200 kHz–2 GHz. To increase the sensitivity and linearity of the RF front-end in such a wideband frequency range, noise-canceling and DMGTR technology is employed. The dB-in-linear VGA exploits a single PMOS to achieve exponential gain control. The S_{11} of the RF front-end is lower than –11.4 dB. The variable gain range is 39 ± 3 dB within 200 kHz–2 GHz. The DSB NF at maximum gain is 3.1–6.1 dB. The IIP3 at middle gain is -4.7 to 0.2 dBm. The performance of the RF front-end meets the requirements of DRM/DAB/DVB-H applications.

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