A low-power CMOS frequency synthesizer for GPS receivers*

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Abstract: A low-power frequency synthesizer for GPS/Galileo L1/E1 band receivers implemented in a 0.18 μm CMOS process is introduced. By adding clock-controlled transistors at latch outputs to reduce the time constant at sensing time, the working frequency of the high-speed source-coupled logic prescaler supplying quadrature local oscillator signals has been increased, compared with traditional prescalers. Measurement results show that this synthesizer achieves an in-band phase noise of –87 dBc/Hz at 15 kHz offset, with spurs less than –65 dBc. The whole synthesizer consumes 6 mA in the case of a 1.8 V supply, and its core area is 0.6 mm^2.

Key words: frequency synthesizer; GPS; CMOS; PLL; source-coupled logic; prescaler
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1. Introduction

Up to now, GPS (global positioning system) has been the only satellite navigation system supplying services; however, other GNSS (global navigation satellite systems) will soon be available, for example, Galileo, GLONASS and Compass-Ⅱ [1,2]. The GPS L1 band and Galileo E1 band both center at 1575.42 MHz; therefore, dual-mode L1-band RF receivers for the GPS and Galileo signals can share the same RF front-end.

Additionally, there is a great trend for GPS receivers to be incorporated into cell phones, other communication standards devices, and portable hand-held modules. Thus, there is a strong motivation for GPS receivers to offer good performance with low power. With the rapid performance improvements of CMOS technology and the increasing demands for lower cost, higher level of integration and SoC, interest in CMOS GPS receivers has increased and several successful results have been reported[3−5].

This paper presents a low-power PLL-based synthesizer from a dual-mode GPS/Galileo L1/E1-band receiver system perspective, a detailed circuit description, and experimental results.

2. Design of the synthesizer

2.1. Configuration of the synthesizer

With a tradeoff between integration, performance, and power, a low-IF architecture for the dual-mode GPS/Galileo L1/E1-band receiver is selected. Therefore, an agile PLL-based synthesizer for this receiver should provide quadrature LO signals. There are three kinds of methods to generate quadrature LO signals, and the most popular is the generation of quadrature LO signals by a divide-by-2 prescaler, for the following reasons[6]. First of all, the interference to RF front-end can be diminished compared to a quadrature VCO. Secondly, the phase noise of the output of the prescaler is 6 dB lower than the case of a quadrature VCO supplying quadrature signals as shown in Fig. 1, thus the critical phase noise demand of the VCO can be alleviated. The last is that the number of inductors is smaller than that of the quadrature VCO, so the area of the chip is smaller.

According to a phase noise analysis in the linear phase domain, the relationship between the output phase noise of the prescaler and the VCO can be obtained as

$$\Theta_{\rm div} = \left(\frac{1}{2}\right)^2 \Theta_{\rm VCO}. \tag{1}$$

The simulation result of the phase noise can be seen in Fig. 1. The phase noise of the output of the prescaler is almost 6 dB lower than that of the VCO output below 4 MHz offset.

A block diagram of the proposed PLL-based synthesizer is shown in Fig. 2. A novel high-speed divide-by-2 source-coupled logic (SCL) prescaler is proposed to generate quadra-

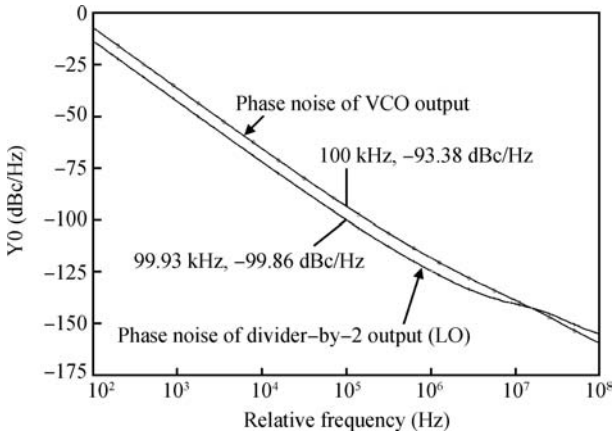

Fig. 1. Phase noise of the output of the prescaler and the VCO.

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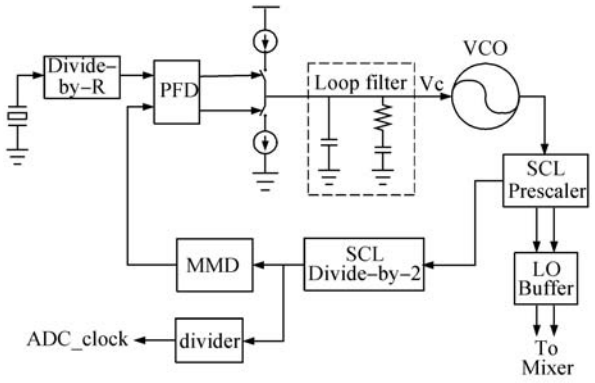

Fig. 2. Block diagram of the proposed synthesizer.

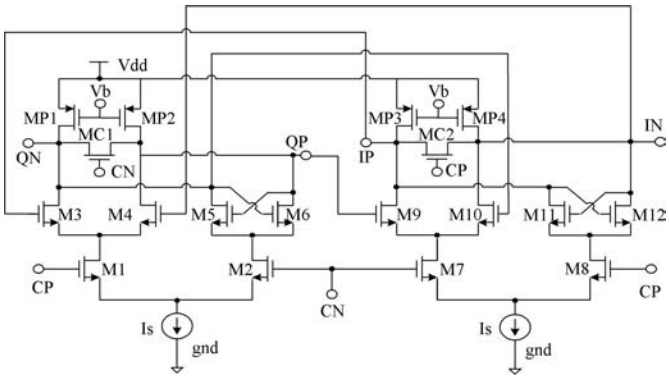

Fig. 3. Proposed prescaler based on a novel latch.

ture LO signals. A wide tuning range VCO ensures that it can work at all process corners without capacitor or inductor switches, which run at double LO frequency, and a pulse-swallow divider is used for the multi-modulus divider (MMD) in the feedback loop. A gain-boosting charge pump ensures a small mismatch between the pump current and the spur.

2.2. High-speed prescaler

The high-speed prescaler used most is a source-coupled logic prescaler which is induced from an ECL logic divider, because of its ultra-wide working range and medium power consumption. To get a higher working speed, the load resistance should be smaller, but a large amplitude needs a large load resistance. To overcome this conflict, a so-called dynamic load architecture has been reported, which uses transistors controlled by an input clock as the load to reduce the charging and discharging time[7, 8]. But this will cause a fatal problem in that the change of load destroys the circuit's quiescent operation stability, so the operation point will also be changed. As a result, the circuit will work at all process corners.

The proposed prescaler based on a new latch with inverted-clock-controlled transistors at the outputs of each latch is proposed to solve this problem, as shown in Fig. 3. To accurately illustrate the performance enhancement of the proposed latch architecture with clock-controlled transistors, a small signal model of this proposed latch has been developed as shown in Fig. 4. Usually, the speed of the current mode logic latch stringently depends on the speed of the sensing logic, so the small signal model is set to sensing mode, and only the semi-circuit

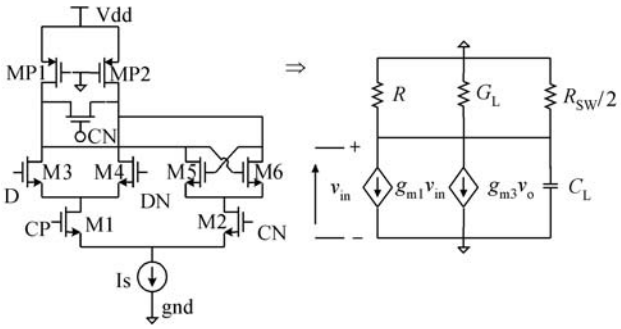

Fig. 4. Equivalent small signal model of the proposed latch.

is under analysis[7]. The transfer function of the proposed latch is derived from Fig. 4,

$$A_V = \frac{v_o}{v_{in}} = -\frac{g_{m3}}{SC_L - g_{m5} + g_{ds3} + g_{ds5} + \dfrac{1}{R} + \dfrac{2}{R_{SW}}}, \quad (2)$$

where g_{m3} is the trans-conductance of the sensing pair (M3, M4), g_{m5} the trans-conductance of the latching pair (M5, M6). C_L is the sum of the load capacitance and the output node's total parasitic capacitance and R, R_{SW} are the equivalent resistance of the load transistor and the clock-controlled transistor, respectively.

When the gain of the small transfer function is set to 1, the maximum output operation frequency of the proposed flip-flop is

$$f_{out,\,max} = \frac{\sqrt{g_{m3}^2 - \left(g_{m5} - g_{ds3} - g_{ds5} - \dfrac{1}{R} - \dfrac{2}{R_{SW}}\right)^2}}{2\pi C_L}. \quad (3)$$

From Eq. (3) the negative trans-conductance of the cross-coupled pair (M5 and M6) is used to cancel the load resistance, clock-controlled transistor's equivalent resistance and G_L. If the cancellation is set perfectly, the maximum output operation frequency of the proposed flip-flop equals

$$f_{max} = 2f_{out,\,max} = 2 \times \frac{g_{m3,\,avg}}{2\pi C_L} = \frac{g_{m3,\,max}}{2\pi C_L}. \quad (4)$$

In this synthesizer, the whole prescaler consumes 2.5 mA (with the LO buffer consuming 1.2 mA), and it can work up to 6.9 GHz in post-simulation, which is 30% higher than a traditional SCL prescaler.

2.3. Multi-modulus divider

To accommodate all the reference between 1 and 40 MHz, the modulus of the multi-modulus divider (MMD) ranges from 9 to 2047. To save power, the multi-modulus divider, utilizing the asynchronous pulse-swallow technique and the division core circuit recycling technique, consists of a quad-modulus divider (whose division modulus can be selected by the signal MC) and two synchronous dividers[9]. A block diagram of the multi-modulus divider is shown in Fig. 5. All the D flip-flops in the MMD are based upon the TSPC. The division core circuit recycling technique is that the master divider and the slave

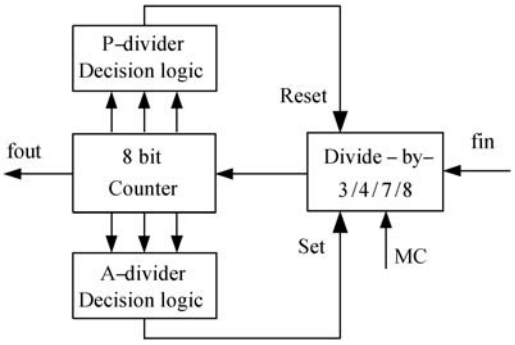

Fig. 5. Configuration of the multi-modulus divider.

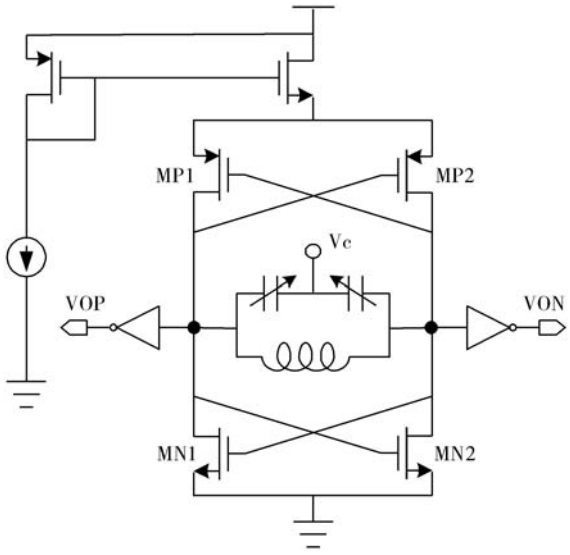

Fig. 6. Complementary cross-coupled LC VCO.

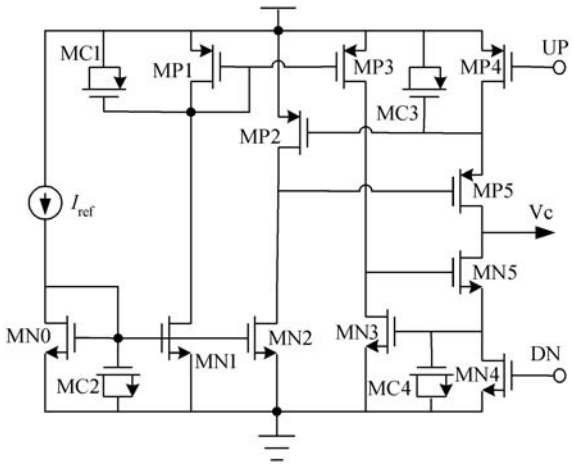

Fig. 7. Improved gain-boosting charge-pump.

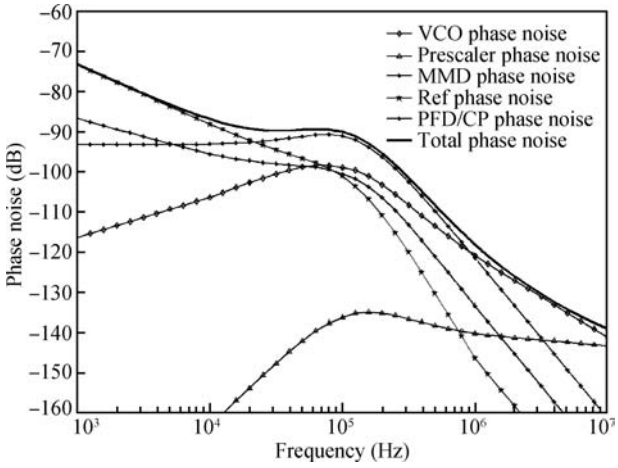

Fig. 8. Predicted total phase noise at the synthesizer output.

divider share the same core division circuit, but their decision circuits are separate; as a result, the area and power reduce by half.

2.4. Voltage controlled oscillator and charge pump

Another challenge block of the PLL is the VCO. Among the various configurations of the oscillator, a differential complementary pair cross-coupled LC CMOS oscillator is chosen for low phase-noise performance with low power consumption. The VCO oscillation frequency is set to be twice the LO signal frequency applied to the mixer ports. Accumulation MOS (AMOS) is preferred to others varactors for low voltage applications, since AMOS has much larger tuning range, usually $C_{max}/C_{min} > 2.5$. In practice, the Q of the AMOS varactor is better than that of a diode varactor, which is an important parameter for the VCO. A larger Q will make the phase noise lower and the output swing larger. Unfortunately, due to its large capacitance variation, the capacitance varies with the output voltage[10]. A simplified schematic of the proposed VCO is shown in Fig. 6, in which a pMOS is used as a tail current transistor for lower phase noise.

CMOS CPs usually have up and down switches made of pMOS and nMOS, respectively. In this case, a current mismatch occurs due to the difference between the drain–source voltages of the pMOS and nMOS when dumping the charge to the loop filter. The source-switching charge-pump has a shorter switching time, which, utilizing the gain-boosting technique, is shown in Fig. 7. The pump-up core consists of MN2, MP2, MP4, MP5, and the pump-down core consists of MN3, MP3, MN4, and MN5. The gain-boosting technique forces the drain voltage to follow the gate voltage of MP2, and the same occurs at MN3, MP5, MN5; as a result, the mismatch between the pump-up current and pump-down current is very small ($<$ 1% in simulation), and the spur at the output of the synthesizer is also small[11].

3. Experimental results

To accurately predict the performance of this synthesizer, a phase-domain model is introduced to calculate the total phase noise at the synthesizer output. The phase noise of the MMD, reference source, PFD, and charge pump all can be represented by a phase noise source at the input of the PFD, because the functions of their phase noise to the phase noise at the synthesizer output are almost the same, differing only by a constant factor. The predicted total phase noise at the synthesizer output can be seen in Fig. 8. The in-band noise of the synthesizer's output is less than -90 dBc/Hz and the phase noise at 1 MHz offset is about -118 dBc/Hz, which is lower than the GPS and

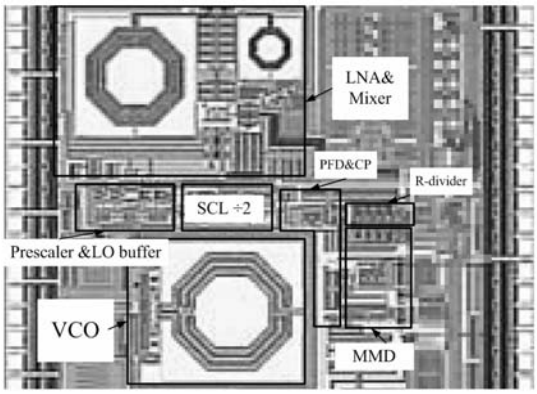

Fig. 9. Die photograph of the proposed synthesizer.

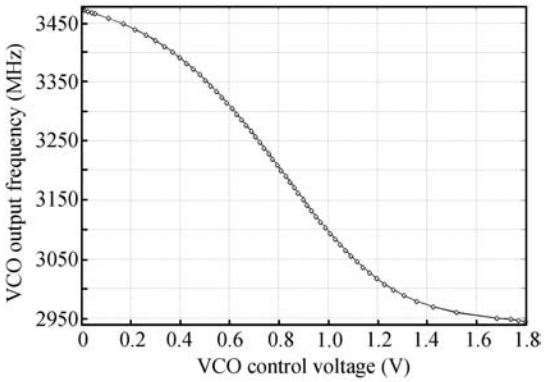

Fig. 10. Measured VCO tuning range.

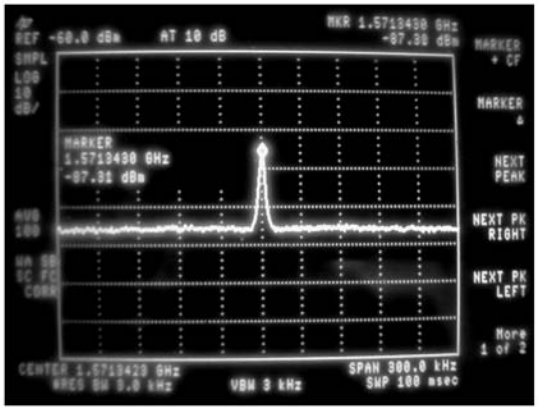

Fig. 11. LO output power spectrum.

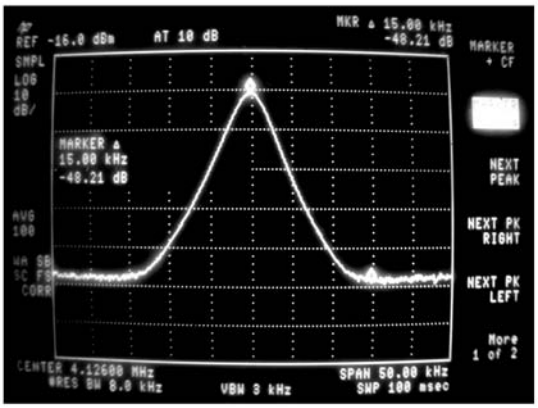

Fig. 12. IF signal power spectrum after mixing.

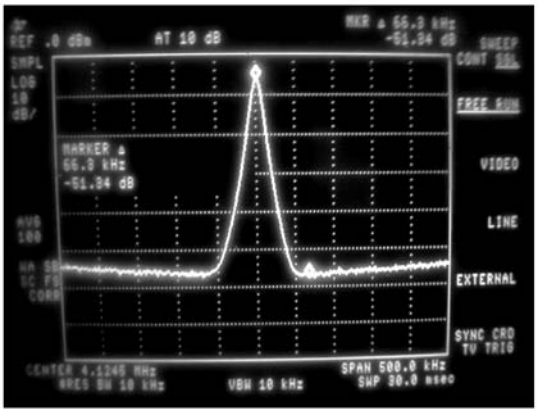

Fig. 13. IF signal.

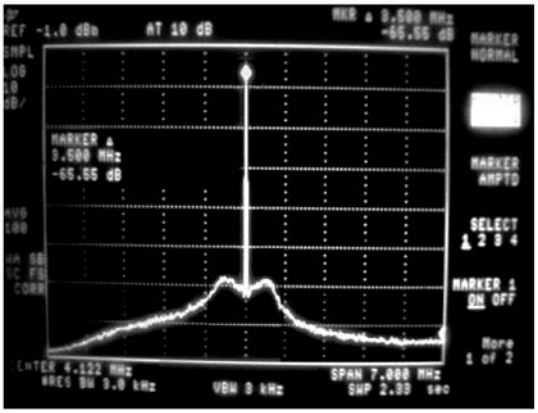

Fig. 14. IF signal with 7 MHz span.

Galileo system requirement.

The proposed frequency synthesizer has been manufactured in a 0.18 μm CMOS process. For test convenience, a low noise amplifier (LNA), a down-conversion mixer and a low intermediate-frequency (LIF) driver are also integrated with the synthesizer in the same chip, a die photograph of which is shown in Fig. 9. The whole frequency synthesizer including LO buffer and reference frequency divider, occupies 0.6 mm^2. Under a regular working environment, the proposed synthesizer consumes 6 mA under a 1.8 V power supply including the LO buffer to the mixer.

The VCO's frequency varies from 2.935 to 3.462 GHz covering all process deviations while the control voltage varies from 0 to 1.8 V as shown in Fig. 10, which is measured from the buffer output by fixing the feedback divider division and changing the input reference frequency when the synthesizer is in a closed loop. It is obvious that the tuning curve of the VCO is almost linear between 0.3 and 1.3 V.

In the down-conversion mixer, the quadrature output of the frequency synthesizer generated by the high-speed SCL prescaler mixes with the low phase noise RF signal generated by a low phase noise RF signal generator. The LO power spec-

Table 1. Performance comparison with published frequency synthesizers.

Parameter	Ref. [2]	Ref. [12]*	Ref. [13]	Ref. [14] *	This work
Process	0.18 μm CMOS	0.18 μm SiGe	0.18 μm CMOS	0.13 μm CMOS	0.18 μm CMOS
V_{dd} (V)	1.8	1.8	1.6–1.8	1.2	1.8
Frequency (GHz)	1.571	1.571	1.571	1.58	1.571
Phase noise (dBc/Hz)	−81 @ 70 kHz −120 @ 1 MHz	−90 (in-band) −108 @ 1 MHz	−82 (in-band) −112 @ 1 MHz	−70 @ 100 kHz −109 @ 1 MHz	−87 (in-band) −118 @ 1 MHz (simulated)
Spur (dBc)	–	−55	−65	–	< −65
Power (mW)	41.4[#]	3.96	> 7.2	1.2	10.8 (including LO buffer)

Total receiver, * Quadrature VCO, – Not mentioned.

trum is shown in Fig. 11, and there is no significant spur in the 100 MHz span. The phase noise of the proposed frequency synthesizer can be measured at IF output. Figure 12 shows the measured IF signal power spectrum, and the corresponding phase noise of the proposed frequency synthesizer is better than −87 dBc at 15 kHz offset, and −91.3 dBc/Hz at 66 kHz offset as shown in Fig. 13. The reference spur is less than –65 dBc as shown in Fig. 14.

A performance comparison between the proposed PLL and other related frequency synthesizers is listed in Table 1. Although the power of the synthesizers in Refs. [12–14] is smaller than that in this work, the phase noise and spur are less attractive. Additionally, the synthesizers in Refs. [12, 14] were manufactured with expensive technology, and the power of that in Ref. [13] is not including the LO generator (high speed divide-by-2) and LO buffers to the quadrature mixer. The phase noise at 1 MHz offset in Ref. [2] is superior to ours, but its in-band phase noise is worse, and the power and area of the whole RF receiver are larger to some extent.

4. Conclusion

A low-power CMOS integer-N frequency synthesizer for GPS/Galileo L1/E1 band receivers is proposed in this paper, and it has been manufactured in standard 0.18 μm CMOS. By introducing clock-controlled transistors at latch outputs to reduce the time constant at sensing time, the maximum working frequency of the high-speed source-coupled logic (SCL) prescaler has been increased. The complementary cross-coupled LC VCO has a wide working range with low current consumption. The gain-boosting charge pump makes the mismatch between pump-up and pump-down current smaller, thus giving a smaller spur. The whole synthesizer consumes 6 mA under a 1.8 V supply and it has been successfully applied to dual-mode GPS/Galileo L1/E1 band receivers.

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