Sigma–delta modulator modeling analysis and design

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Abstract: This paper introduces a new method for SC sigma–delta modulator modeling. It studies the integrator's different equivalent circuits in the integrating and sampling phases. This model uses the OP-AMP input pair's tail current (I_0) and overdrive voltage (v_{on}) as variables. The modulator's static and dynamic errors are analyzed. A group of optimized I_0 and v_{on} for maximum SNR and power × area ratio can be obtained through this model. As examples, a MASH21 modulator for digital audio and a second order modulator for RFID baseband are implemented and tested, and they can achieve 91 dB and 72 dB respectively, which verifies the modeling and design criteria.

Key words: sigma-delta; modeling; transient behavior; optimization
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1. Introduction

The rapid development of the IC process has dramatically improved digital chip density and calculation capability, and it also leads to a higher requirement for data converters. Over-sampling and noise shaping techniques can reduce in-band quantization noise in sigma–delta[1] data converters. Now sigma–delta converters have been extensively applied in low-frequency and mid-frequency fields[2], and they are also being used more and more in many low power multi-mode communication systems[3].

Unlike a Nyquist ADC, a sigma–delta ADC incorporates memory elements in its structure. This property destroys the one-to-one relation between input and output samples. It needs a large amount of transient data to evaluate its accuracy, either in the time domain or the frequency domain. With the modulator's transient model, time consuming transistor simulation can be replaced by fast MATLAB model simulation, and provides advice for circuit design.

This paper studies the integrator's different equivalent circuits in the integrating and sampling phases, and develops two transient models for both phases respectively. The proposed models use I_0 and v_{on} as modeling variables. The modulator's static and dynamic errors for every phase can be analyzed with this model and a group of optimized I_0 and v_{on} for maximum SNR and power/area ratio can also be obtained.

2. Modulator transient modeling

The integrator is the sigma–delta modulator's key block; it alternately works in the integrating and sampling phases under the control of a non-overlap clock: Ph1 and Ph2. A schematic of the integrator is shown in Fig. 1.

Cpin and Cpout are parasitic capacitors in the OP-AMP's input and output node, V_{os} is the offset voltage, and Cs2 is the next stage's sampling capacitor. Here, a non-ideal OP-AMP is modeled with a single pole system, shown in Fig. 2.

The integrator's state switching in the integrating and sampling phases is shown in Fig. 3.

At the beginning of state switching, the OP-AMP input voltage's initial value can be obtained through the charge conservation principle[4]. As expressed in Eqs. (1) and (2), the initial values are determined by the integrator's input voltage and capacitor ratio.

$$V_{a,i}(0) = -V_{ins}[n-1]C_{s1}(C_{i1} + C_{pout})/(C_{eq,i}C_{i1}), \quad (1)$$

$$V_{a,s}(0) = -V_{oi,i}[n]C_{s2}/C_{eq,s}. \quad (2)$$

As is known, an integrator has different equivalent circuits in different phases. This paper uses I_0 and v_{on} as modeling variables but not the OP-AMP's GBW and SR[5]. As will be

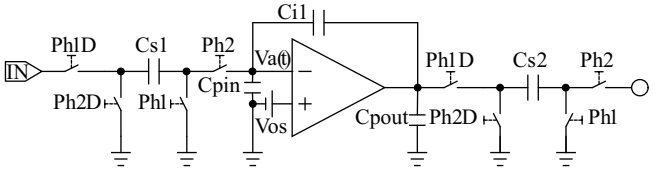

Fig. 1. SC integrator.

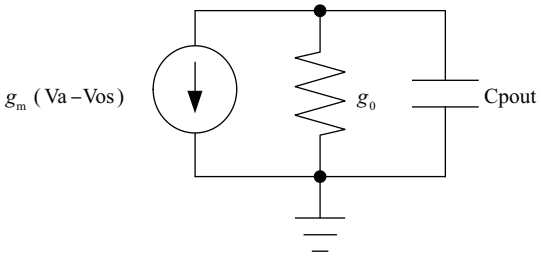

Fig. 2. Single pole system for the OP-AMP.

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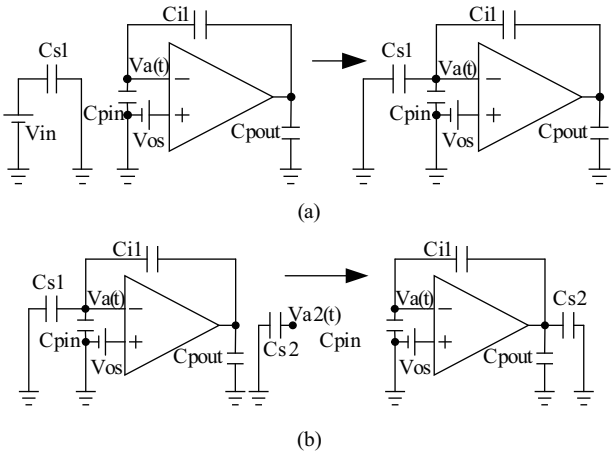


Fig. 3. (a) State switching in integrating phase. (b) State switching in sampling phase.

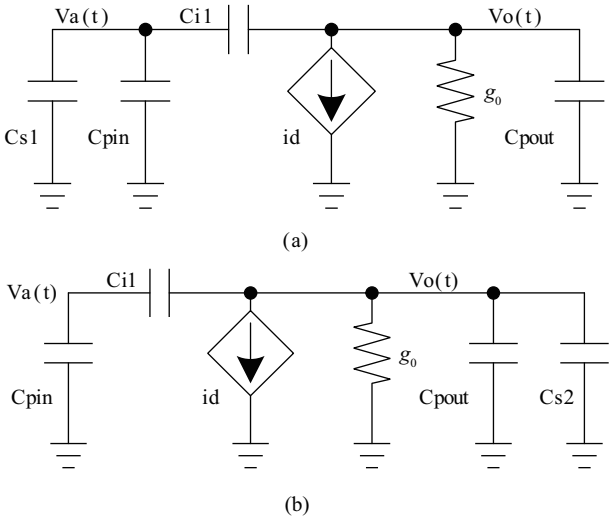


Fig. 4. (a) Integrating phase equivalent circuit. (b) Sampling phase equivalent circuit.

seen, the OP-AMP's GBW and SR change with phase switching, so the proposed model is much closer to a real circuit. The integrator's small signal equivalent circuits in both phases are shown in Fig. 4.

Equations (1) and (2) show that the OP-AMP's input voltage will changes in a large scale. Here it is assumed that the OP-AMP's conductance (g_m) remains constant, and when $V_a(t)$ is over v_{on}, the OP-AMP will enter SR-limited settling[6]. I_0 and v_{on} have a relationship, expressed as Eq. (3).

$$I_0 = g_m v_{on}. \tag{3}$$

The controlled current source in Fig. 4 can be expressed as Eqs. (4) and (5).

$$i_d = g_m[V_a(t) - V_{os}], \quad |V_a(0) - V_{os}| \leqslant V_{on}, \tag{4}$$
$$i_d = \mathrm{sgn}(V_a(0) - V_{os})I_0, \quad |V_a(0) - V_{os}| > V_{on}. \tag{5}$$

According to the KCL principle, differential equations about the OP-AMP's input and output nodes can be obtained.

Table 1. Integrator transient model parameters.

Parameter	Value
F_{dci}	$C_{il}/(C_{s1} + C_{pin} + C_{i1})$
F_{dcs}	$C_{i1}/(C_{pin} + C_{il})$
$V_{oi,i}[n]$	$V_{oi,s}[n-1] + V_{ins}[n-1]$
$V_{oi,s}[n]$	$V_{oi,i}[n]$
C_{eqi}	$C_{s1}+C_{pin}+C_{pout}+(C_{s1}+C_{pin})C_{pout}/C_{i1}$
C_{eqs}	$C_{s2}+C_{pin}+C_{pout}+(C_{s2}+C_{pin})C_{pout}/C_{i1}$

Table 2. Coefficients in the linear and SR-limited regions.

Parameter	Value
$a_{1,lin}$	$-\mathrm{GBW}(1 + 1/(A_0F_{dc}))$
$a_{1,sr}$	$-\mathrm{GBW}/F_{dc}$
$a_{2,lin}$	$\mathrm{GBW}(V_{os} - V_{oi}/A_0)$
$a_{2,sr}$	$\mathrm{GBW}[\mathrm{sgn}(V_a(0) - C_{os})V_{on} - V_{oi}/A_0]$

These nodes' transient expressions can be obtained from these equations[4], which are expressed as Eqs. (6) and (7).

$$V_o(t) = V_a(t)F_{dc} + V_{oi}, \tag{6}$$
$$V_a(t) = -(a_2/a_1)[1 - \exp(a_1 t)] + V_a(0)\exp(a_1 t). \tag{7}$$

Here F_{dc} is the DC ratio between the input and output node, V_{oi} is the integrator's ideal output, and C_{eq} is the OP-AMP's equivalent capacitor load. These parameters are listed in Table 1.

a_1 and a_2 in Eq. (7) have different values when the OP-AMP is in the linear region and the SR-limited region as expressed in Table 2.

GBW and A_0 can be expressed as below:

$$\mathrm{GBW} = g_m/C_{eq}, \quad A_0 = g_m/g_0. \tag{8}$$

By now, the SC integrator's transient model has been developed. The proposed model has different expressions in integrating and sampling, and also has a difference in the linear region and the SR-limited region. It can be seen that the integrator's transient response is mainly determined by the OP-AMP's I_0 and v_{on}. In the next part, the integrator's non-idealities caused by finite I_0 and v_{on} will be analyzed.

3. Integrator design analysis

The integrator's non-ideality can be divided into two categories: static non-ideal and dynamic non-ideal. When GBW is infinite, static non-ideal can be expressed as below.

$$V_o(t) = \frac{A_0F_{dc}}{1 + A_0F_{dc}}V_{oi} + \frac{A_0}{1 + A_0F_{dc}}V_{os}. \tag{9}$$

The first part in Eq. (9) indicates the integrator's leakage and gain error caused by A_0. The second part indicates offset amplification. Static non-ideal will cause a pole shift in the integrator trans-function, and it has less impact on the single loop modulator. As Figure 5 shows, the SNR drop is only 6 dB even when A_0 is 50 dB. But static non-ideal impacts on MASH modulators are much more severe[7].

The first part of Eq. (6) is the integrator's dynamic non-ideal; when static non-ideal is ignored, the dynamic ones in the integrating and sampling phases can be written as Eqs. (10) and (11).

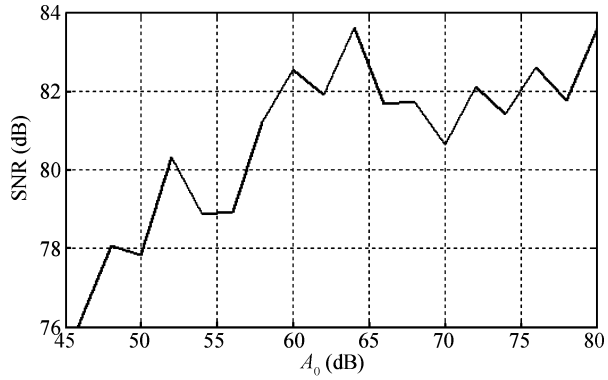


Fig. 5. SNR versus A_0 of RFID ADC.

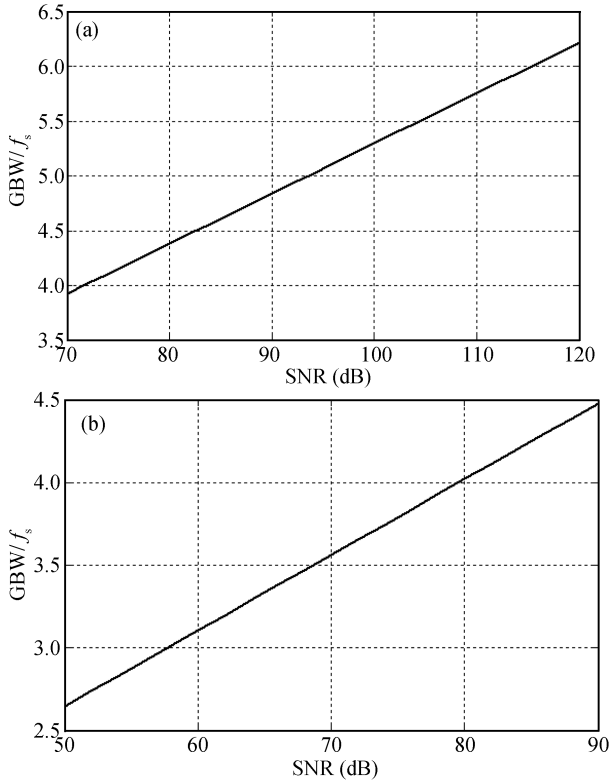


Fig. 6. (a) GBW versus SNR of audio ADC. (b) GBW versus SNR of RF ADC.

$$\frac{1}{F_{dc}}\frac{C_{s1}}{C_{eqi}}\frac{C_{i1}+C_{pout}}{C_{i1}}\exp(a_1 T_s/2), \tag{10}$$

$$\frac{1}{F_{dc}}\frac{C_{s2}}{C_{eqs}}\exp(a_1 T_s/2). \tag{11}$$

It can be seen that dynamic non-ideal is mainly caused by finite GBW. If only dynamic non-ideal is considered, the relationship between SNR and GBW (in the integrating phase) in an audio ADC and RF ADC can be obtained from this model; they are shown in Fig. 6.

The integrator's non-ideal can be ignored when its dynamic error is less than 0.5 LSB[8]. Figure 6 shows that the OP-AMP's GBW should be larger than $5.8 f_s$ if the audio ADC's SNR wants to be 110 dB. Also, if the RF ADC's SNR wants to be

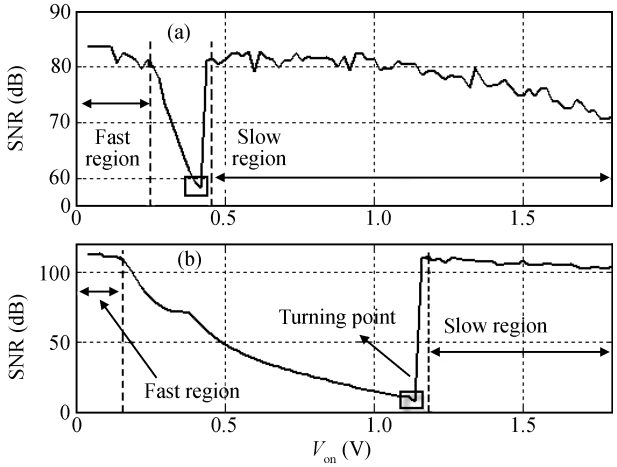


Fig. 7. v_{on} sweep versus SNR. (a) At RF ADC. (b) At Audio ADC.

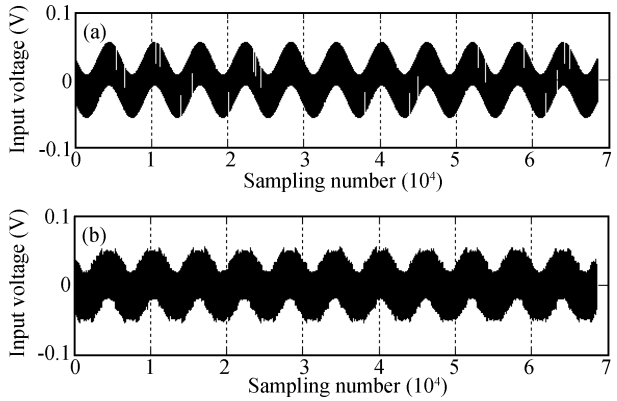


Fig. 8. OP-AMP input voltage. (a) Opamp1. (b) Opmp2.

80 dB, the OP-AMP's GBW should be larger than $4.6 f_s$. (Here only the first OP-AMP is considered.)

The OP-AMP input pair has three design variables: I_0, g_m and v_{on}. The third one can be calculated from any of the other two. Here I_0 is fixed and v_{on} is swept from 0 to 1.8 V. The sweep results of the audio ADC and RF ADC are shown in Fig. 7.

It can be seen that the modulator can achieve normal SNR in two different regions: the fast region and the slow region[8]. When v_{on} is small, the modulator will be in the fast region, and SR-limited settling will happen in the beginning, but fast linear settling can compensate the nonlinearity. When v_{on} is large enough, the modulator will be in the slow region. SR-limited settling will never happen, and no harmonic distortion will be introduced under the ideal condition.

When the modulator is in the slow region, the OP-AMP's input voltage is always unable to return to zero because of low GBW, as shown in Fig. 8. In a real circuit, g_m and A_0 cannot remain constant as assumed. Nonlinear gm and A_0 will introduce large harmonics and make the modulator's SNR drop dramatically. The OP-AMP's large v_{on} also leads to a narrow common mode range and makes it unable to work under low supply voltage. So, the modulator is always designed to work in the fast region.

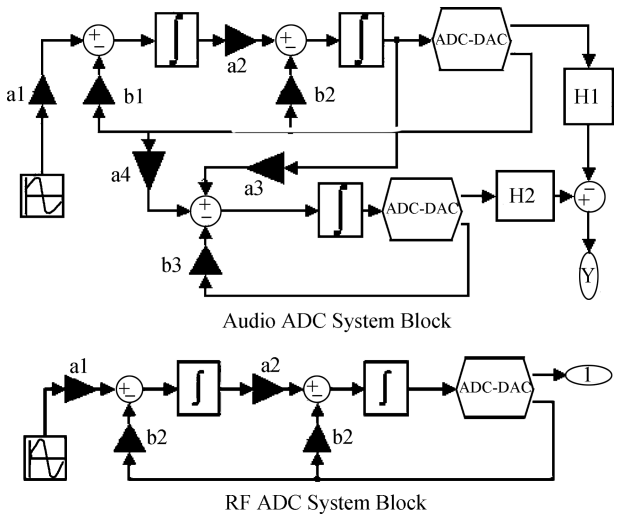


Fig. 9. Audio ADC and RF ADC.

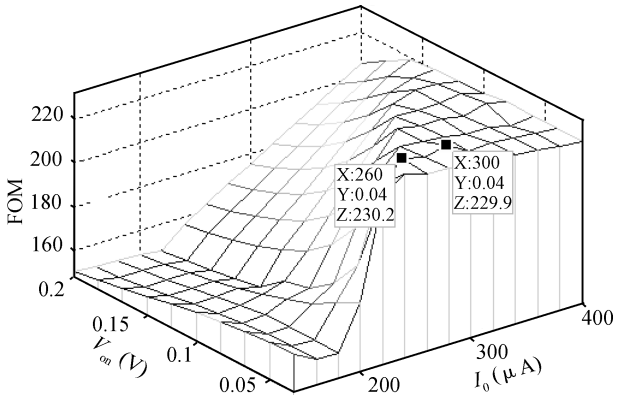


Fig. 10. FOM sweep for audio ADC.

4. Modulator design and test

In this part, a MASH21 modulator for digital audio and a second order modulator for RFID reader baseband will be designed to verify the proposed model and analysis; they are shown in Fig. 9.

Here figures-of-merit (FOM) are defined to evaluate the modulator's efficiency. This indicates the ratio between the modulator's SNR and its power area product, and its definition is expressed as below:

$$\mathrm{FOM} = \mathrm{dB}\{\mathrm{SNR}/[I_0(W/L)]\} = \mathrm{dB}(\mathrm{SNR}\cdot v_{\mathrm{on}}/I_0^2). \quad (12)$$

When the integrator works in the fast region, a 3D curve between FOM I_0 and v_{on} can be obtained. Figure 10 shows the FOM of the audio ADC.

It can see that the FOM reaches its peak when $v_{\mathrm{on}} = 40$ mV and $I_0 = 260$ μA. But this point is at the edge of the ramp, so $v_{\mathrm{on}} = 40$ mV and $I_0 = 300$ μA are chosen to keep the design margin. Detailed design specifications for the audio ADC and RF ADC are listed in Table 3. (Here only the first OP-AMP is listed.)

The two modulators are implemented with TSMC18MMRF technology, and their output PSD is shown in Fig. 11 together with the simulation results. Test

Table 3. Design specifications.

SPECs	Audio ADC	RF ADC
A_0 (dB)	80	65
I_0 (μ A)	300	200
V_{on} (mV)	40	60
Jitter (ns)	10	1
Comp hysteresis (mV)	30	20
C_{s1} (pF)	25.2	0.57
R_{on} (k Ω)	1.5	2
OP swing (V)	0.38–1.42	0.3–1.5
BW (kHz)	25	250
SNDR (dB)	98.7	77.5

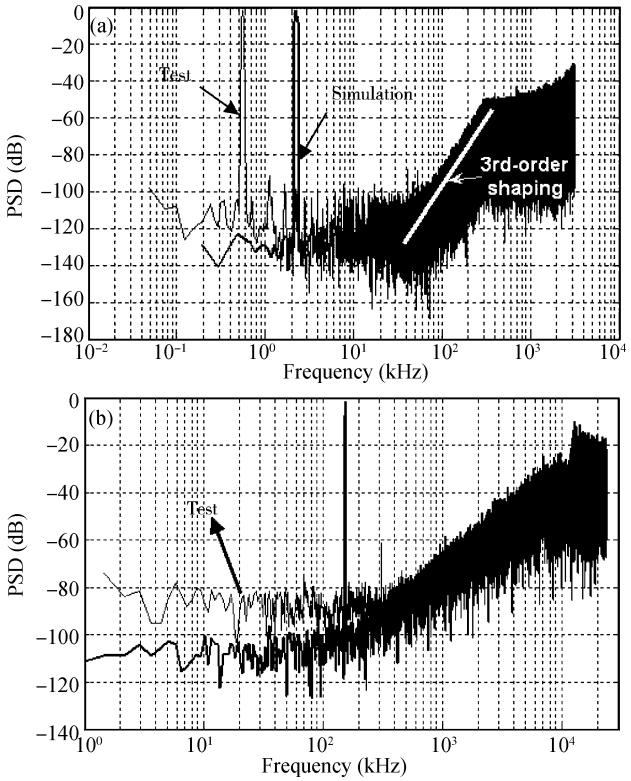


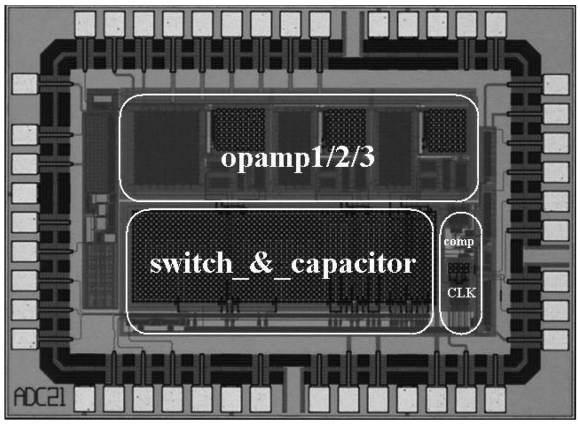
Fig. 11. (a) Output PSD for audio ADC. (b) Output PSD for RF ADC.

results show that the audio ADC's SNR is 91 dB and the RF ADC's SNR is 72 dB; both modulators attain the desired requirement, and the test results and model simulation results show good agreement.

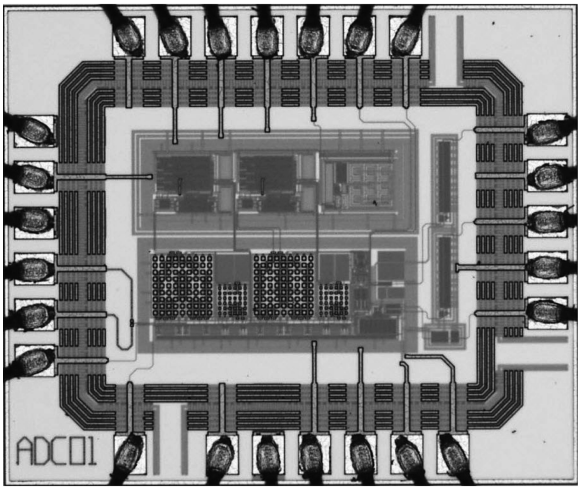
Die photos of the modulators are shown in Fig. 12, and their detailed specifications are listed in Table 4.

5. Conclusion

This paper proposes a new behavioral model for an SC integrator; the proposed model uses I_0 and v_{on} as modeling variables, and it describes different transient settling in the integrating and sampling phases. Static and dynamic non-ideals are studied with the proposed model and optimized design specifications are developed for an audio MASH21 modulator and a second order RF baseband modulator. The chip test results and modeling simulation results show good agreement.



(a)



(b)

Fig. 12. (a) Die photo for audio ADC. (b) Die photo for RF ADC.

Table 4. Modulator specifications.

Modulator	Audio	RF
Peak SNDR (dB)	91	72
Sampling rate (MHz)	6.4	48
Oversampling ratio	128	96
Signal band (kHz)	25	250
Differential input range (V)	[–1.0, 1.0]	[–0.7, 0.7]
Reference voltage (V)	1.8	1.0
Supply voltage (V)	1.8	1.8
Power dissipation (mW)	7.8	1
Area (mm^2)	0.083	0.02
Technology	TSMC18MMRF	TSMC18MMRF
Technology	3Well-2P6M	3Well-2P6M

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