A 6–9 GHz ultra-wideband CMOS PA for China's ultra-wideband standard*

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Abstract: A 6–9 GHz ultra-wideband CMOS power amplifier (PA) for the high frequency band of China's UWB standard is proposed. Compared with the conventional band-pass filter wideband input matching methodology, the number of inductors is saved by the resistive feedback complementary amplifying topology presented. The output impendence matching network utilized is very simple but efficient at the cost of only one inductor. The measured S_{22} far exceeds that of similar work. The PA is designed and fabricated with TSMC 0.18 μm 1P6M RF CMOS technology. The implemented PA achieves a power gain of 10 dB with a ripple of 0.6 dB, and $S_{11} < -10$ dB over 6–9 GHz, $S_{22} <$ –35 dB over 4–10 GHz. The measured output power at the 1 dB compression point is over 3.5 dBm from 6 to 9 GHz. The PA dissipates a total power of 21 mW from a 1.8 V power supply. The chip size is 1.1×0.8 mm^2.

Key words: power amplifier; CMOS; ultra-wideband
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1. Introduction

The demand for a high-speed wireless communication system has grown during the last few years. Ultra-wideband (UWB) has emerged as a new technology capable of transmitting data with low power and high data rate. Since the Federal Communications Commission (FCC) has allocated UWB applications in the 3.1–10.6 GHz frequency range, accordingly, the China Radio Administration Bureau allocated 4.2–4.8 GHz and 6–9 GHz frequency ranges for China's UWB applications as shown in Fig. 1. The UWB power amplifier (PA) is one of the most challenging components in ultra-wideband systems. The amplifier must meet several stringent requirements such as broadband input matching, sufficient gain with wide bandwidth, and stability. In addition, it is highly desirable to implement this amplifier in CMOS technology in order to perform a high level of integration. This poses other design challenges due to the inferior RF characteristics of CMOS, such as larger parasitic capacitance, lower transconductance, and lower supply voltage.

Until now, the reported wideband amplifiers have normally been sorted by three major topologies: the distributed amplifier[1, 2], the resistive feedback amplifier[3], and the band-pass filter based input matching amplifier[4, 5]. The distributed amplifier can absorb the parasitic capacitance of the input transistor as part of the transmission line, which leads to a broadband operating performance, but needs to consume a large DC current and occupy a large area of chips due to the multiple amplifying stages. The traditional resistive feedback amplifier provides good wideband matching and flat gain, but consumes rather a large amount of current in the CMOS process since the voltage gain is strongly dependent on the amplifying transistor's transconductance. The band-pass filter-type input matching amplifier can achieve wideband matching and low power consumption, but utilizes too many inductors. In this study, a resistive feedback complementary amplifying topology is employed as the input matching network. Compared with the classic band-pass filter wideband input matching methodology[4, 5], which consumes two and four inductors respectively, it only exploits one inductor realizing the wideband input matching. The circuit design of the PA is detailed, and the chip implementation and the on-wafer testing results are shown.

2. Circuit design

Figure 2 shows the proposed PA core which consists of a complementary amplifying input stage, a common source second-stage and an output impendence matching stage. Figure 3 is the small-signal equivalent circuit for the input part of the proposed wideband PA core. Figure 4 is the small-signal equivalent circuit for the input impendence matching network, which is formed by C_1, L_1, C_{gs} and the input Miller component of R_1 where C_{gs} denotes the sums of the gate–source capacitance of M1, M2 and the input Miller capacitance of M1, M2$[(C_{gd1} + C_{gd2})(1 + A_{v1})]$ and C'_{gs} represents the sums of the gate–source capacitance of Mg , the drain–source capacitance of M1, M2 and the output Miller capacitance of M1, M2$[(C_{gd1} + C_{gd2})(1 + \frac{1}{A_{v2}})]$. The resistor R_e $[= R_1/(1 - A_v)]$ stands for the Miller equivalent input resistance of R_1, where A_{v1} is the open-loop voltage gain of the first stage expressed in Eq. (3). The voltage of the node X is set to 0.9 V, half of the supply voltage, $V_{DD}/2$. Z_{in}, the input impendence of the PA, is indicated in Eq. (1).

Z_{in} is optimized at 8 GHz by appropriate selection of the value for L_1 and C_1. With precise feedback resistor R_1, the band width could be extended to cover 6–9 GHz. Compared with the classical wideband input matching topology[5] in Fig. 5, this methodology saves three inductors, which reduces the chip area dramatically.

$$Z_{in} = SL_1 + \frac{1}{SC_2} + \frac{1}{\frac{1}{R_2} + SC_{gs}}, \tag{1}$$

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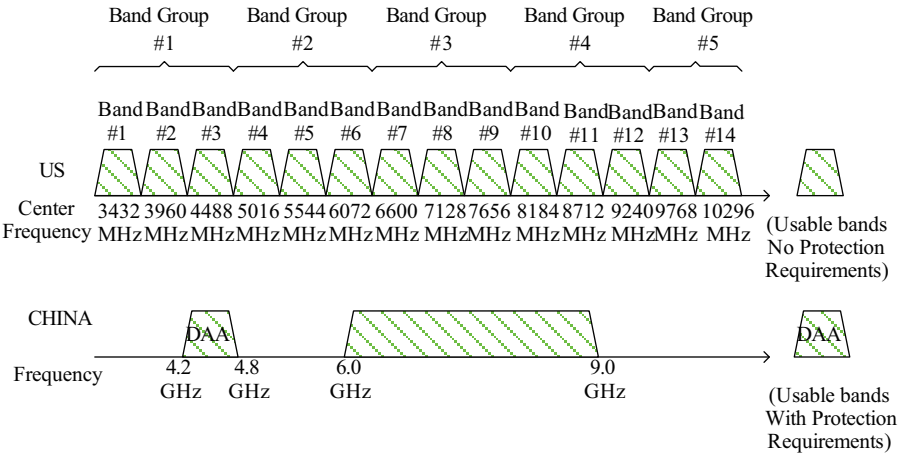

Fig. 1. US and China UWB spectrum standard.

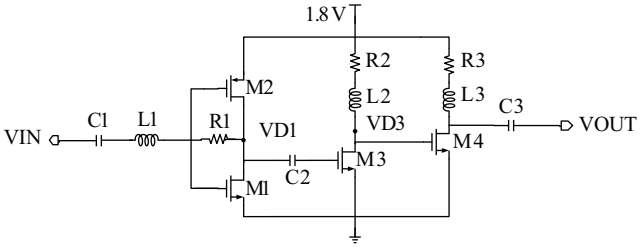

Fig. 2. Schematic of the proposed PA core.

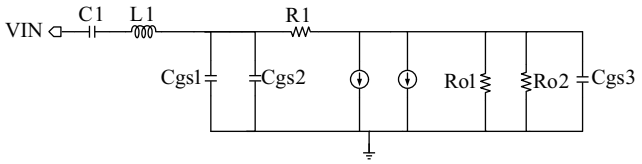

Fig. 3. Small-signal circuit model of the first stage.

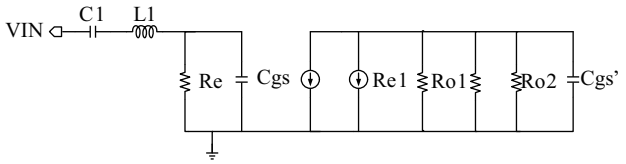

Fig. 4. Small-signal equivalent circuit of the input matching network.

$$R_{\mathrm{e}} = \frac{R_1}{1 - A_{\mathrm{v1}}}, \quad R_{\mathrm{e1}} = \frac{R_1}{1 + \dfrac{1}{A_{\mathrm{v2}}}}, \tag{2}$$

$$A_{\mathrm{v_2}} = (g_{\mathrm{m1}} + g_{\mathrm{m2}})(R_{\mathrm{o1}} \parallel R_{\mathrm{o2}}), \tag{3}$$

$$Z_{\mathrm{out}} = \frac{1}{SC_3} + \frac{1}{\dfrac{1}{r_{\mathrm{o4}}} SC_{\mathrm{p4}} + \dfrac{1}{SL_3 + R_3}}. \tag{4}$$

The transfer function of the first stage can be expressed as Eq. (5), which is a narrow-band frequency response. The second stage is a simple common-source stage, which provides high-frequency gain and determines the higher 3-dB bandwidth of the PA. A series peaking inductor L_2 is resonant with the total parasitic capacitances C_{D3} at the drain of M3 around 10 GHz. The transfer function of this is expressed as Eq. (6). Conventionally, the quality factor (Q factor) of the inductor for PAs should be as high as possible to achieve a high-gain, narrow-band characteristic. However, the quality factor of L_2 in this design is kept smaller for the flat gain of the whole PA. Hence, an extra resistor of 15 Ω is added to reduce the Q factor. The third stage is an output impendence matching stage with transfer function shown in Eq. (7). Combined with the gain flattening techniques mentioned above, the S_{21} ripple is excellent within 0.6 dB over 6–9 GHz verified by the measurement results in Fig. 8.

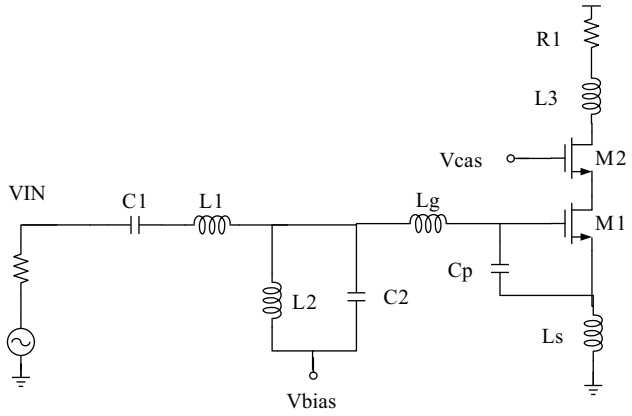

Fig. 5. Classical band-pass filter input matching topology.

$$\frac{V_{\mathrm{D1}}}{V_{\mathrm{1N}}} = \frac{R_{\mathrm{e}} + \dfrac{1}{SC_{\mathrm{gs}}}}{\dfrac{1}{SC_1} + SL_1 + R_{\mathrm{e}} + \dfrac{1}{SC_{\mathrm{gs}}}} \times \frac{1}{\dfrac{1}{R_{\mathrm{e1}}} + \dfrac{1}{R_{\mathrm{o1}}} + \dfrac{1}{R_{\mathrm{o2}}} + SC'_{\mathrm{gs}}}, \tag{5}$$

$$\frac{V_{\mathrm{D3}}}{V_{\mathrm{D1}}} = g_{\mathrm{m3}} \left[(SL_2 + R_2) \parallel \frac{2}{SC_{\mathrm{gs4}}} \right], \tag{6}$$

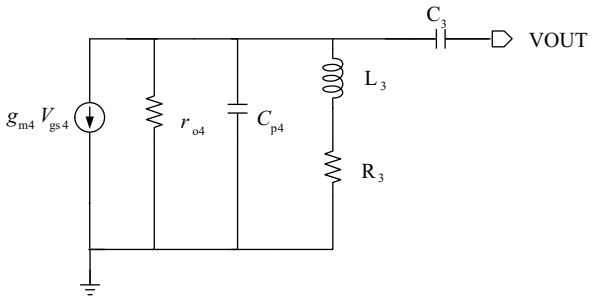

Fig. 6. Small-signal equivalent circuit of the output matching network.

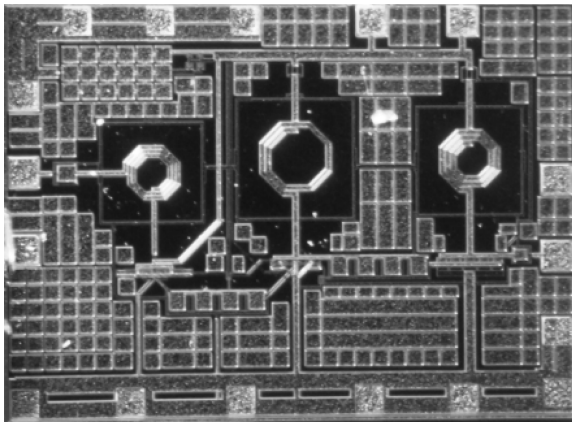

Fig. 7. UWB PA die photo.

$$\frac{V_{\text{out}}}{V_{\text{D3}}} = g_{\text{m4}} \frac{1}{\dfrac{1}{r_{\text{o4}}} + SC_{\text{p4}} + \dfrac{1}{SL_3 + R_3} + \dfrac{1}{\dfrac{1}{SC_3} + R_{\text{load}}}} \times \frac{R_{\text{load}}}{\dfrac{1}{SC_3} + R_{\text{load}}}. \quad (7)$$

Figure 6 shows the small-signal equivalent circuit of the output matching network. C_3, L_3, R_3, C_{p4}, and r_{o4} form an output impendence matching network, where C_{p4} represents the parasitic capacitance at the drain of M4. Z_{out} is expressed in Eq. (4). The output impendence matching network utilized here is very simple but efficient at the cost of only one inductor. The measured S_{22} far exceeds that of similar work.

Working in the high frequency of 6–9 GHz, the layout plays an important role in the overall circuit performance. Operating in such a high frequency range, the signal can suffer from parasitic capacitors between the metal layer or via and substrate. In this design the top thick metal is used for the signal path to reduce the capacitors from the metal to the substrate.

3. Measurement results and analysis

The PA in this work is designed in TSMC 0.18 μm 1P6M RF CMOS technology. The chip photograph of the circuit, with an area of 1.1 × 0.8 mm^2 including pads, is shown in Fig. 7. The PA is tested on wafer. An Agilent E8363B is used to measure the S parameters. The measured S parameters are demonstrated in Fig. 8. The simulated and measured S parameters are

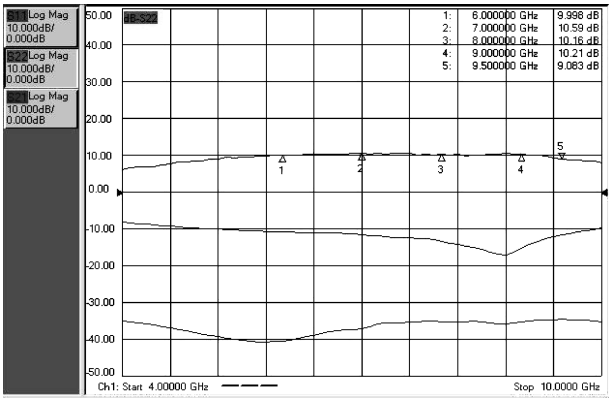

Fig. 8. Measured S parameters.

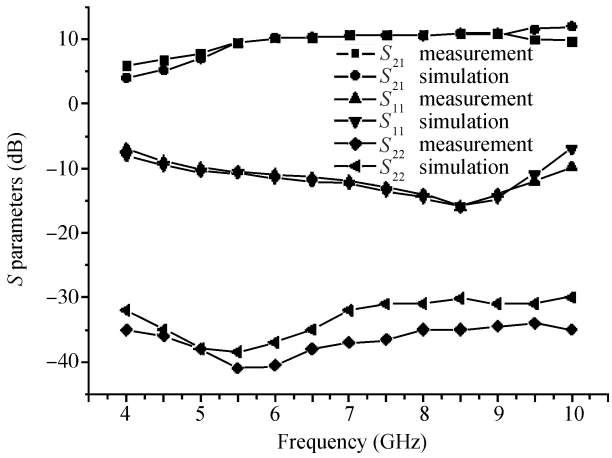

Fig. 9. Measured and simulated S parameters.

compared in Fig. 9. The measured S_{11} agrees well with simulations with –10 dB below from 6 to 9 GHz. The measured S_{21} is also quite close to simulations and has a ripple of an excellent 0.6 dB from 6 to 9 GHz. The measured S_{22} is the outstanding merit of this thesis (< –35 dB) over 4 to 10 GHz, which far exceeds that of similar UWB amplifiers[5, 7–10]. Figure 10 shows the output 1 dB compression points of the amplifier, swept versus frequency. The measured $\text{OP}_{1\text{dB}}$ compression point is above 3.5 dBm from 6 to 9 GHz. The total current used in this circuit is 11.6 mA under 1.8 V supply voltage.

Table 1 summarizes the performance of the proposed PA, with a comparison with previously published UWB CMOS PAs.

4. Conclusion

This paper describes the design of a 6–9 GHz CMOS PA fabricated in TSMC 0.18 μm 1P6M CMOS technology. To obtain wideband input matching, a resistive feedback complementary amplifying topology is employed, which saves the number of inductors. The output impendence matching network utilized is very simple but efficient at the cost of only one inductor. The implemented PA achieves a power gain of 10 dB with a ripple of 0.6 dB, and S_{11} < –10 dB over 6–9 GHz, S_{22} < –35 dB over 4–10 GHz. The measured output power at the 1 dB compression point is over 3.5 dBm from 6 to 9 GHz.

Table 1. Performance comparison with published UWB PAs.

Reference	Technology	BW (GHz)	S_{21} (dB)	S_{11} (dB)	S_{22} (dB)	Gain ripple (dB)	Power (mW)
This work	0.18 μm CMOS	6–9	10	< –10	< –35	0.6	21
Ref. [7]	0.18 μm CMOS	3.1–8.5	10	< –9	< –8	6	25.2
Ref. [8]	0.18 μm CMOS	6–10	8	< –7	< –3	2	18
Ref. [9]	0.18 μm CMOS	3.0–10.0	10.4	< –10	< –10	0.8	84

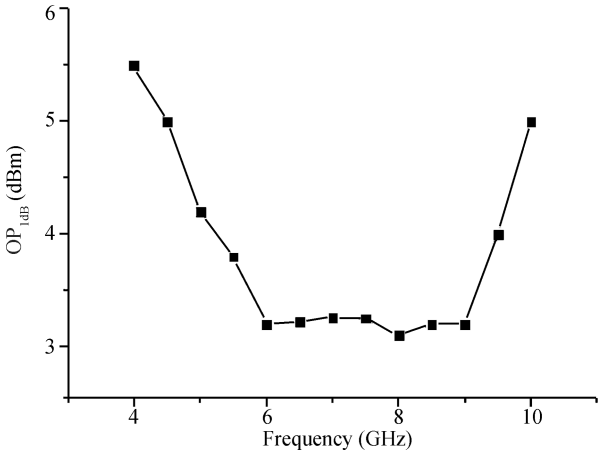

Fig. 10. Measured OP_{1dB} versus frequency.

The PA dissipates a total power of 21 mW from a 1.8 V power supply. The measured results validate the feasibility of these techniques.

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