Fabrication of a 120 nm gate-length lattice-matched InGaAs/InAlAs InP-based HEMT*

Huang Jie(黄杰)[1, 2, †], Guo Tianyi(郭天义)[1], Zhang Haiying(张海英)[1], Xu Jingbo(徐静波)[1], Fu Xiaojun(付晓君)[1], Yang Hao(杨浩)[1], and Niu Jiebin(牛洁斌)[1]

(1 Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China)
(2 School of Physical Science and Technology, Southwest University, Chongqing 400715, China)

Abstract: A new PMMA/PMGI/ZEP520/PMGI four-layer resistor electron beam lithography technology is successfully developed and used to fabricate a 120 nm gate-length lattice-matched $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ InP-based HEMT, of which the material structure is successfully designed and optimized by our group. A 980 nm ultra-wide T-gate head, which is nearly as wide as 8 times the gatefoot (120 nm), is successfully obtained, and the excellent T-gate profile greatly reduces the parasitic resistance and capacitance effect and effectively enhances the RF performances. These fabricated devices demonstrate excellent DC and RF performances such as a maximum current gain frequency of 190 GHz and a unilateral power-gain gain frequency of 146 GHz.

Key words: HEMT; InP; InGaAs/InAlAs; cutoff frequency; T-shaped gate technology
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1. Introduction

Millimeter and submillimeter-wave frequency ranges are of great interest for remote atmospheric sensing, next-generation automotive collision-avoidance radars, broadband and satellite communications[1, 2]. InP-based InGaAs/InAlAs high electron mobility transistors (HEMTs) are considered to be one of the most promising devices for these applications. These performances are attributed to the high electron mobility, high saturation velocity, and high sheet carrier density obtained in this material system[3]. The continuous drive to improve the RF performance of HEMT technology has led to the development of various sub 100 nm gate processes[4, 5]. The fabrication of short gate length T-shaped gates has become increasingly difficult as the footwidth of the gate is made smaller. The T-shaped gate is the key to the device fabrication process. At present, there are basically two kinds of methods in the fabrication of T-shaped gates, namely one method with media-assisted support and another with non-media-assisted support. The latter is widely used, due to the small parasitic effect of the T-gate and its relatively simple manufacturing processes, which only use wet etching and electron beam lithography (EBL) technology, and do not need high-power equipment. In this article, this T-shaped gate technology with non-media-assisted support is performed. A new PMMA/PMGI/ZEP520/PMGI four-layer resistor electron beam lithography (EBL) technology is successfully developed and used to successfully fabricate a lattice-matched $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ InP-based HEMT with excellent DC and RF performances such as a maximum current gain frequency (f_T) of 190 GHz and a unilateral power-gain gain frequency (f_{max}) of 146 GHz.

2. Material structures

The expitaxial structure of the InGaAs/InAlAs channel HEMT employed in our study was designed and optimized by our group and grown by MBE technology, which is shown in Table 1. All layers were grown by MBE on a semi-insulating InP-substrate. From bottom to top, the basic structure consists of a 300 nm $In_{0.52}Al_{0.48}As$ buffer layer, a 15 nm $In_{0.53}Ga_{0.47}As$ channel followed by a 3 nm spacer layer and a Si-δ-doped (5×10^{12} cm^{-3}) $In_{0.52}Al_{0.48}As$ donor layer. Then an 8 nm undoped $In_{0.52}Al_{0.48}As$ Schottky layer was grown followed by a 4 nm InP etch-stopper layer and a 30 nm doped (1×10^{19} cm^{-3}) $In_{0.53}Ga_{0.47}As$ cap layer. All the layers are lattice-matched to the InP substrate. Hall measurement of the grown material indicated that the two-dimensional electron gas (2DEG) sheet density is 3.32×10^{12} cm^{-2} and the mobility is 9300 cm^2/(V·s) at room temperature.

3. Fabrication process

The devices were fabricated by ohmic metallization, mesa etching and formation of the T-shaped gate. The fabrication process is as follows. Firstly, the source and drain ohmic metal patterns were formed by an image reversal process using AZ5214 photoresist (PR) for the lift off process[6]. The source–drain space L_{sd} is 2 μm. After pattern lithography, to achieve ohmic metallization we evaporated Ni/Ge/Au/Ge/Ni/Au (40/40/660/80/30/2200 Å) using an electron beam evaporator. Then the devices were annealed in nitrogen (N_2) ambient at a temperature of 270 ℃ for 10 min to decrease the contact resistance between the metal and semiconductor[7], and a contact resistance of 0.16 Ω·mm was obtained. Secondly, mesa etching can be accomplished by wet chemical

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† Corresponding author. Email: jiehuang_79@sohu.com
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Table 1. InP-based InGaAs/InAlAs HEMT epitaxial layer structure.

Layer		Thickness (nm)	Dopant	Concentration (cm^{-3})
$In_{0.53}Ga_{0.47}As$	Cap	30	Si	1×10^{19}
InP	Etch-stopper	4		
$In_{0.52}Al_{0.48}As$	Barrier	8		
Si-δ-doped layer			Si	5×10^{12}
$In_{0.52}Al_{0.48}As$	Spacer	3		
$In_{0.53}Ga_{0.47}As$	Channel	15		
$In_{0.52}Al_{0.48}As$	Buffer	300		
		SI InP substrate		

etching using a mixed etchant of $H_3PO_4 : H_2O_2 : H_2O$ (3 : 1 : 50) to expose the $In_{0.52}Al_{0.48}As$ buffer layer. In order to allow on-wafer DC and RF characterization the coplanar waveguide bondpads patterns were formed by an IR process using AZ5214 PR and Ti/Au (250/3000 Å) connection wires were evaporated.

The definition of the 120 nm T-shaped gate was followed by use of an electron beam lithography tool operating at 100 keV, with a new four-layer (PMMA/PMGI/ZEP520/PMGI) EB resist stack, which is different from our group's previous trilayer resist process[8, 9] in order to form a narrower gate-length. This is mainly due to the following considerations. First of all, to produce a T-shaped gate around 100 nm, the width–length ratio of the T-shaped gatefoot should meet certain requirements; measures such as replacing part of the ZEP520A with PMGI can reduce the thickness of ZEP520A and are conducive to producing shorter gate length devices. Then ZEP520 is difficult to remove clearly. So we choose PMGI as the bottom of the four-layer PR stack. It is easily removed to ensure that imaging is complete without EB resist on the chip surface. Briefly, a four-layer (PMMA/PMGI/ZEP520/PMGI) EB resist stack was used to pattern the T-shaped resist profile and one lithography step was employed. A 20-nm-wide gate line in the middle of the source and drain pad was exposed at 1000 $\mu c/cm^2$. The top PMMA layer was selectively developed in methylisobutyketone (MIBK)/isopropanol (IPA). The intermediate PMGI layer was selectively developed in TAHM/H_2O, and only the head of the T-shaped gate was defined in this step. The ZEP520A layer is in ZED-N50, where the gatefoot of 120 nm will be defined, and then the PMGI layer has the purpose that BE PR on the chip surface can be removed completely. After patterning the 120 nm T-shaped gate, gate recessing was performed using citric-acid-based ($C_6H_8O_7 : H_2O_2 = 1 : 1$) wet etching prior to Ti/Pt/Au (25/25/300 nm) gate metallization, whose etching selectivity ratio of InGaAs over InP is about 160[10]. Figure 1 shows an SEM photo of the T-shaped pattern after development and lifting. Figure 2 shows a photograph of the device we obtained with a gate length of 120 nm and a gate width of 2×50 μm. During the whole process, no surface passivation was performed. This is because passivation will cause a parasitic capacitance gate effect, and then weaken the high-frequency performances such as the current cut-off frequency and maximum oscillation frequency.

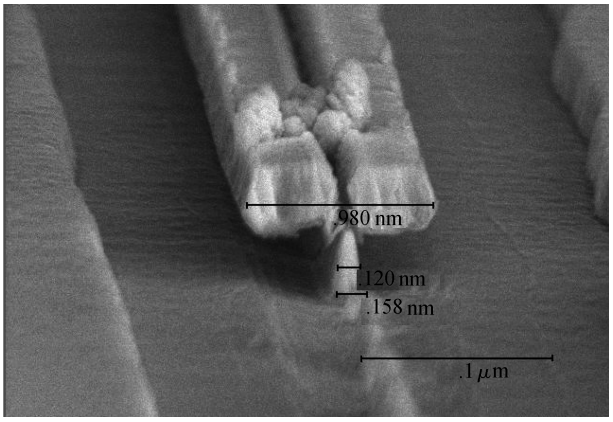

Fig. 1. SEM photo of T-shaped pattern after development.

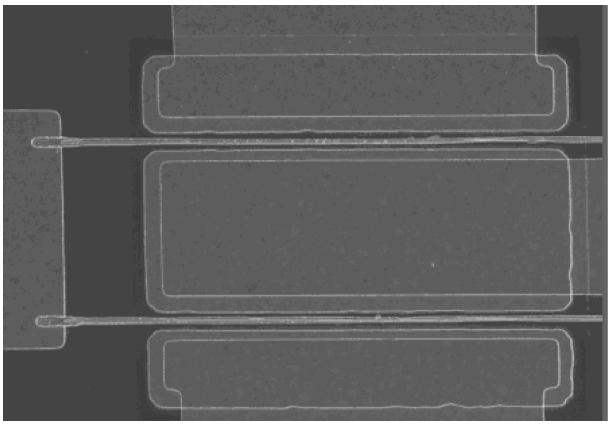

Fig. 2. Partial photograph of an InP HEMT.

4. Results and discussion

DC and RF characteristics were measured using a probe station and RF probe from Cascade Microtech. The current–voltage characteristics of 2×50 μm devices measured at room temperature are shown in Fig. 3, where the gate–source voltage V_{gs} is increased from (bottom) –1.0 V to (top) 0.6 V in steps of 0.4 V. The fabricated 120 nm T-shaped gate HEMT can be effectively pinched off at the gate bias $V_{gs} = -1$ V. The peak extrinsic transconductance (g_m) was 520 mS/mm at the gate bias $V_{gs} = -0.5$ V and the drain bias $V_{ds} = 1.5$ V in Fig. 4, where the relatively non-ideal DC curve shape occurs because domestic epitaxial growth technology on III–V compound semiconductors is not mature and also because of the deviation of gate-recess-etching during the device fabrication process.

On-wafer S-parameter measurements were performed from 1 to 26.1 GHz in steps of 0.1 GHz using an HP8510C vector analyzer at room temperature. Two-step de-embedding using an open and short pad was used to remove the parasitic ca-

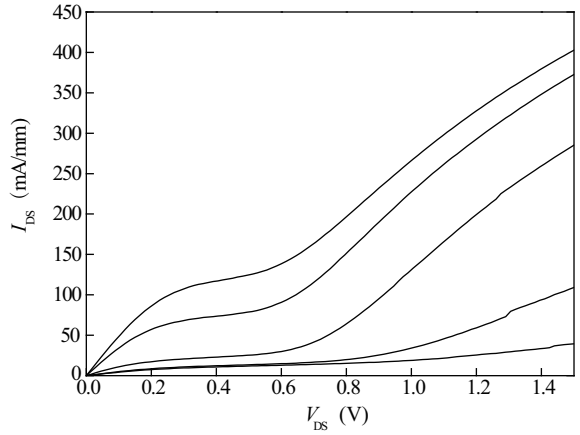

Fig. 3. DC characteristics of the HEMT.

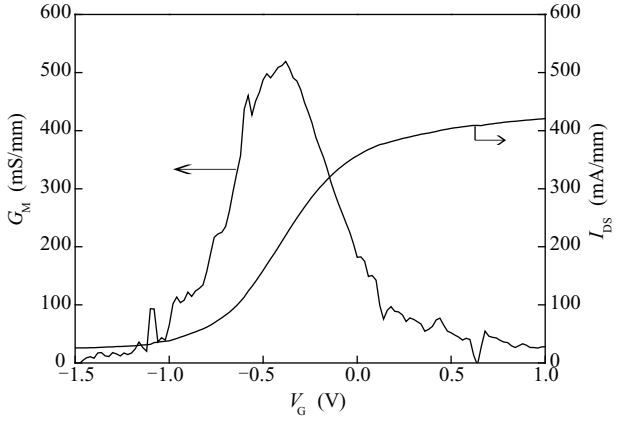

Fig. 4. Transfer characteristics of the HEMT.

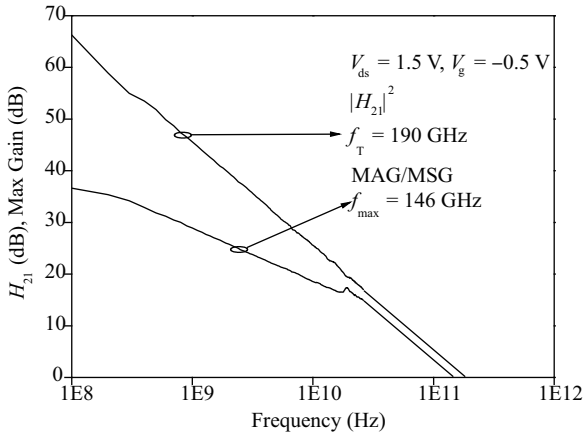

Fig. 5. Frequency dependence of current gain ($|H_{21}|^2$) and maximum oscillation frequency of the InAlAs/InGaAs HEMT.

pacitance and inductance components related to probing pads. Figure 5 shows the frequency dependence of the current gain $|H_{21}|^2$ and maximum available power gain (MAG) / maximum stable gain (MSG) at the gate bias V_{gs} = –0.5 V and drain bias V_{ds} = 1.5 V. Maximum oscillation frequency (f_{max}) and current gain cutoff frequency (f_T) were determined by extrapolating MAG/MSG and the current gain by the 20-dB/decade line. After de-embedding was carried out, the fabricated InP-based InGaAs/InAlAs 0.12 × 100 μm HEMT demonstrated a current cutoff frequency of about 190 GHz and a maximum unilateral power gain frequency of about 146 GHz, which are relatively lower than values reported by others because of the existence of PMGI at the bottom. This leads to lateral broadening of the gate foot during electron beam evaporation for the formation of T-shaped gate. However, the influence of the PMGI layer could be weakened by reducing its thickness.

We realize that a fabrication process series should be optimized in order to improve the maximum oscillation frequency (f_{max}) and current gain cutoff frequency (f_T). T-gate fabrication without using the dielectric layer enables low C_{gd}. In addition, an excellent T-shaped gate profile should have two typical characteristics, namely, the gatefoot should be as short as possible and the head of the T-gate should be as wide as possible. A 980 nm ultra-wide T-gate head, which is nearly as wide as 8 times the gatefoot (120 nm), is successfully obtained. Moreover, the mechanical stability of the gate has not been weakened. A wide T-gate head enables low gate resistance. Our T-gate has 180 nm gate stem height, which is determined by the thickness of the bottom two layers BE PR (ZEP520A/PMGI). The gate parasitic capacitance is proportional to the ratio of the gate head width over the gate stem height. Therefore, the gate parasitic capacitance is greatly reduced. Moreover, the gate parasitic resistance is also reduced because of the increase in the gate head width.

5. Conclusions

In this letter, we have successfully developed a new PMMA/PMGI/ZEP520/PMGI four-layer resistor electron beam lithography (EBL) technology and achieved a perfect T-gate profile, with a wide gate head of 980 nm and a narrow T-gate gatefoot of 120 nm, to get high f_T, low gate-to-drain capacitance, and low gate resistance. We fabricated a 120 nm gate-length lattice-matched $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ InP-based HEMT by optimizing the fabrication process and these fabricated devices also demonstrated excellent DC and RF performances such as a maximum current gain frequency (f_T) of 190 GHz and a unilateral power-gain gain frequency (f_{max}) of 146 GHz. These good performances are advantageous in many millimeter-wave applications.

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