A low power automatic gain control loop for a receiver*

Li Guofeng(李国锋), Geng Zhiqing(耿志卿), and Wu Nanjian(吴南健)†

(State Key Laboratory for Super lattices and Microstructures, Institute of Semiconductors, Chinese Academy of Sciences, Beijing 100083, China)

Abstract: This paper proposes a new structure to lower the power consumption of a variable gain amplifier (VGA) and keep the linearity of the VGA unchanged. The structure is used in a high rate amplitude-shift keying (ASK) based IF-stage. It includes an automatic gain control (AGC) loop and ASK demodulator. The AGC mainly consists of six-stage VGAs. The IF-stage is realized in 0.18 μm CMOS technology. The measurement results show that the power consumption of the whole system is very low. The system consumes 730 μA while operating at 1.8 V. The minimum ASK signal the system could detect is 0.7 mV (peak to peak amplitude).

Key words: low power; linearity; variable gain amplifier; automatic gain control loop; amplitude-shift keying
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1. Introduction

A body area network (BAN) is a potential technology which can monitor health status in real time and build a personal information system[1]. A typical BAN consists of vital sensors, personal audio/video devices, communication devices and a main body station. The vital signs and audio/video signals can be transferred by wired and wireless communication networks among the devices and the body station. Then the body station can transmit (receive) signal data to (from) a home base station.

The vital body parameter collection system is a typical application of the body area network. It usually consists of sensors, simulators, wireless transceivers and the body station. The wireless transceivers can provide the communication systems with low and high data rates. They are suitable for simple vital sensor networks, such as temperature, heart rate and pH[2], and image sensor systems, such as capsule endoscopy[3] and vision neurosimulators[4]. Because the sensors and simulators with RF transceivers are put inside or on the surface of body, they are usually powered by a small-size battery. The power consumption of the wireless transceiver should be ultra low, although the RF transceiver in capsule endoscopy must transfer a lot of images at a high rate[3].

In order to reduce the power consumption of the transceiver, some progress has been were reported. A simple ASK modulating and demodulating technique was adopted in the transceiver to reduce the power consumption[5]. The VCO direct modulation technique was adopted to increase data rate and reduce power consumption[6, 7]. In the transceivers, the power consumption of the RF-front end circuit was greatly reduced [8, 9], but in the IF-stage circuit there is a lot room for improvement in power consumption[10, 11]. The power consumption of the automatic gain control (AGC) loop circuit occupies the main part of the consumption in the IF-stage circuit. The design of a low power AGC loop is an important challenge.

This paper proposes a low power AGC loop for a high rate ASK receiver IF-stage. The AGC loop is followed by an ASK demodulator. In AGC, a new structure is proposed to reduce the power consumption. The AGC loop can provide a high dynamic range for the IF-stage and improve the sensitivity.

2. AGC architecture

Figure 1 shows the architecture of the AGC loop with an ASK demodulator. The AGC loop consists of six-stage variable gain amplifiers (VGAs), a high pass filter (HPF), a peak detector (PD) and an error amplifier (EA). The six-stage VGAs can amplify or attenuate the input signal and maintain the signal at a fixed level. The HPF plays a role in eliminating low frequency noise and DC offset. The feedback circuit consists of a PD and EA. The PD can detect the output signal of the six-stage VGAs and calculate its level. The EA is a differential operational amplifier and amplifies the differential signal between the output $V_{\rm d}$ of PD and the reference level $V_{\rm ref}$.Then it outputs an inverting control signal $V_{\rm ctrl}$ and adjusts the gain of the VGA chain.

In a typical radio frequency (RF) receiver, the RF small input signal should be amplified around 85 dB and then is sent into the digital baseband processor[12]. This gain of 25 dB is usually realized by a combination of LNA and mixer. Therefore, the AGC circuit must provide a maximum gain of 60 dB. The RF signal level depends on the wireless communication

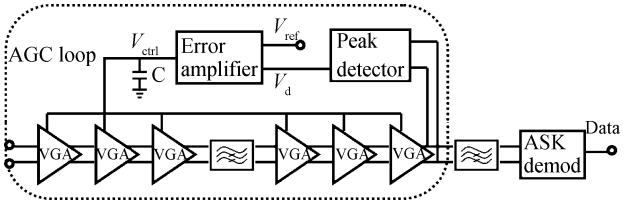

Fig. 1. ASK receiver block diagram.

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† Corresponding author. Email: nanjian@red.semi.ac.cn
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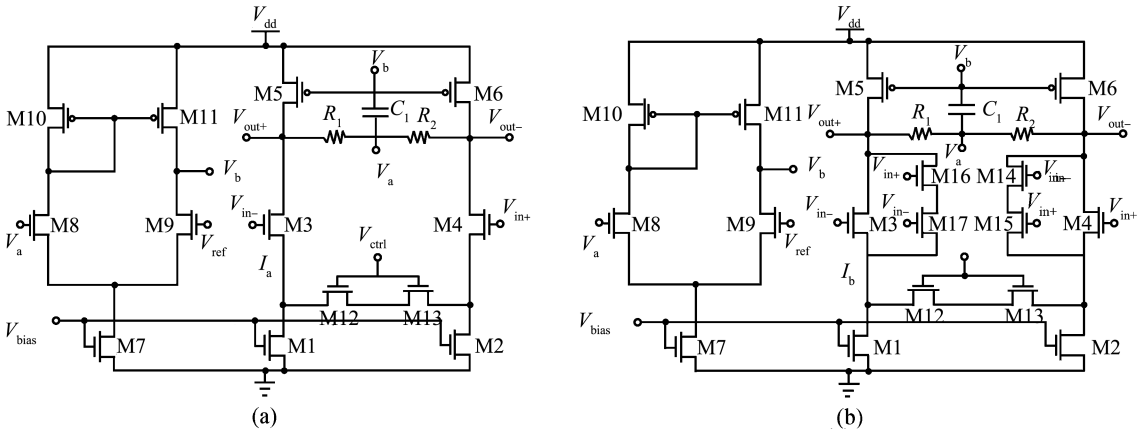

Fig. 2. Schematic of (a) one stage VGA and (b) improved VGA.

channel and varies by several decades. The AGC loop is used to compensate for this variation. Initially, the input signal is very small. After the input signal is amplified by the six-stage VGAs, the PD circuit detects the output signal of the six-stage VGAs and calculates its level $V_{\rm d}$. Then the EA compares the level $V_{\rm d}$ and the level $V_{\rm ref}$. It outputs a signal $V_{\rm ctrl}$ which controls the gain of the six-stage VGAs. The relation curve between $V_{\rm d}$ and $V_{\rm ctrl}$ is fixed. One $V_{\rm d}$ value corresponds to one $V_{\rm ctrl}$ value. The adjustment process is finished when $V_{\rm ctrl}$ is stabilized. The settling process is a trade off between speed and accuracy. Speed is determined by the slew rate of the EA with capacitor C. Accuracy is determined by the fluctuation of $V_{\rm ctrl}$ after the loop filter. The loop filter mainly consists of capacitor C. Here, we make a balance between them. Simulation results show that the fluctuation of $V_{\rm ctrl}$ is very small while the settling process is relatively quick. In the AGC loop, when the input signal level is different, the final stabilized output signal level of the six-stage VGAs is slightly different. This small difference makes $V_{\rm d}$ different which directly controls the value of $V_{\rm ctrl}$. $V_{\rm ctrl}$ changes the gain of the six-stage VGAs. Finally, the AGC loop outputs a constant-amplitude signal which could be stably demodulated by the ASK demodulator.

This paper designs a low power AGC loop circuit based on the above architecture, which is applied in a VCO-direct-modulation ASK receiver with a higher rate than 4 Mbps. We set the bandwidth of AGC to a value which fairly covers the system requirement. In the IF-stage, the carrier frequency is set to 6 MHz, and the bandwidth is set to 11 MHz due to the following reasons: (1) the ASK signal needs 8 MHz bandwidth to cover 4 Mbps data rate; (2) in the VCO direct modulation receiver the carrier frequency usually deviates from the target frequency[7]. Therefore the cut off frequencies of the HPF and AGC are designed to be 250 kHz and 11 MHz, respectively. In the AGC loop a proposed VGA circuit is used to reduce the power consumption while keeping the linearity almost unchanged. The details are given below.

3. Circuit design and operation

3.1. AGC loop

The AGC loop circuit in Fig. 1 consists of six-stage VGAs, a high pass filter (HPF), a PD and an error amplifier (EA). To eliminate low frequency noise and DC offset, an HPF is inserted between two three-stage VGAs. Without the HPF, DC offset will cause distortion in the following VGA stages while too many HPFs will occupy too much chip area. After calculation and simulation, the output DC offset of the three-stage VGAs is less than 200 mV which can be recovered after one HPF to a normal operating voltage level. Considering that the frequency response of the six-stage VGAs is a low pass characteristic, after inserting one HPF, the AGC shows a band pass characteristic. Such a method to eliminate DC offset shows a constant high pass cut off frequency which will not change with the gain of the six-stage VGAs. However, other techniques such as the continuous-time feedback technique[13] will change the high pass cut off frequency with the gain of the VGA which apparently cannot provide a constant bandwidth[14].

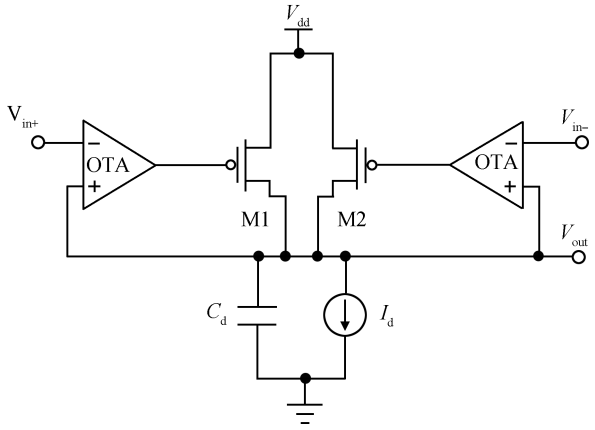

Fig. 3. Schematic of the peak detector.

One stage of the differential VGA circuit is shown in Fig. 2. M3 and M4 form the linear transconductance pair. R_1 and R_2 act as the load to provide high gain. The common-mode feedback circuit consists of R_1, R_2, M7–M10. In order to reduce the power consumption, a new structure in Fig. 2(b) is proposed to improve the linearity of the VGA[15]. Working with M16 and M14, M17 and M15 operate in the triode region. After carefully selecting the sizes of M17 and M15, the third order intermodulation of M17, M15 and M3, M4 can be cancelled out. This improves the linearity of the VGA. Due to the fact that there is a trade off between linearity and power consumption,

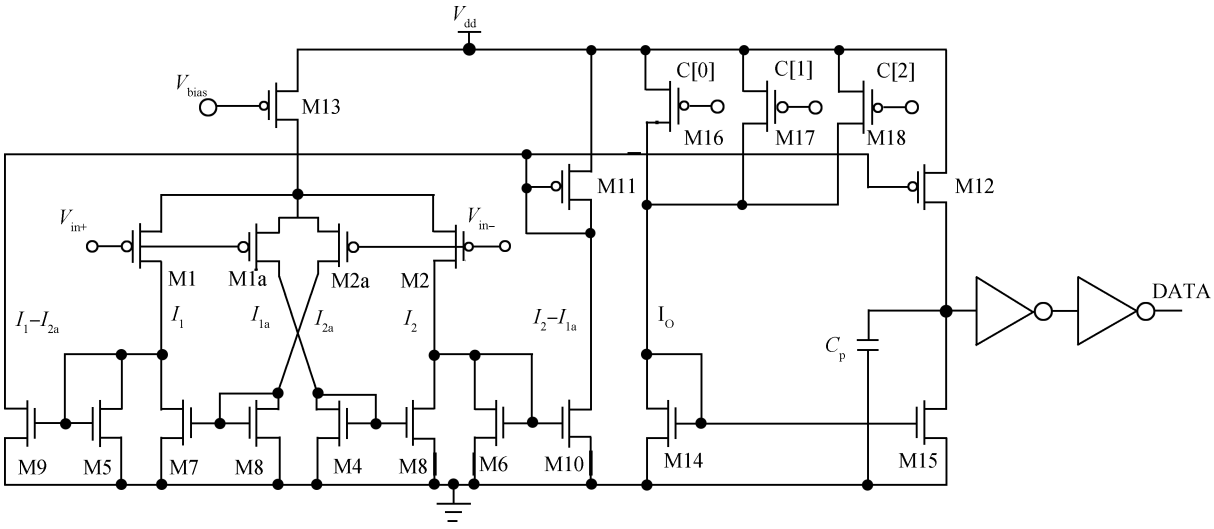

Fig. 4. Schematic of the ASK demodulator.

utilizing such a technique could reduce the power consumption while at the same time keeping the linearity unchanged. A simulation shows that if the power consumption is unchanged, adopting such a structure can improve I_{M3} by 6 dB. If the I_{M3} is unchanged, the power consumption can be reduced by 30% according to Eq. (1)[16]. This paper reduces the power dissipation by adopting such a technique, while keeping the linearity unchanged.

$$\Delta I_{M_3} = 20 \lg \left(\frac{I_a}{I_b} \right)^2, \tag{1}$$

where I_a and I_b are the current consumption of Figs. 2(a) and 2(b), and I_b is 30% smaller than I_a.

The gain of the VGA shown in Figs. 2(a) and 2(b) can be expressed as:

$$A_v = G_s R_d \frac{g_m}{g_m + G_s}, \tag{2}$$

where g_m, R_d and G_s represent the transconductance of the input transistors M1 and M2, the load resistance of R_1 and R_2 and the conductance of source degeneration transistors M12 and M13 respectively.

$$G_s = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{gs} - V_{th}). \tag{3}$$

If $g_m \gg G_s$, $g_m/(g_m + G_s) \approx 1$, A_v can be rewritten as

$$A_v = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L} \right)_{13} (V_{gs13} - V_{th}) R_d. \tag{4}$$

Therefore, the gain of the VGA can be linearly controlled by the gate voltage of V_{gs13}.

Figure 3 gives the schematic of the PD. V_{in+} and V_{in-} are differential signal outputs from the last stage VGA which determine charging (discharging) of the capacitor C_d depending on the comparison with V_{out}. If charging, M1 and M2 are turned on to charge capacitor C_d. If discharging, M1 and M2 are turned off, and I_d discharges capacitor C_d. Current I_d plays a role in refreshing V_{out}. Otherwise, V_{out} will remain unchanged even though the input signal is changed. Choosing the value of current I_d depends on the data rate and linearity requirement. A high data rate needs a comparatively large current to maintain a high refreshing rate. However, a large current will compromise the linearity of the VGA because the fluctuation of V_{out} will increase with the current increment and the fluctuation will transfer to V_{ctrl} through the EA. In this design, we use the minimum current to satisfy the requirement of the data rate, which not only lowers the power consumption but also improves linearity.

3.2. ASK demodulator

Figure 4 is the schematic of the ASK demodulator. The schematic utilizes a double differential structure, which improves the sensitivity and responding speed of the ASK demodulator. The differential pairs consist of M1, M2, and M1a, M2a. V_{in+} and V_{in-} connect to the gate of M1, M1a and M2, M2a separately. The working principle of the ASK demodulator is described as follows: When V_{in+} is low and V_{in-} is high, the current generated at the source of M1 and M2a is I_1 and I_{2a}. The current generated at the drain of M9 is $I_1 - I_{2a}$ after subtraction operation. At the other side, with the same principle, the current generated at the drain of M10 is $I_2 - I_{1a}$, but the value is below zero which is actually equal to zero in the circuit. Finally, the current from M9 and M10 is summarized to M11 and mirrored to M12. If the current at the drain of M12 is larger (smaller) than the current at the drain of M15, it charges (discharges) the capacitor C_p. In this circuit, we control the threshold of the demodulator through digitally programming the gate state of M16–M18 by C[0], C[1], C[2] which determines the current value of I_o. When I_o is large, the current at the drain of M15 is large, and the electron cannot be accumulated at the capacitor C_p which makes the inverter not flipped. So, large I_o makes the threshold of the demodulator high[10].

4. Experimental results

The whole IF receiver system was fabricated in 0.18 μm CMOS technology. It is shown in Fig. 5, and occupies an area of about 1×1 mm^2.

Fig. 5. Micrograph of the IF-stage of the ASK receiver.

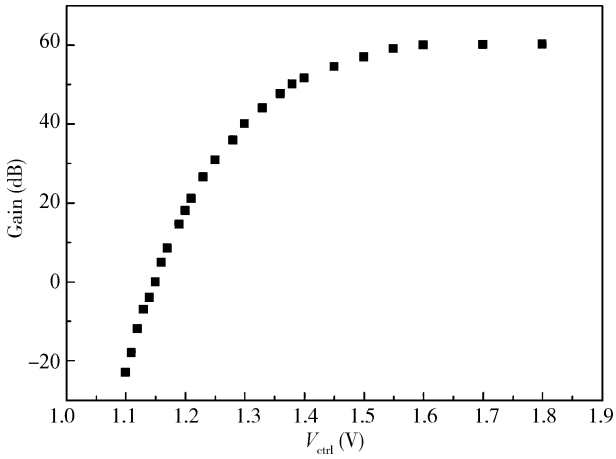

Fig. 6. Gain of the six-stage VGA with changing V_{ctrl}.

Figure 6 shows that the dB gain of the six-stage VGAs changes logarithmically with V_{ctrl}, which demonstrates good similarity with Eq. (4). Figure 7 shows the AC response of the six-stage VGAs when V_{ctrl} is 1.8 V. Due to the HPF, the AC response shows a band pass characteristic. The maximum and minimum gain is 60 dB and –20 dB. The high pass and low pass cut off frequencies are 250 kHz and 11 MHz which match the post simulation results well. Measurement shows that the high pass and low pass cut off frequencies change little when the gain changes. Deducing from the –20 dB/Decade roll off speed, DC offset suppression is about 50 dB when V_{ctrl} is 1.8 V. Figure 8 shows the AGC settlement process. When the 4 Mbps input ASK signal amplitude is reduced by 6 dB, the settlement time is less than 10 μs. When the 4 Mbps ASK signal amplitude is amplified by 6 dB, the settlement time is less than 20 μs. In the whole settling process, the ASK signal can be demodulated correctly. The whole AGC consumes 690 μA. Table 1 shows the test results of the AGC and makes some comparisons with other papers.

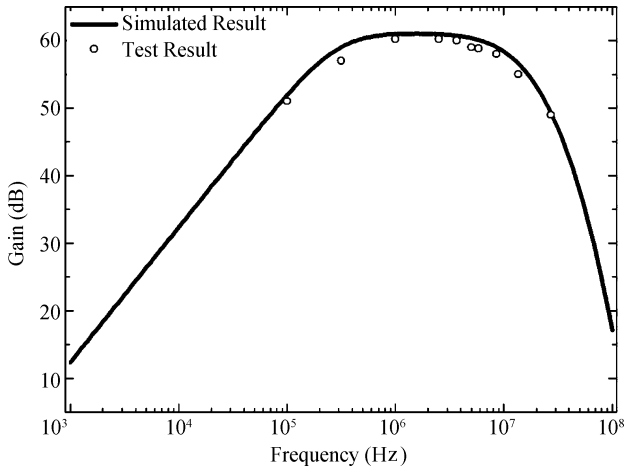

Fig. 7. Frequency response of the six-stage VGA.

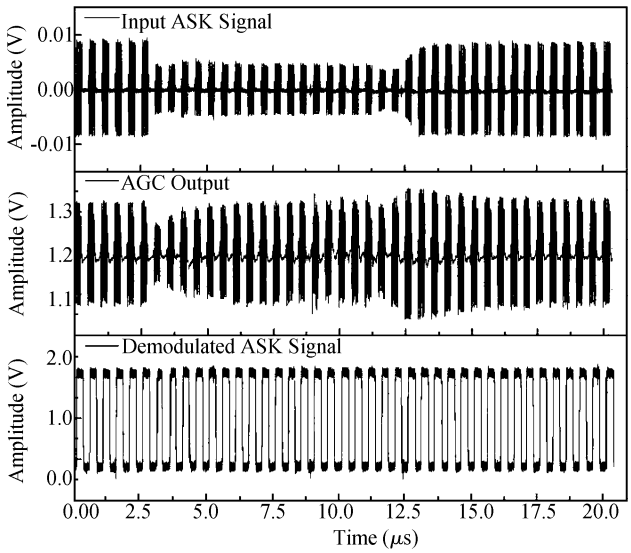

Fig. 8. Circuit response to changing the input ASK amplitude level.

Table 1. Comparison of AGC performance.

Parameter	Tadjpour[17]	Zheng[18]	Okjune[19]	This work
Technology (μm)	0.5	0.35	0.18	0.18
Power (mA)	10	2.1	5.8	0.69
Gain range (dB)	0–70	0–60	–8 to 32	–20 to 60
Bandwidth (MHz)	20	2.9	18	11
OIP3 (dBm)	20	16	—	15

The whole ASK-based IF receiver could demodulate minimally a 0.7 mV (peak to peak amplitude) ASK signal. The whole IF-stage consumes merely 730 μA. Table 2 gives some comparisons between this work and other papers including the AGC and ASK demodulator.

5. Conclusion

This paper proposes a new structure to lower the power consumption of a VGA and keep the linearity of the VGA un-

Table 2. Brief comparison of state-of-art IF receivers.

Parameter	Harjani[10]	Wang[11]	This work
Technology (μm)	0.5	0.18	0.18
Supply voltage (V)	3.3	1.8	1.8
Power (μA)	910	1200	730
Maximum gain (dB)	40	50	60
Data rate (Mbps)	1	2	4

changed. The IF-stage includes an AGC loop and ASK demodulator, embedded in a whole transceiver in 0.18 μm CMOS technology. The gain range of the IF-stage is –20 to 60 dB. The maximal data rate is 4 Mbps. The minimum ASK signal the system could detect is 0.7 mV (peak to peak amplitude). Such a low power system could be widely used in a BAN, satisfying its requirement for power and data rate.

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