A 12 bit 100 MS/s pipelined analog to digital converter without calibration

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Abstract: A 1.8 V 12 bit 100 MS/s pipelined analog to digital converter (ADC) in a 0.18 μm complementary metal–oxide semiconductor process is presented. The first stage adopts a 3.5 bit structure to relax the capacitor matching requirements. A bootstrapped switch and a scaling down technique are used to improve the ADC's linearity and save power dissipation, respectively. With a 15.5 MHz input signal, the ADC achieves 79.8 dB spurious-free dynamic range and 10.5 bit effective number of bits at 100 MS/s. The power consumption is 112 mW at a 1.8 V supply, including output drivers. The chip area is 3.51 mm^2, including pads.

Key words: pipelined ADC; multi-bit; opamp; low power
DOI: 10.1088/1674-4926/31/11/115007 **EEACC:** 2570

1. Introduction

High-speed high-resolution pipelined analog to digital converters (ADCs) are required in many digital applications, such as video digitizers and communication base stations. The fast trend towards advanced complementary metal–oxide–semiconductor (CMOS) processes has presented greater challenges as the device dimensions and supply voltages are scaled down. Using advanced processes, the design of low-voltage, high-gain, large-swing operational amplifiers (opamps) becomes more difficult. To realize high-resolution ADCs larger than 10 bits, the mismatch between capacitors needs special attention.

This paper presents a 12 bit 100 MS/s pipelined ADC which utilizes a 1.8 V supply voltage and is fabricated in a 0.18 μm CMOS process. The first stage adopts a multi-bit structure to improve the nonlinearities of the pipelined ADC and to relax the capacitor matching requirements. To realize a high-gain high-swing opamp, a two-stage amplifier with a gain-boosted structure in the first stage is adopted. This paper also describes the ADC architecture, and explains the circuit implementation of key building blocks.

2. Pipelined ADC architecture

The pipelined ADC architecture is shown in Fig. 1. The die is mainly composed of a clock generator, a reference block and an ADC core. The core has a sample-and-hold amplifier (SHA) as a front-end of the ADC. The first stage is a multi-bit (3.5 bit) stage and the rest of the pipeline consists of seven succeeding 1.5 bit stages and a 2 bit flash ADC at the end.

SHA: Because the input bandwidth of the ADC without a dedicated SHA can be limited due to aperture error[1], an SHA is applied with compromising power dissipation. For both noise and power advantages, a "flip-around" SHA (Fig. 2) is chosen over the charge-redistribution architecture.

Multi-bit 1st stage: the first stage adopts a 3.5 bit structure for the following reasons. (1) When the first stage changes from sample mode into settling mode, a step voltage (V_m) will be seen in the input of the opamp. It is pointed out in Ref. [3] that the higher resolution the 1st stage has, the lower the step voltage amplitude is. For the opamp designed in the advanced CMOS process, the small-signal bandwidth is preferable to the large-signal slew rate due to the limited $V_{gs} - V_t$. So adopting a multi-bit structure will be helpful for low power design. (2) Capacitor matching is crucial for the ADC to achieve 12 bit resolution without calibration, and it is helpful to reduce the capacitor mismatch error by using a multi-bit system in the first stage[4]. (3) Compared to a conventional 1.5 bit/stage structure, a multi-bit structure is more efficient in power dissipation. However, if the resolution is higher than four, the circuit of the

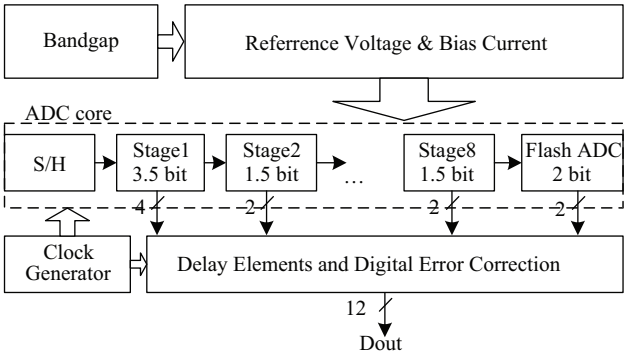

Fig. 1. Pipelined ADC architecture.

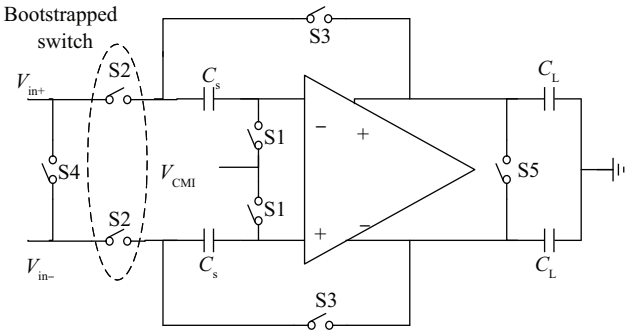

Fig. 2. Flip-around sample-and-hold amplifier.

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Received 6 May 2010, revised manuscript received 4 June 2010

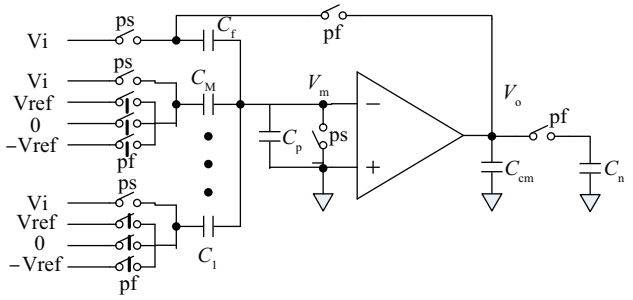

Fig. 3. Typical schematic of MDAC.

Table 1. Sample capacitor of every stage.

Stage N	Sample capacitor (single ended)
Stage1 (3.5 bit)	0.2 pF × 16
Stage2 (1.5 bit)	0.5 pF × 2
Stage3 (1.5 bit)	0.2 pF × 2
Stage4–8 (1.5 bit)	0.1 pF × 2

MDAC will become quite complicated[5, 6].

Scale down: due to the relaxed requirements of the stages along the pipeline chain, these stages are scaled down with regard to C and the bias currents. This results in a lower area and lower power consumption. Table 1 shows the sample capacitor of every stage.

3. Circuit implementation

3.1. OPAMP

The opamp is a fairly important element in a pipeline ADC, and the most critical opamps in the ADC are the two used in SHA and stage1. In SHA, the opamp must have an open loop gain A_0 of

$$A_0 > 2^{N+1}/f = 2^{12+1}(1 + C_p/C_s), \quad (1)$$

where C_s is the sample capacitor and C_p is the parasitic capacitor at the input opamp's input. Assuming $C_p/C_s \approx 0$, the minimum A_0 is 78 dB. Considering process corner variation, a design margin of 6 dB need reserved, which means that A_0 should be larger than 84 dB. In order to realize such a large gain, a cascode opamp combined with a gain-boost structure is adopted. However, this structure badly limits the output swing. So, a common source amplifier with a large output swing is added as the second stage. In addition, in Fig. 2 the size of the switch S1 is designed quite large because of the need for sample bandwidth, and when S1 is closed the charge injection will induce a large step voltage at the input of the opamp. So a folded cascode is selected as the first stage but not a telescopic cascode. Using PMOS-input folded cascode as the first stage, the input common mode voltage can be set lower, which means the smaller switch-on resistance of S1.

3.2. Comparator

Using a digital error correction technique, the first stage is tolerant of a comparator offset with a value of $V_{ref}/16$ (62.5 mV).

In order to reduce the requirement of the comparator, we adopt an "input offset storage" technique[7], as shown in Fig. 5.

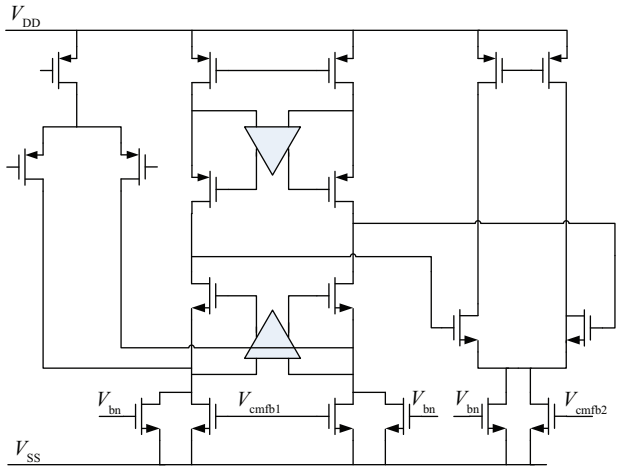

Fig. 4. High gain and large output swing OPAMP.

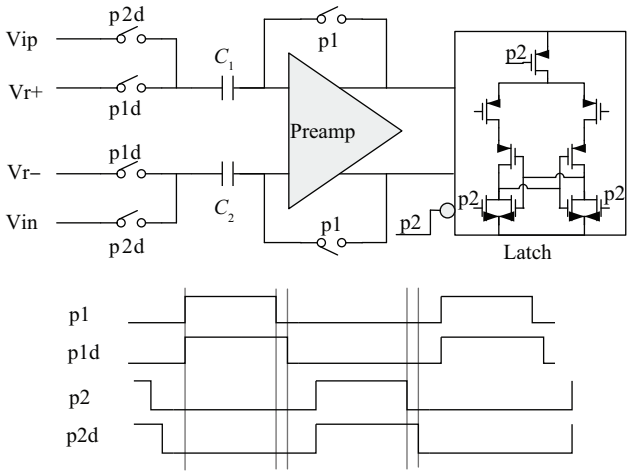

Fig. 5. Comparator using input offset cancellation techniques.

3.3. Bootstrapped switch

The sample circuit should achieve high speed, high linearity and high precision in the design of a high-resolution high-speed ADC. The performance of the sample circuit is usually limited by the performance of the sampling switches. The speed is limited by the on-resistance of the sampling switches, and the linearity is limited mainly by variation in the on-resistance. Then a bootstrapped switch is adopted because it has high linearity and small on-resistance compared to the same size negative channel metal–oxide–semiconductor (NMOS) switch[8]. In order to get excellent linearity, the sampling switches of SHA, the first stage (3.5-bit) and the second stage (1.5-bit) are bootstrapped switches, and the other stages adopt a CMOS sampling switch.

3.4. Reference voltage and reference current

Generally, there are two ways to design internal reference voltages[9]. The first way uses large off-chip capacitors. Then the reference voltages are stable because of the large capacitors. The other way uses high speed voltage buffers without off-chip capacitors. However, making reference voltages settle in 1/2 fs (5 ns), the voltage buffers are designed with high bandwidth, which means quite high power consumption. So, in

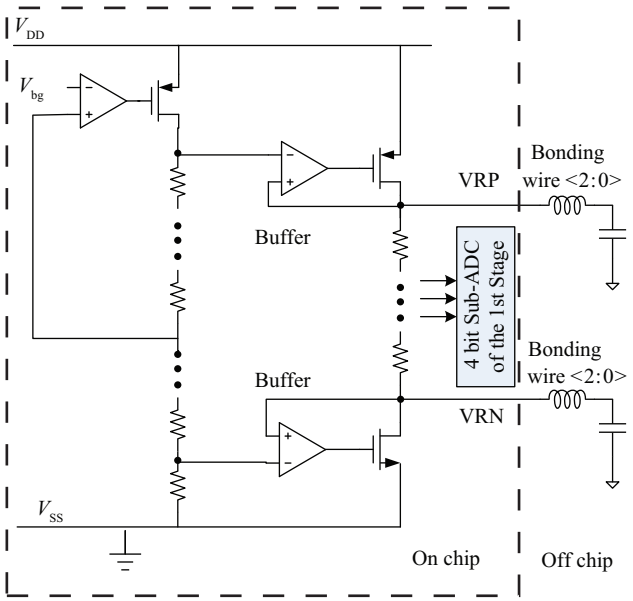

Fig. 6. Reference generator.

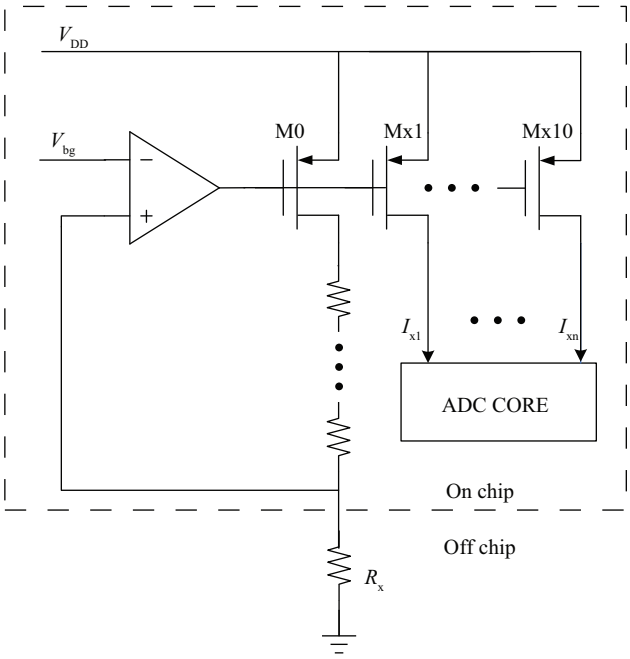

Fig. 7. Simplified schematic of reference current.

order to save power dissipation, the reference buffer with large off-chip capacitors is adopted here. Figure 6 shows the simplified schematic for the generation of top (VRP) and bottom (VRN) references, and the references for the 4-bit sub-ADC of the 1st stage are generated by the series resistances between the top and bottom references. VRP and VRN are connected to off-chip capacitors through bonding wire. To reduce the inductance effect of the bonding wire, 3 bonding pads are used for each reference voltage.

Figure 7 shows the generation of reference currents for opamps. V_{bg} is the bandgap voltage, which is almost independent of variations in process parameters, temperature and supply voltage. The current through the PMOS transistor M0 is set

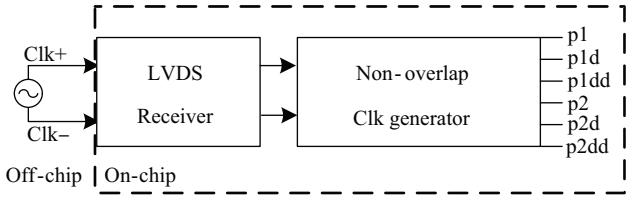

Fig. 8. Clock generation.

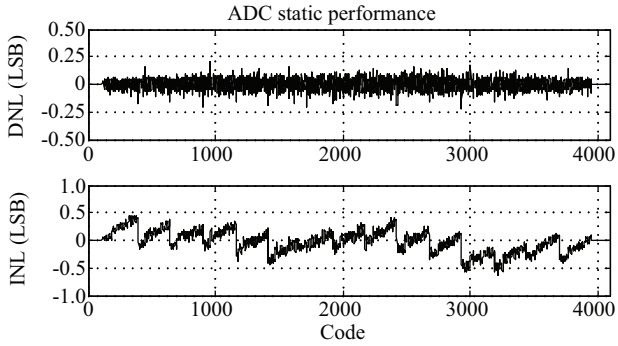

Fig. 9. Measured DNL and INL.

up by V_{bg} and the off-chip resistance R_x. The current through M0 is mirrored to I_{x1} to I_{x10}, which are applied to S/H, stages 1 to 9, respectively.

$$I_x = \alpha \frac{V_{bg}}{R_x}, \tag{2}$$

where α is the mirror coefficient.

Then we can control the bias currents of all opamps by adjusting the off-chip resistance R_x according to different sampling rates.

3.5. Clock generator consideration

When the sampling frequency is up to 100 MHz, it becomes difficult to transfer single-ended signals from off-chip to on-chip through bonding wire and pad. LVDS (low voltage differential signaling) has two primary characteristics: a small voltage swing and differential implementation[10]. LVDS is a good method in high speed signal transmission and it can reject common interference. So, in order to generate a high-speed low-jitter clock signal to the ADC core, the off-chip clock adopts LVDS input, as illustrated in Fig. 8. Then the differential signals are received by an LVDS receiver and translated to non-overlap clocks by a non-overlap clock generator.

4. Measurement results

The input signal and the clock are obtained by using Agilent E8267D and E4436B, respectively. Both were filtered using high-order passive band-pass filters. As illustrated in Fig. 9, with a 15.5 MHz input signal, the measured DNL and INL are within –0.22/+0.21 LSB and –0.62/+0.46 LSB, respectively, at 20 MS/s.

Figure 10 shows the measured FFT spectrum at 100 MSps and 15.5 MHz input signal. The SFDR, SNDR and ENOB are 79.8 dB, 65.1 dB and 10.5 bit, respectively.

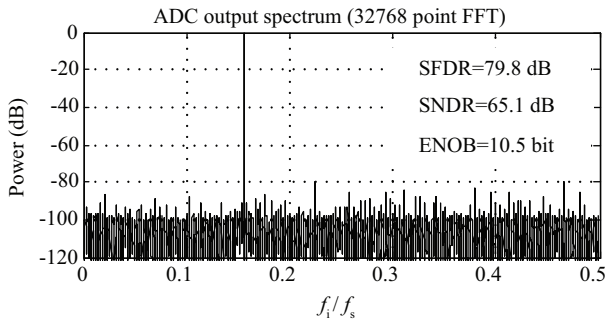

Fig. 10. Measured FFT spectrum at 100 MS/s and f_{in} = 15.5 MHz.

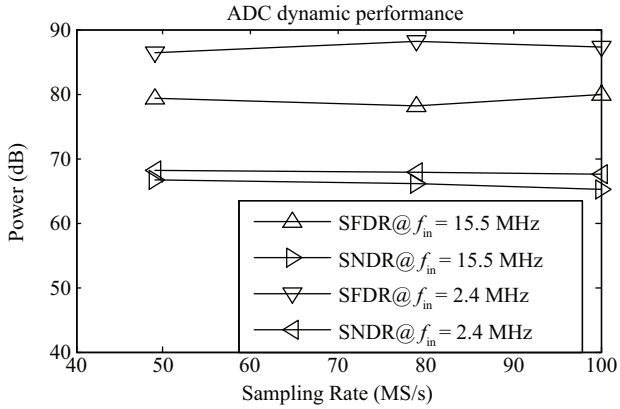

Fig. 11. Measured SFDR and SNDR versus conversion rate.

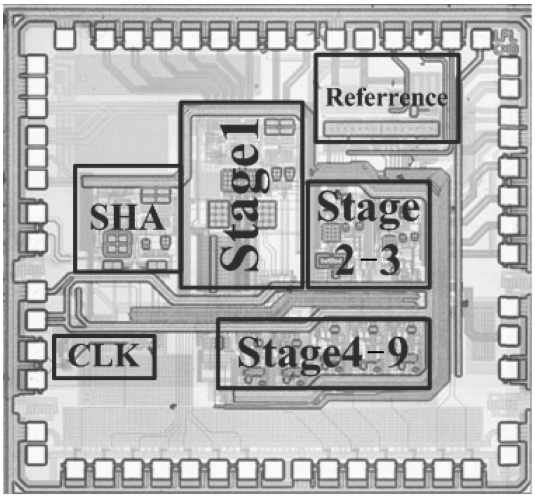

Fig. 12. Die micrograph.

Figure 11 shows the SFDR and SNDR with varying sampling frequencies up to 100 MHz. For the 2.41 MHz input, we always have the SFDR over 86 dBc and the ENOB over 10.9 bit. For the 15.5 MHz input, the ENOB is 10.8 bit at 50 MS/s and decreases to 10.5 bit at 100 MS/s.

Figure 12 shows the die micrograph of the chip. The key measurement results are summarized in Table 2. The ADC silicon area, including all pads, is 1.95 × 1.8 mm^2, and the power dissipation (including pad drivers) is 112 mW.

Table 3 lists this work and some other ADCs with similar performance in recent years. The figure of merit (FOM) is

Table 2. Key performance summary (25℃).

Parameter	Value
Process	0.18 μm 1P6M CMOS
Supply voltage	1.8 V
Sampling rate	100 MS/s
Resolution	12 bit
Full scale input	2 Vp-p
Area	1.95 × 1.80 mm^2
Power consumption @ 100 MS/s	Analog part 93 mW
	Digital part 19 mW
DNL	–0.22/+0.21 LSB
INL	–0.62/+0.46 LSB
SFDR (f_{in} = 15.5 MHz)	79.8 dB @ f_s = 100 MHz
SNDR (f_{in} = 15.5 MHz)	65.1 dB @ f_s = 100 MHz
ENOB (f_{in} = 15.5 MHz)	10.5 bit @ f_s = 100 MHz

calculated using the following formula:

$$\mathrm{FOM} = \frac{\mathrm{Power}}{2^{\mathrm{ENOB}} f_s}. \tag{3}$$

Power is the total power dissipation, ENOB is the effective number of bits of the ADC including distortion, and f_s is the sampling rate. As shown in Table 3, this work has the advantage of low power dissipation compared with existing work. It is worth noting that the FOM of the ADC in Ref. [11] is calculated from its analog power consumption, but not the total power consumption. In addition, compared with the ADCs[12−14] with an LMS-based calibration technique, this ADC converts analog input to accurate digital output directly, instead of waiting for a convergence time.

5. Conclusion

A 12-bit 100 MS/s pipelined ADC without using calibration technology is presented. The ADC is fabricated in a 0.18 μm 1P6M CMOS process. The area of the ADC is 1.95 × 1.80 mm^2 and the total power consumption is 112 mW. With a 15.5 MHz input signal, the SNDR and SFDR are 65.1 dB and 79.8 dB at 100 MS/s, respectively. This ADC has the advantage of low power dissipation compared with the ADCs presented in recent years.

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Table 3. Performance comparison with other ADCs.

Parameter	Ref. [11]	Ref. [12]	Ref. [13]	Ref. [14]	This work
Resolution (bit)	12	12	11	12	12
Sampling rate (MS/s)	110	75	45	100	100
INL (LSB)	+1/–1.5	+0.95/–0.93	+1.1/–1	+0.4/–0.6	+0.46/–0.62
DNL (LSB)	+1.2/–1.2	+0.3/–0.64	+0.45/–0.4	+0.1/–0.08	+0.21/–0.22
SFDR (dBc)	69.4	71.2	70	85<2>	79.8
SNDR (dB)	64.2	63.5	60.1	66<2>	65.1
Power (mW)	97<1>	308	90.5	205	112
FOM (pJ/step)	0.67<1>	3.36	2.43	1.26	0.76

* <1> analog power consumption; <2> input frequency is 2 MHz.

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