MOS structure fabrication by thermal oxidation of multilayer metal thin films

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Abstract: A novel approach for the fabrication of a metal oxide semiconductor (MOS) structure was reported. The process comprises electrochemical deposition of aluminum and zinc layers on a base of nickel–chromium alloy. This two-layer structure was thermally oxidized at 400 ℃ for 40 min to produce thin layers of aluminum oxide as an insulator and zinc oxide as a semiconductor on a metallic substrate. Using deposition parameters, device dimensions and SEM micrographs of the layers, the device parameters were calculated. The resultant MOS structure was characterized by a C–V curve method. From this curve, the device maximum capacitance and threshold voltage were estimated to be about 0.74 nF and –2.9 V, respectively, which are in the order of model-based calculations.

Key words: MOS structure; electrochemical deposition; thermal oxidation; C–V curve
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1. Introduction

Deposition of a thin layer of materials on an object is of prime technical importance. These films can be used for a variety of industrial applications. In the microelectronics industry, various layers of semiconductors, dielectrics and conductors are necessary to complete the components and facilitate the integration of them into the circuit[1].

Thin layers can be created by a number of techniques, such as chemical vapor deposition (CVD)[2], physical vapor deposition (PVD) and electrochemical deposition. Amongst various deposition techniques, the electrochemical method which is often called "electroplating" is attractive due to its simplicity, low cost, low temperature and capability of significant production[3]. This method has been widely used for the growth of various films such as metallic[4, 5], metallic alloys[6], semiconductors[7] and dielectric[8]. Recently, more effort is being made in the deposition of multi-layers, such as metal–insulators[9, 10].

In this paper, we propose a simple technique for the fabrication of double layers of oxide and semiconductor on a metal substrate, which can be used as a metal oxide semiconductor (MOS) structure. The oxide and semiconductor in this research are Al_2O_3 and ZnO, respectively. A MOS structure is a very useful device in the study of semiconductor surfaces. Recently, such structures have been proposed as sensing elements in sensors[11], such as gas and magnetic field sensors[12].

The fabrication process comprises electrochemical deposition and post oxidation of suitable metallic films on a Cr–Ni alloy substrate. The thermal oxidation of metals is a cost effective method for the fabrication of oxide layers and recently has been used for the fabrication of high temperature diodes[13] and Schottky-type gas sensors[14]. Electrical measurements are employed to judge the process and predict the electrical behavior of the layers. On the other hand, the capacitance of the whole structure is recorded at different voltages as a capacitance versus voltage (C–V) curve to certify the formation of a MOS structure and estimate its relevant threshold voltage.

It has been shown that the charge concentration in a semiconductor–oxide boundary can shift the C–V curve of MOS structures[15]. On the other hand, ZnO is a gas sensitive material and its interface trapped charge density varies as a function of the surrounding gas nature and concentration[16, 17]. So the presence of a contamination gas is expected to affect the C–V curve of our device. This phenomenon leads us to use this device as a capacitive gas sensor. More information about the application of the proposed device for gas detection will be reported elsewhere.

2. Theory

2.1. MOS structure

A schematic of the proposed structure, as well as its corresponding band diagram, is given in Fig. 1. In this figure, we have assumed the ideal situation in which the semiconductor is a single crystal and the charge concentration in the oxide–semiconductor interface is zero. It is important to note that these assumptions result in deviations between theoretical and experimental results.

In this figure, $\phi_{\rm m}$ is the metal work-function. χ and $E_{\rm g}$ are the electron affinity and energy band-gap of the semiconductor, respectively. $\psi_{\rm B}$ is the potential difference between the Fermi level $E_{\rm F}$ and the intrinsic level $E_{\rm i}$ of the semiconductor, which is known as the bulk potential[15]. Except for $E_{\rm F}$, all parameters are physical constants of the materials and their typical values can be found in Refs. [18, 19], as shown in Table 1. On the other hand, the semiconductor characteristic $\psi_{\rm B}$ and its value can be calculated from $\psi_{\rm B} = E_{\rm g}/2-(E_{\rm F}-E_{\rm C})$. Experimental measurements in the next section indicate that $E_{\rm F}$ is 0.019 eV under the $E_{\rm C}$, so we have $\psi_{\rm B} = 1.656$ eV.

The semiconductor work-function is another important parameter in MOS structure and can be calculated from $\phi_{\rm s} = \chi + (E_{\rm C} - E_{\rm F})$. Using the above parameters, the value of $\phi_{\rm s}$ will be about 4.369 eV, which is less than the metal work func-

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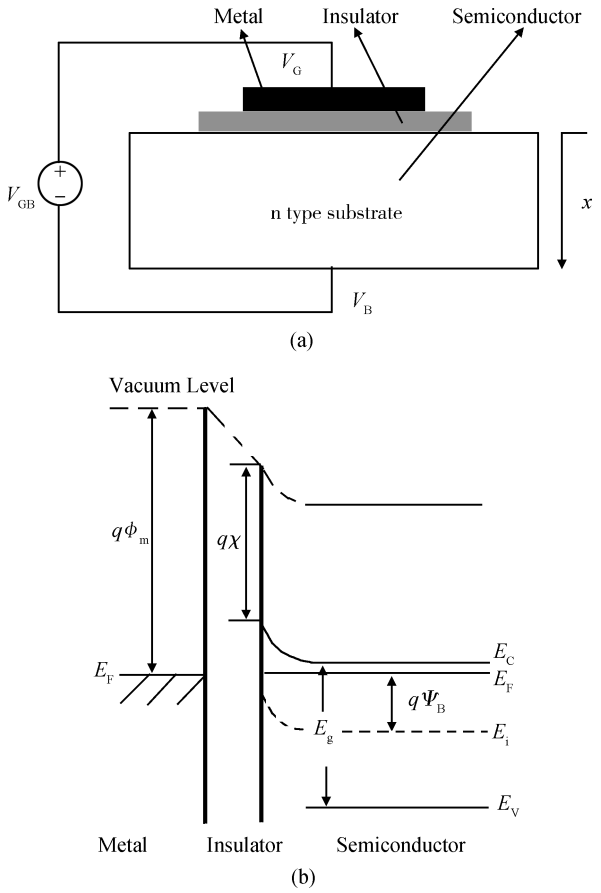


Fig. 1. (a) MOS capacitor structure. (b) Energy band diagram of MOS capacitor before voltage application.

Table 1. Parameters of proposed system.

Parameter	E_g	ψ_B	χ	ϕ_m	χ_i
Value	3.35	1.495	4.35	5.3	1.35

tion, $\phi_m = 5.2$ eV. In this case, we have $\phi_{ms} = \phi_m - \phi_s = 0.87 > 0$ and the semiconductor surface will be depleted from free electrons and its energy bans bends upward, as shown in Fig. 1. The value of band bending is known as surface potential. By connecting the external voltage with the appropriate polarity, it is possible to increase this bending. If the surface potential increases beyond twice the bulk potential, $2\psi_B$, the junction will be in the strong inversion condition. In this case, the voltage across the MOS device is known as the threshold voltage, V_T, which is an important parameter of any MOS structure. So, in the absence of any interface and oxide charges the threshold voltage, V_T, can be calculated from[16]

$$V_T = \frac{1}{q}\left(\phi_{ms} - 2\psi_B - \frac{Q_{SD}}{t_{ox}}\right), \quad (1)$$

where Q_{SD} is the charge density per unit area in the depletion region and t_{ox} is the oxide layer thickness. In the present prototype, t_{ox} is large enough to ignore the last term of Eq. (1). In such a case, the threshold voltage is in the order of $(\phi_{ms} - 2\psi_B)/q$, which is equal to –2.44 V. This value will be verified experimentally by studying the device's C–V curve.

2.2. The C–V curve of the MOS structure

The C–V curve is a specific characteristic of any MOS capacitor and gives complete information about the semiconductor and the oxide properties. In the calculation of the MOS capacitor, the depletion region at the semiconductor surface is taken as a dielectric in series with the insulator, so the equivalent MOS capacitance, C, is assumed as a series combination of the insulator capacitance C_i and the semiconductor depletion-layer capacitance C_d, as below,

$$C = \frac{C_i C_d}{C_i + C_d}. \quad (2)$$

The insulator capacitance is constant, corresponds to the maximum capacitance of the system and can be calculated from

$$C_i = \varepsilon\varepsilon_0 \frac{A}{d}. \quad (3)$$

In the present research, $\varepsilon \approx 9$ is the Al_2O_3 dielectric constant, $\varepsilon_0 = 8.85 \times 10^{-14}$ F/cm is the free space permittivity, and d and A are the insulator thickness and device area, respectively. Based on the experimental results in the next section, d and A are in the order of 20 μm and 0.44 cm^2, respectively, so the maximum capacitance is estimated to be about 0.17 nF. We will show by measurement that, although the experimental value of the capacitance is in range of this estimation, the ignored parameters have a considerable effect on the final result.

On the other hand, the depletion capacitance C_d depends on the depletion-layer width (then applied voltage across the semiconductor) as well as the measurement frequency. It has been shown that a minimum low frequency capacitance C_{min} occurs in the vicinity of the threshold voltage, V_T, in which the depletion layer width is at a maximum[17]. So by recording the device capacitance versus the voltage as a C–V curve from the experimental data, the threshold voltage can be anticipated experimentally.

3. Experimental

3.1. Layer deposition

The experimental verification of the proposed method was accomplished by fabrication and test of a prototype structure. In contrast with the ordinary MOS fabrication technology, the proposed method was started by a metal substrate, and oxide and semiconductor layers were deposited on it.

A wire of nickel–chromium alloy, which is commercially available as heating elements, was used as the starting substrate. This specification of the substrate is useful for self heating of the final instrument. The length and diameter of the substrate were 80 mm and 0.2 mm, respectively. After substrate preparation, the fabrication process was performed as below:

(1) successive deposition of aluminum and zinc films on metal substrate;

(2) selective deposition of Ag film;

(3) thermal oxidation of multi layer structure;

(4) connection of ohmic contacts.

The deposition process was carried out in a conventional electrolytic cell as schematically depicted in Fig. 2. This comprises a 500 cm^3 borosilicate beaker; the electrolyte, which was

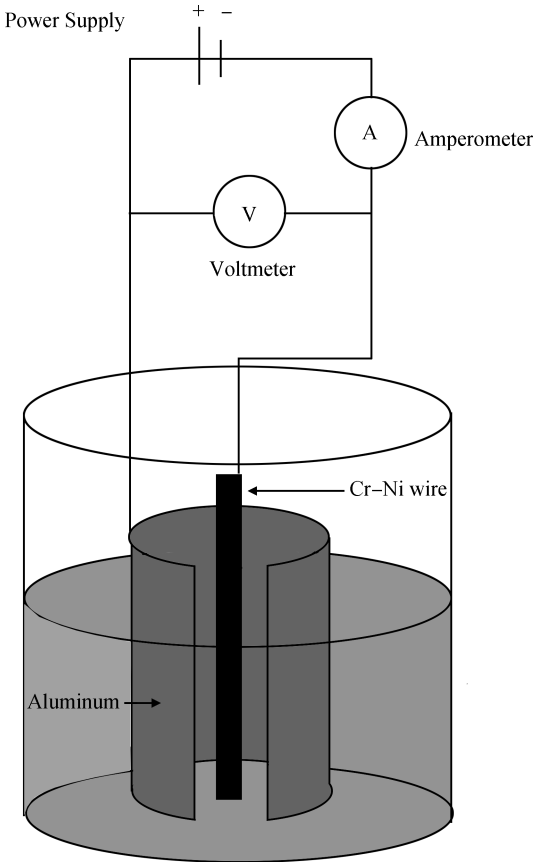


Fig. 2. Schematics of electrolytic cell for deposition of aluminum on Cr–Ni wire.

a water-soluble salt of under deposition metal; a DC power supply; and the relevant electrodes.

In the Al deposition stage, the electrolyte was 25 g of aluminum sulfate ($Al_2(SO_4)_3$) dissolved in 200 cm^3 of aquapura. The anode and cathode were connected to pure Al foil and Cr–Ni substrate, respectively. Upon connection of the electrodes to the power supply, electrolysis was started. During this process, the Al ions were attracted by the substrate and deposited on it. The deposition was performed at room temperature for 6 min. The applied voltage was 10 V but the current began at 2.5 mA and increased to 120 mA at the end of the deposition time. So the average value of the current can be taken as about 60 mA. Using the above parameters, the coated Al mass and volume were estimated as about 2 mg and 7.5×10^{-4} cm^3, respectively. Using the geometrical dimensions of the substrate and considering the film porosity (see below), the Al film thickness will be about 16 μm. To control the insulator capacitance value, the Al thickness should be controlled by variation of the current or deposition time.

In the second stage, the middle part of the sample was coated with a thin layer of zinc. At this stage, electrolyte was replaced with 10 g of zinc sulfate ($ZnSO_4$) dissolved in 100 cm^3 of aquapura and the anode electrode was replaced by zinc foil. At this stage, the deposition time was about 10 min and the applied voltage and average current were 12 V and 175 mA, respectively. In this condition, only 70 mm of the wire was coated, so the estimated thickness of Zn layer will be about 113.7 μm.

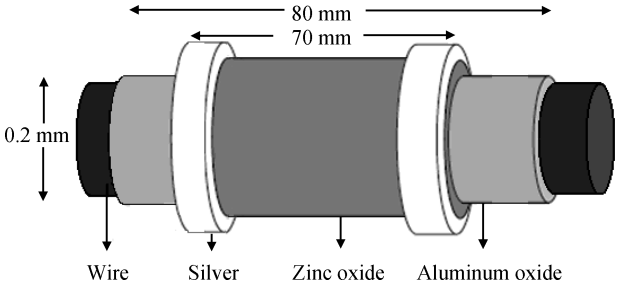


Fig. 3. Schematics of the fabricated MOS structure.

In the third stage, the silver layer was selectively deposited on the front and end of the Zn layers for metallization. Ag coated regions will be used as the metallized area for connection of the ohmic contacts to the final semiconductor (ZnO) layer. Electrolyte at this stage was silver nitrate ($AgNO_3$) solution and the anode metal was replaced with Ag wire. More details about the deposition process can be found in Ref. [18].

3.2. Sample preparation

The next stage of the process was thermal oxidation of the zinc–aluminum multilayer. In this stage, the prototype was gradually heated up to 400 ℃ by an electric furnace and kept there for 40 min. As a result of this heating in air ambient, the aluminum and zinc films were oxidized and converted to the insulator and semiconductor, respectively. Considering full oxidation of the Al and Zn layers and taking account of the porosity and density of the Al_2O_3 and ZnO layers, their thickness was estimated to be about 20 μm and 175 μm, respectively. On the other hand, at this temperature the substrate (Cr–Ni alloy) and silver layers withstand oxidation and remain unchanged because of their oxidation resistance. The resultant MOS structure is shown schematically in Fig. 3.

For the electrical connections, thin copper wires were cemented to silver metallic areas by conductive carbon paste and gradually heated up to 200 ℃ for contact stabilization. Finally, the metal contacts were tested to be ohmic.

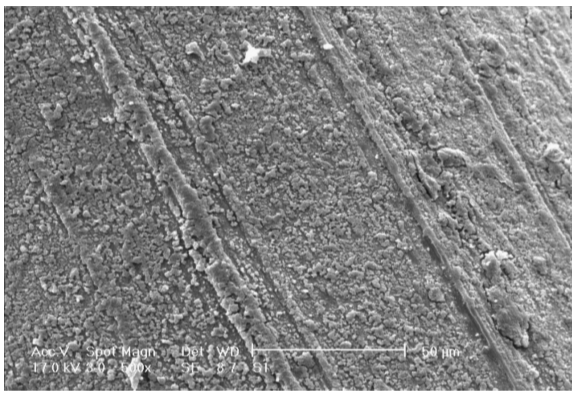
4. Results and discussion

4.1. Microstructure of insulator layer

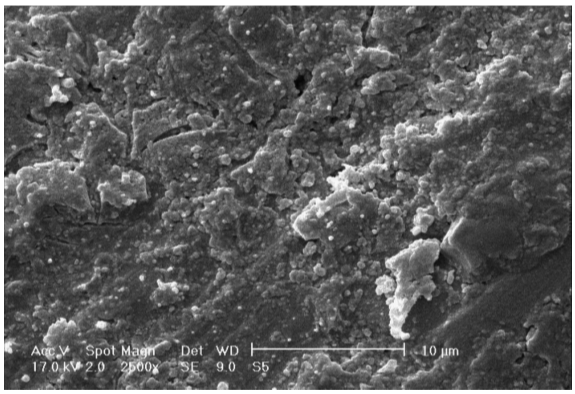
The insulator layer thickness is a key factor in controlling MOS capacitance. So, in order to achieve a more accurate estimation from the thickness of this layer, the morphology of the Al_2O_3 film was examined by scanning electron microscope (SEM). Figure 4(a) shows a micrograph of a deposited Al layer after oxidation, which indicates a porous layer on the substrate surface. Using this figure, the apparent porosity of the Al_2O_3 films was estimated to be about 10%. This value of porosity was taken account of in the calculation of the layer thickness. It is important to note that insulator layer non-uniformity is expected to cause a considerable deviation between the experimental and calculated value of the device capacitance.

4.2. Semiconductor layer

A micrograph of a ZnO layer is shown in Fig. 4(b). This shows the ZnO layer as a flaky film with some micro-cracks.



(a)



(b)

Fig. 4. Micrograph of deposited layers after oxidation. (a) Al_2O_3. (b) ZnO.

The cracks are useful for utilization of the device as a gas sensor. The morphology of this layer is different from that of the oxide layer, but their porosity can be supposed to be the same. This value was also taken account in calculating the semiconductor layer thickness.

Since the ZnO layer acts as the semiconductor part of the final MOS device, so its semiconductor characteristic was verified by recording its electrical conductivity versus the temperature. In such a case, the conductivity can be expressed as[19]

$$\sigma = \sigma_0 \exp\left[-(E_C - E_D)/2k_B T\right], \tag{4}$$

or equivalently

$$\lg \sigma(T) = \lg \sigma_0 - \frac{E_C - E_D}{kT}, \tag{5}$$

where E_C and E_D are conduction and donor levels, respectively, and their difference, $E_C - E_D$, is known as the activation energy, E_A, of carrier generation. T is the absolute temperature, $k = 1.380066 \times 10^{-23}$ (J/K) is Boltzmann's constant and σ_0 is a conductivity pre-factor.

To do this, the electrical resistance of the layer was measured via the two predicted ohmic contacts on the ZnO surface at different temperatures from room temperature up to 850 ℃. The result of this measurement was used to draw lg $(1/R)$ verses $1000/T$, as an Arrhenius plot, which is depicted in Fig. 5.

The resultant curve is linear with a negative slope, which indicates a semiconductor property of the ZnO layer. On the other hand, using the absolute value of the slope, the activation energy, E_A, was calculated as below,

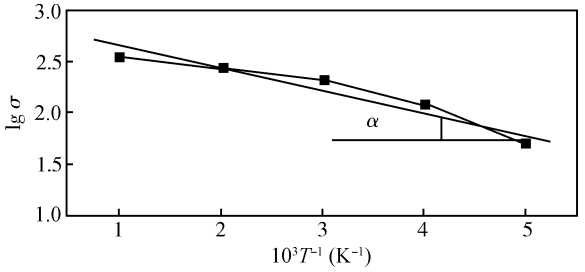


Fig. 5. Arrhenius plot for ZnO layer.

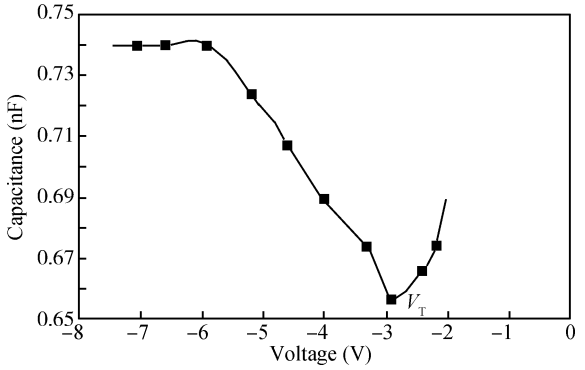


Fig. 6. Experimental of capacitance versus voltage (C–V) curve for the sample and estimated value of V_T.

$$\tan\alpha = -\frac{E_A}{1000}\frac{1000}{kT} = \frac{1.7-2.6}{5-1} = -0.225, \tag{6}$$

so we have

$$E_A = 0.225 \times 1000\,k = 0.31 \times 10^{-20}\ \text{(J)}, \tag{7}$$

or equivalently

$$E_A = \frac{0.31 \times 10^{-20}}{1.6 \times 10^{-19}} = 1.938 \times 10^{-2}\ \text{(eV)}. \tag{8}$$

This activation energy belongs to dominant trap levels in the ZnO forbidden gap and its value is in the order of what has been reported by researchers of ZnO films prepared by other methods[19]. Assuming the ionization of all donors, E_A can be considered as a good approximation for $E_C - E_F$ in the forbidden gap[20].

4.3. MOS capacitance

In the final stage of verification, the C–V curve of the prototype was recorded. The MOS capacitance is a small signal or AC parameter and is generally measured by superimposing a small AC voltage on an applied DC voltage. The capacitance value, then, is measured as a function of the applied DC voltage. Using this method, the device capacitance at different values of DC voltages was calculated and recorded as a C–V curve, as depicted in Fig. 6. This curve is similar to that of prevalent MOS devices and confirms the formation of a MOS structure. As Figure 6 shows, the C–V curve contains a local

minimum of –2.9 V, which can be taken as an experimental value of the threshold voltage, V_T. This value is in the order of what was calculated by Eq. (1). On the other hand, the maximum value of the capacitance, or equivalently the insulator capacitance C_i, is about 0.74 nF, which is in the same order of magnitude to what was estimated by theoretical analysis in Eq. (3).

Although we ignored some non-ideal parameters in our theoretical model analyses, it is obvious that the discrepancy between experimental and theoretical estimations is in an acceptable range, and that can be considered a result of simplifying assumptions in theoretical models such as oxide thickness non-uniformity, interface charges and also measurement system errors.

5. Conclusion

We have shown that the fabrication of a MOS structure using electrochemical deposition and post oxidation of multilayer metal films is possible. This method is simple and cost effective. Characterization of deposited layers and adequate test of the MOS device confirms the capability of the proposed method. On the other hand, by recording the device capacitance at different DC voltages as a C–V curve, its threshold voltage and insulator capacitance, C_i, were estimated to be about –2.9 V and 0.74 nF, respectively. These values are comparable to what was estimated by model base calculation and some inequality can be related to non-ideality of structure and simplification in the considered model. In addition to simplicity and effectiveness of the proposed method for the fabrication of a MOS structure, this research shows that this method can be applied to the fabrication of other multi-layers structures.

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