A novel low-offset dynamic comparator for sub-1-V pipeline ADCs*

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Abstract: A novel low-offset dynamic comparator for high-speed low-voltage analog-to-digital converters (ADCs) has been proposed. In the proposed comparator, a CMOS switch takes the place of the dynamic current sources in the differential comparator, which allows the differential input transistors still to operate in the saturation region at the comparing time. This gives the proposed comparator a low offset as the differential comparator while tolerating a sub-1-V supply voltage. Additionally, it also features a larger input swing, less sensitivity to common mode voltage, and a simple relationship between the input and reference voltage. This proposed comparator with two traditional comparators has been realized by SMIC 0.13 μm CMOS technology. The contrast experimental results verify these advantages over conventional comparators. It has been used in a 12-bit 100-MS/s pipeline ADC.

Key words: comparator; high speed; low voltage; low offset; ADC
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1. Introduction

Pipeline analog-to-digital converters (ADCs) are widely used in applications that require high speed, medium resolution and low power consumption. Each pipeline stage consists of a sub-ADC and a multiplying digital-to-analog converter (MDAC). Comparators are the core of the sub-ADCs. The employment of the redundant-signed-digit (RSD) correction makes the offset requirement less stringent than that of other ADCs. Hence, fairly simple dynamic comparators can be used to further reduce power consumption. However, as the supply voltage scales with device dimension, the offset tolerated by RSD becomes smaller. Moreover, a larger input swing, less power consumption, and higher comparing speed are always the objects of comparator design. Traditional comparators suffer from drawbacks of excessive offset[1], large metastable delay time[2−5], high operation voltage[2, 4−6] and greater power consumption[7]. To solve these problems, some improved dynamic comparators have been proposed[8, 9], which introduce multi-stage amplification or positive feedback techniques. This paper will also provide a novel competitive choice in the high speed low voltage pipeline ADC design.

2. Traditional dynamic comparators

2.1. Resistive divider comparator

The comparator shown in Fig. 1 is called a resistive divider comparator[1], because the input pairs (M1–M4) operate in the deep linear region and adjust the trip point of the comparator resistively by means of

$$V_{\rm in}^{+} - V_{\rm in}^{-} = \frac{\beta_1}{\beta_2}\left(V_{\rm ref}^{+} - V_{\rm ref}^{-}\right), \qquad (1)$$

where

$$\beta_1 = \mu_{\rm n} C_{\rm ox}\frac{W_1}{L_1} = \mu_{\rm n} C_{\rm ox}\frac{W_2}{L_2},$$

$$\beta_2 = \mu_{\rm n} C_{\rm ox}\frac{W_3}{L_3} = \mu_{\rm n} C_{\rm ox}\frac{W_4}{L_4}.$$

This comparator is widely used because of its low kickback noise and simple relationship between input voltage and reference voltage, as expressed in Eq. (1). Additionally, the input can be as low as one threshold voltage $V_{\rm thn}$ and therefore it can be used in low supply voltage. However, since M1–M4 are in the deep linear region while M5–M6 are in the saturation region, the input-referred offset is sensitive to the device mismatch of M1–M4 and M5–M6, especially M5–M6. The offset can reach over hundreds of millivolts, which is unbearable in pipeline ADCs.

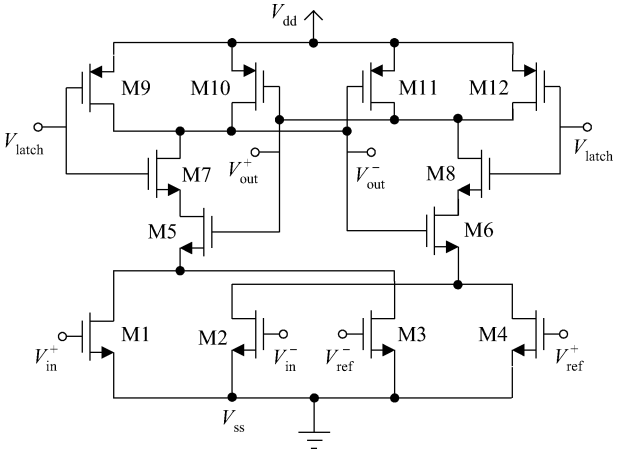

Fig. 1. Resistive divider comparator.

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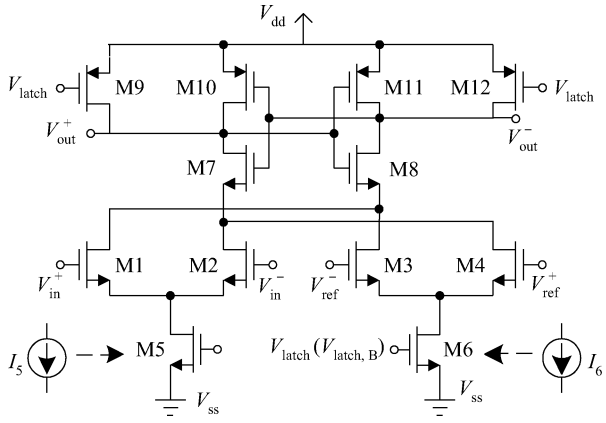

Fig. 2. Differential pair comparator.

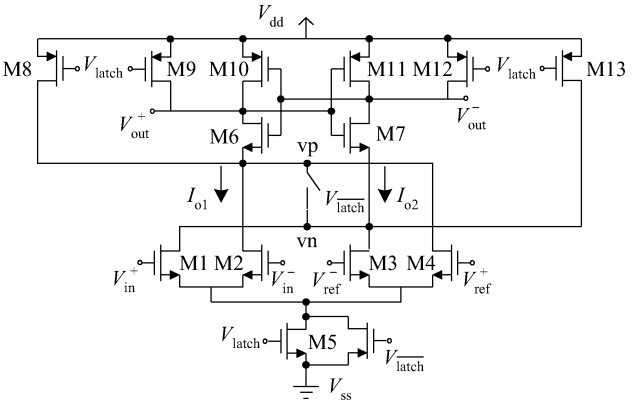

Fig. 3. Proposed comparator.

2.2. Differential pair comparator

A fully differential dynamic comparator with current sources controlled by V_{latch} is shown in Fig. 2[2, 4, 6]. All of the differential pairs and current source transistors are in the saturation region at the regeneration time, which makes the offset insensitive to device mismatch. To ensure this condition, the current source controlled clock should have a long transition time[2, 4] or restricted voltage[6] less than V_{dd}. The trip point of the comparator depends on the imbalance between the differential pairs and the switch controlled current sources. However, several drawbacks compromise its applications. Firstly, the nonlinear relationship between the input and reference voltage[2, 4] as Eq. (2) makes it difficult to determine the trip point ($V_{\text{in}} = eV_{\text{ref}}$). As a result, to achieve the ideal trip point, designers often use simulation tools to iterate.

$$2de^2 I_6 \frac{W_1}{L} - K'e^4 V_{\text{ref}}^2 \left(\frac{W_1}{L}\right)^2 = 2I_6 \frac{W_3}{L} - K' V_{\text{ref}}^2 \left(\frac{W_3}{L}\right)^2, \tag{2}$$

where

$$I_5 = dI_6, \quad V_{\text{in}} = eV_{\text{ref}}, \quad W_1 = W_2, \quad W_3 = W_4,$$

$$K' = \mu_{\text{n}} C_{\text{ox}}, \quad V_{\text{in}} = V_{\text{in}}^+ - V_{\text{in}}^-, \quad V_{\text{ref}} = V_{\text{ref}}^+ - V_{\text{ref}}^-.$$

Secondly, since there are dynamic current sources in the tail of the source coupled pairs, the input voltage and reference voltage have to be above $V_{\text{thn}} + 2V_{\text{dsatn}}$, where V_{dsatn} is the corresponding overdrive voltage. A large input swing or too low a common input voltage will lead to turning off one of the differential pairs and all of the tail current will converge into the other transistors. As a result, the comparator only compares V_{in}^+ with V_{ref}^+ (or V_{in}^- with V_{ref}^-) rather than differential V_{in} with differential V_{ref}. The trip point will deviate from the ideal value as the theory predicts. It is worse in the condition of 1.2 V or lower supply voltage. Thirdly, there is a problem with the previous comparing result affecting the next decision when there is some charge imbalance left in the drain of the differential pairs from the previous comparing result.

3. Proposed dynamic comparator

3.1. Introduction

To overcome the drawbacks of the two comparators mentioned above and to exploit their advantages, some improvements are introduced to make the proposed comparator not only insensitive to device mismatch but also capable of operating at lower supply voltage and larger input swing. The basic idea is to ensure that all of the comparing transistors (M1–M4) are always working in the saturation region at the regeneration time while other transistors that consume the voltage margin are removed. To achieve these objectives, the proposed dynamic comparator[10] removes two current sources from the tail of the differential pair in Fig. 2, and replaces them with a CMOS switch (or NMOS switch) controlled by a clock, as shown in Fig. 3. The difference between the current sources and the CMOS switch will be addressed in detail below.

3.2. Operation of the comparator

The key point in designing this comparator is that the W/L of M5 should be designed large enough (16 μm/0.13 μm in this design) and the transition time of the controlled logic signal V_{latch} should be as short as possible to make sure that the source of the differential pairs can be pulled down to V_{ss} quickly at the regeneration moment. Actually, M5 acts as a switch controlled by a logical signal V_{latch}. An alternative implementation is to use a CMOS switch, as plotted with grey lines in Fig. 3. As a result, the input can be as low as one threshold voltage in the regeneration time, and therefore a larger input swing or a lower input common voltage can be achieved.

The operation of the comparator is as follows. When the comparator is reset, the switch M5 is cut off. There is no static current from V_{dd} to V_{ss}. The nodes of vp and vn are pulled up to V_{dd}. Once V_{latch} goes to V_{dd}, the sources of the differential pairs are pulled down to V_{ss} by switch M5, while the drain of the differential pairs (vp and vn) are still close to 1.2 V because of no transient current from V_{dd} to V_{ss} at this right time. Therefore, transistors M1–M4 are in the saturation region at this moment.

In the meantime, the comparator begins to compare the input voltage and reference voltage. The ratio of the size between the input transistors and reference transistors determines the

trip point. M1–M4 follow the large signal current equations,

$$I_{o1} = \beta_1 \left(V_{in}^- - V_{thn}\right)^2 + \beta_2 \left(V_{ref}^+ - V_{thn}\right)^2, \quad (3)$$

$$I_{o2} = \beta_1 \left(V_{in}^+ - V_{thn}\right)^2 + \beta_2 \left(V_{ref}^- - V_{thn}\right)^2, \quad (4)$$

where

$$\beta_1 = \frac{1}{2}\mu_n C_{ox}\frac{W_1}{L_1} = \frac{1}{2}\mu_n C_{ox}\frac{W_2}{L_2},$$

$$\beta_2 = \frac{1}{2}\mu_n C_{ox}\frac{W_3}{L_3} = \frac{1}{2}\mu_n C_{ox}\frac{W_4}{L_4}.$$

Given

$$V_{in,com} = \left(V_{in}^+ + V_{in}^-\right)/2 = \left(V_{ref}^+ + V_{ref}^-\right)/2, \quad (5)$$

the trip point can be derived as

$$V_{in}^+ - V_{in}^- = \frac{\beta_2}{\beta_1}\left(V_{ref}^+ - V_{ref}^-\right). \quad (6)$$

Equation (6) is similar to that of the resistive divider comparator as expressed in Eq. (1). However, Equation (6) is based on the input transistors operating in the saturation region, which is insensitive to device mismatch.

It is worth noting that vp and vn are shorted in the reset time for the purpose of eliminating the effect of last comparing result on the next decision.

3.3. Offset

Since the differential pairs of proposed comparator are in the saturation region at the regeneration moment, the offset is little affected by the transistor mismatch, which is similar to that of the differential pair comparator. In other words, this proposed comparator is adaptive to the supply voltage as low as that of the resistive comparator while the offset is as low as that of the differential pair comparator.

The total offset voltage of the comparator is expressed in Eq. (7). The offset of one differential pair has the well known dependency on the mismatch of the threshold voltage ΔV_T, load resistance ΔR_L, transistor dimensions $\Delta\beta$ and their corresponding average values (V_T, R_L, β). This equation is also the same with a differential pair comparator[2].

$$V_{os} = \Delta V_T + \frac{V_{gs} - V_T}{2}\left(\frac{\Delta\beta}{\beta} + \frac{\Delta R_L}{R_L}\right). \quad (7)$$

4. Experimental results and analysis

This comparator with two traditional comparators mentioned in Section 2 is designed and fabricated by SMIC 0.13 μm CMOS technology. The micrograph of these three comparators is shown in Fig. 4. It should be noted that an internal buffer is added to drive the capacitive load introduced by the pads and probes.

The transistor dimensions are presented in Table 1. The M1–M4 are sized so that the comparator trip point is set to $V_{in} = (1/4)V_{ref}$, corresponding to the situation in a 1.5-bit pipeline stage. It should be noted that the coefficient of 1/4 is simply realized by $(W_1/L_1)/(W_3/L_3) = (W_2/L_2)/(W_4/L_4) = 1/4$ in the resistive and proposed comparators.

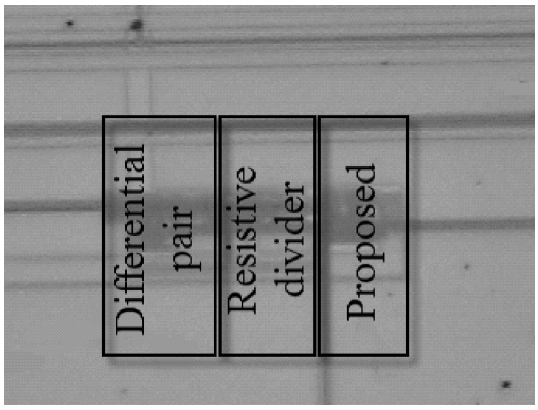

Fig. 4. Micrograph of three comparators.

Table 1. Correspondence value of MCy and yield.

Trans.	Res. divider		Diff. pair		Proposed	
	W	*L*	*W*	*L*	*W*	*L*
M1	8.0	0.13	4.0	0.13	8.0	0.13
M2	8.0	0.13	4.0	0.13	8.0	0.13
M3	2.0	0.13	2.0	0.13	2.0	0.13
M4	2.0	0.13	2.0	0.13	2.0	0.13
M5	2.0	0.13	2.0	1.0	16.0	0.13
M6	2.0	0.13	1.0	1.0	2.0	0.13
M7	4.0	0.13	2.0	0.13	2.0	0.13
M8	4.0	0.13	2.0	0.13	4.0	0.13
M9	4.0	0.13	4.0	0.13	4.0	0.13
M10	2.0	0.13	2.0	0.13	2.0	0.13
M11	2.0	0.13	2.0	0.13	2.0	0.13
M12	4.0	0.13	4.0	0.13	4.0	0.13
M13					4.0	0.13

Table 2. Simulation results.

Comparator	Average power (μW)	Offset voltage (mV)	Metastable delay time (ps)
Resistive	24.2	338.0	217.5
Differential	56.8	23.2	546.6
Proposed	50.9	17.8	136.3

Table 2 shows the simulation results, which compare the comparator performance in terms of average power, offset voltage, and metastable delay time. The comparison of offset voltages is in agreement with the discussion in Sections 2 and 3. However, to achieve low offset, the input transistors of the proposed comparator must work in the saturation region, and the drain of the input transistors has to be pulled up to V_{dd} in the reset phase. As a result, its dynamic average power is larger than that of the resistive comparator. It should be noted that the offset voltage, which is introduced by process variation and device mismatch, is obtained from 1000 Monte Carlo results.

The functional performance is shown in Fig. 5. The sine wave is the differential input whose swing ($V_{in,swing} = 2\left(V_{in}^+ - V_{in}^-\right) = 2\left(V_{ref}^+ - V_{ref}^-\right)$) is 831 mV, and the square wave is the comparator's output. The trip point is the input voltage at the time when the output changes its logic state.

V_{dd}, $V_{in,com}$, $V_{in,swing}$ are three factors that influence the trip point. To evaluate these influences, the following three mea-

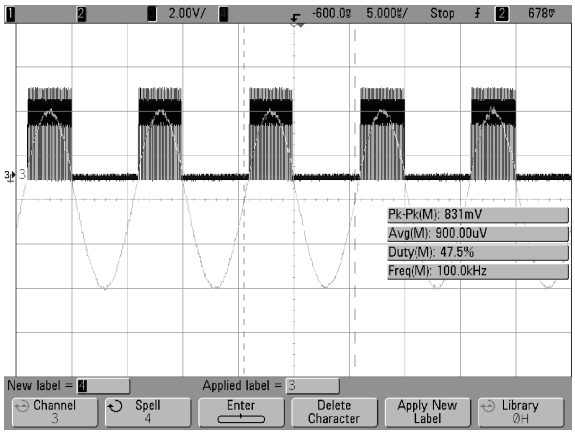

Fig. 5. Measured transient waveforms.

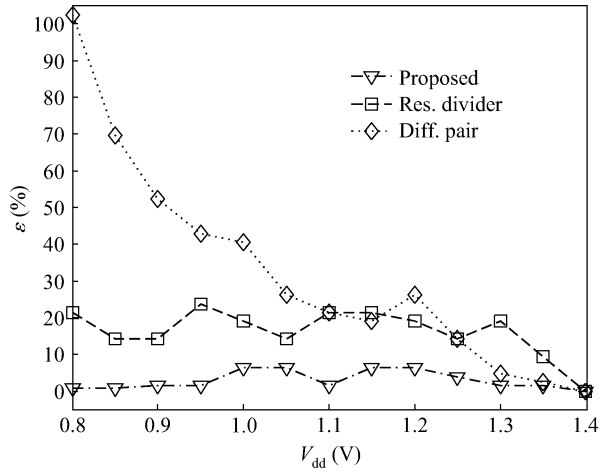

Fig. 6. Measured trip point error as a function of V_{dd}.

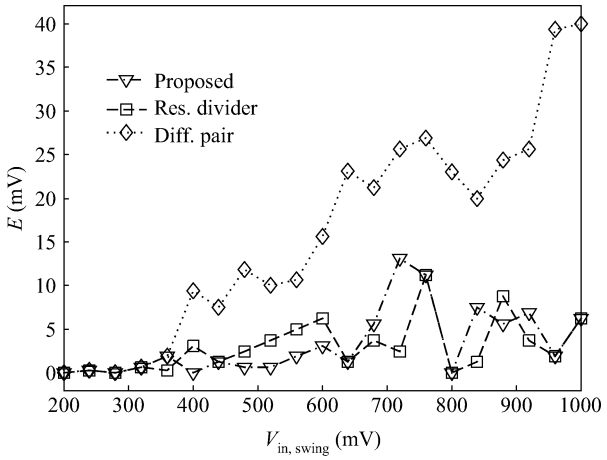

Fig. 7. Measured E as a function of differential input swing.

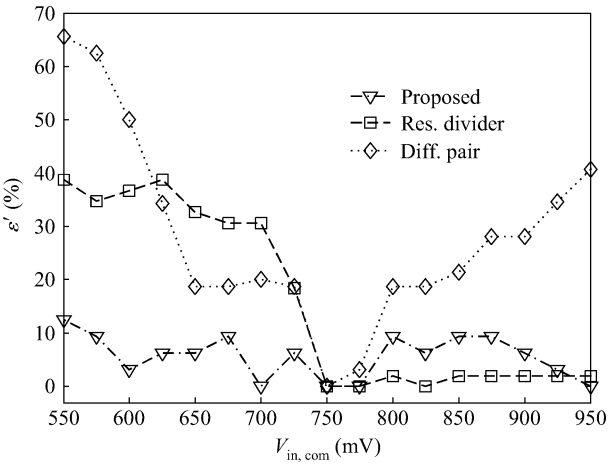

Fig. 8. Measured trip point error as a function of $V_{in, com}$.

surements are based on single-variable control experiment, i.e., one variable is changed while the others are fixed.

In the condition of $V_{in, cm} = 650$ mV, $V_{in, swing} = 800$ mV, trip points are measured at different V_{dd}. Here, we use the trip point error to evaluate the deviation, which is defined as

$$\varepsilon = \left| \frac{V_{trip} - V_{trip, 1.4}}{V_{trip, 1.4}} \right| \times 100\%, \tag{8}$$

where $V_{trip, 1.4}$ is the trip point at $V_{dd} = 1.4$ V and V_{trip} represents different trip points at different V_{dd}. Figure 6 shows the relationship between the trip point error and V_{dd}, indicating that the trip point of the proposed comparator is less sensitive to V_{dd} compared with differential comparators or resistive comparators. This is also predicted by the analysis in Sections 2 and 3.

Figure 7 shows the relationship between the differential input swing ($V_{in, swing}$) and E, which is defined as

$$E = \left| V_{real, trip} - V_{ideal, trip} \right|. \tag{9}$$

It is in the condition of $V_{dd} = 1.2$ V, $V_{in, com} = 650$ mV. As depicted above, the resistive divider comparator and the proposed comparator can tolerate a larger input swing and have a similar curve while the real trip point of the differential pair comparator deviates from the ideal value once the input swing becomes large. The reason has also been analyzed in Section 2.

In the condition of $V_{dd} = 1.2$ V and $V_{in, swing} = 800$ mV, trip points are measured at different $V_{in,com}$. Here, we use the trip point error to evaluate the deviation, which is defined as

$$\varepsilon' = \left| \frac{V_{trip} - V_{trip, 750}}{V_{trip, 750}} \right| \times 100\%, \tag{10}$$

where $V_{trip, 750}$ is the trip point when $V_{in, com} = 750$ mV. V_{trip} represents different trip points corresponding to different $V_{in, com}$. Figure 8 shows the relationship between the trip point error and $V_{in, com}$. As shown in Fig. 8, when $V_{in, com}$ increases towards 950 mV, the four input transistors of the differential pair comparator begin to get into the linear region. The characteristic of ε' versus $V_{in, com}$ begins deviating from the ideal value that is set in the condition of all the transistors in the saturation region, while the resistive divider comparator and the proposed comparator still work in their proper region (the resistive divider comparator is in the deep linear region and the proposed comparator is in the saturation region). So their trip point errors are not as large as the differential pair comparator. When $V_{in, com}$ decreases towards 550 mV, one of the input transistors in the differential pair comparator (V_{in}^{-} with V_{ref}^{-} or V_{in}^{+} with V_{ref}^{+}) goes into the cutoff region and the dynamic cur-

Table 3. Performance comparison.

Comparators	Power	Offset	Delay	$V_{\text{in, swing}}$	V_{dd}	$V_{\text{in, com}}$
Resistive	√	×	−	√	−	×
Differential	−	√	×	×	×	×
Proposed	−	√	√	√	√	√

√: Good. −: Average. ×: Poor.

rent sources no longer work in the saturation region. For the resistive comparator, once the input voltage falls lower than $V_{\text{ds}} + V_{\text{th}}$, the resistive divider comparator will work in the saturation region. Neither of the two traditional comparators not work in their proper region any longer. However, the proposed comparator keeps working in the saturation region as usual. As a result, a small trip point error is achieved from 550 to 950 mV.

5. Conclusion

In this paper, a new mismatch insensitive dynamic comparator has been proposed by using a switch to control the source voltage of the differential pairs. Compared with two traditional comparators, simulation and measured results verify its advantages of low offset, high speed, low supply voltage, large input swing and insensitivity to input common voltage. Table 3 summarizes the performance comparison between these three comparators. Therefore, it can be widely used in sub-1-V pipeline ADCs.

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