

An SPICE model for phase-change memory simulations*

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Abstract: Along with a series of research works on the physical prototype and properties of the memory cell, an SPICE model for phase-change memory (PCM) simulations based on Verilog-A language is presented. By handling it with the heat distribution algorithm, threshold switching theory and the crystallization kinetic model, the proposed SPICE model can effectively reproduce the physical behaviors of the phase-change memory cell. In particular, it can emulate the cell's temperature curve and crystallinity profile during the programming process, which can enable us to clearly understand the PCM's working principle and program process.

Key words: phase-change memory; SPICE; Verilog-A

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1. Introduction

Based on the Ovshinsky effect, which was proposed in the early 1970s, phase-change random access memory (PCRAM, PCM) has become one of the main research focuses in the micro-electronic field. Because of its merits of low-cost and high-performance, it is likely to replace current flash memory and become the first commercial non-volatile memory product^[1–4].

Traditionally, PCM is made on silicon substrate. Its key materials include the recordable phase film, heating electrode materials, insulation materials and lead electrode materials. Usually, a chalcogenide material is used as the recordable phase film, such as $\text{Ge}_2\text{Sb}_2\text{Te}_5$ (GST). The basic principle is to make the GST cell switch between an amorphous state (Reset) and a crystalline state (Set) with different electrical pulses. This is the Set/Reset operation. Then, by distinguishing the amorphous state (high resistance, $\sim 200 \text{ k}\Omega$) from the crystalline state (low resistance, $\sim 2 \text{ k}\Omega$)^[5], the information stored in the GST cell can be read easily. However, the I - V characteristics of PCM show an unwanted snapback behavior or Ovonic threshold switching (OTS) and the GST material remains amorphous during the whole process, even after switching. The phase transition does not happen unless the cell temperature reaches a crystalline temperature through an increase in bias current.

As we all know, a good model should be a real reflection of the physical properties. On the one hand, it should be closely combined with the component prototype. On the other hand, it should also be simple enough so that it can work well in the system-level applications. However, because of its various unknown characteristics, there is no universal SPICE model for GST still. Moreover, in most of the reported models, the GST

module, which should be of variable resistance according to temperature and other factors, is in fact always of fixed resistance^[5, 7–9]. This can not reflect the real-time characteristics of GST obviously. In this paper, a simplified SPICE model based on Verilog-A language is introduced. By handling it with physical models of heat distribution, thermoelectric theory and the JMAK crystallography equation, the model can well reproduce the physical behaviors of a PCM cell. Simulation results show that the proposed module has a similar I - V curve to the experimental data. Moreover, the real-time reproduced temperature and crystallinity curves can enable the operation process to be clearly understood.

2. Modeling with Verilog-A

Figure 1(a) shows the full structure of a PCM cell, in which the GST resistance can be taken into account as a changeable resistance. Briefly, this SPICE model is proposed to be the form as shown in Fig. 1(b), which contains three main parts: a heat distribution module (HDM), a crystallization module (CM) and a resistance change module (RCM). Firstly, the Joule heating law and thermal diffusion theory are included in the HDM so that it can output an effective temperature on time. Secondly, by coupling the effective temperature with the previous state, the JMAK equations based on the CM can compute the accurate crystallization rate of the GST cell. Thirdly, the RCM is utilized here to express the thermoelectric relationship between the resistivity and temperature of GST material. Naturally, the RCM can be separated into two conditions, one for the amorphous (RCA) and another for the crystalline (RCC). In addition, the parameters of bias voltage (or current) pulse width and amplitude are used here. The prototype theories and physical modules are described as follows.

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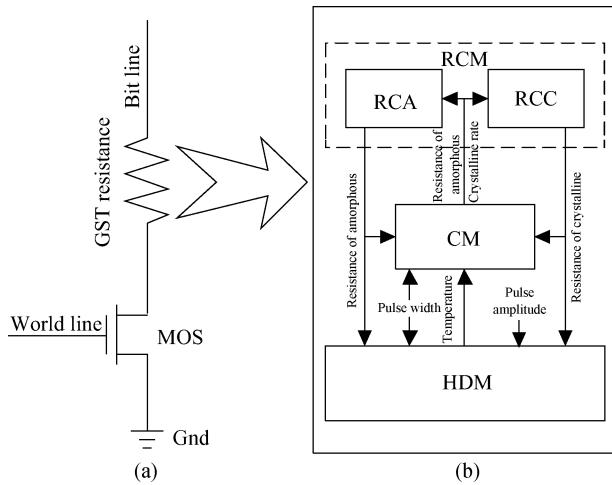


Fig. 1. (a) PCM memory cell structure. (b) Block diagram of the proposed SPICE model.

2.1. Heat distribution module

The heat distribution of a GST cell is always a complex problem. In simple terms, we can evaluate the cell temperature with Joule heating and heat dissipation as

$$T = \int (W_j - W_d) dt = \nabla T + 298 \text{ K}, \quad (1)$$

where W_j is the heating power of the PCM device and W_d is the thermal dispersion rate. They are given by

$$W_j = \frac{IU}{CV} = \frac{I^2R}{CV}, \quad (2)$$

$$W_d = \frac{dQ}{dt} = -\frac{1}{CV} \sum k \nabla T, \quad (3)$$

where C is the heat capacity, k is the thermal conductance, V is the heating volume, I and U are the current flow and voltage across a GST cell, respectively, and R is the resistance of the PCM cell during the programming process, which is a variable in addition to the temperature and the amorphous and crystalline rates.

Coupling with Eqs. (1)–(3), a homogeneous temperature distribution model is given by

$$\Delta T = \frac{l^2 I^2 R}{kV} \left[1 - \exp \left(-\frac{kt}{l^2 c} \right) \right], \quad (4)$$

where l is the thickness of the GST material and t is the programming time (or the width of the bias pulse). If considering the uneven distribution of the cell temperature^[10], an optimized model should be

$$T = \frac{l^2 IU}{kV} \left[1 - \gamma \exp \left(-\frac{kt}{l^2 c} \right) \right] + 298 \text{ K}, \quad (5)$$

where γ is a thermal efficiency factor.

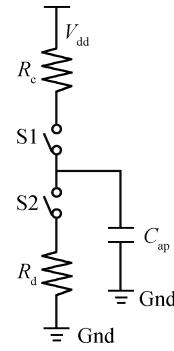


Fig. 2. A solution for the JMAK equation used in the proposed SPICE model.

2.2. JMAK equation and judgment module

When a SET pulse is biased on the PCM cell, its state will change from amorphous to crystalline, and this process follows the JMAK (Johnson–Mehl–Avrami–Kolmogorov) equations^[11]:

$$C_x = 1 - \exp [-(Kt)^n], \quad (6)$$

$$K = K_0 \exp \frac{-E_a}{K_B T}, \quad (7)$$

where K_0 is a frequency factor, E_a is the phase transition activation energy, n is the Avrami factor, K_B is the Boltzmann constant, T is the material temperature and C_x is the crystallinity (or crystalline rate).

Taking account of the fact that Equation (6) is similar to a first-order exponential function, an RC net is applied in this module, as shown in Fig. 2. C_{ap} is used to store the previous state by measuring its charge while S1 and S2 are used to charge or discharge the capacitor. R_c is a changeable resistor according to JMAK equation.

S1 and S2 are controlled by temperature. When the temperature is under T_c (glass transition point, $\sim 200^\circ\text{C}$), it has no affect on the GST status, both S1 and S2 are off, and therefore the capacitor remains at the previous state. When the temperature is between T_c and T_m (melting point, $\sim 600^\circ\text{C}$), the GST begins to crystallize, S1 is on and S2 remains off, and the capacitor becomes charged. When the temperature is over T_m , the GST becomes molten, S1 becomes off and S2 is on, and the capacitor is then discharged rapidly if the temperature suddenly falls to below T_c , both S1 and S2 become off, and the amorphous status can be saved until the next switching occurs.

2.3. Thermo-electric module

It is well known that the resistance of an amorphous semiconductor will change with temperature. The research results show that such performance is the inevitable result of trap-based transition to carriers. It is established that the electrical conductance of the amorphous material follows an expression by^[12]

$$\sigma = \sigma_{\Delta E} \exp(-\Delta E / K_B T) + \sigma_{\Delta E_1} \exp(-\Delta E_1 / K_B T) + \sigma_{\Delta E_2} \exp(-\Delta E_2 / K_B T) + \sigma_{T_0} \exp \left[-(T_0 / T)^{1/4} \right], \quad (8)$$

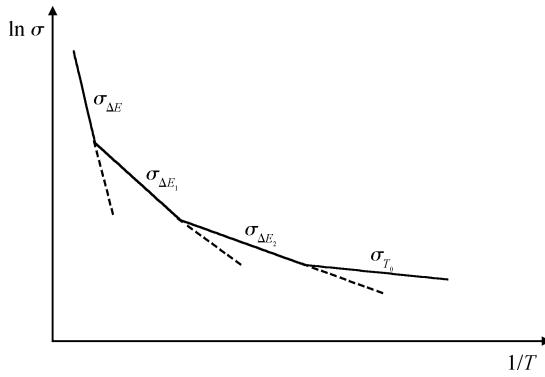


Fig. 3. Relationship between the conductivity and temperature of semiconductor materials^[12].

where the first item is extended-state electrical conductivity, the second item is band tail-state electrical conductivity, the third item is short-range hopping electrical conductivity and the last item is low-temperature localization-state variable-range hopping electrical conductivity. Figure 3 describes such relations of Eq. (8).

Without considering the specific mechanisms of the various effects on localization state conductivity, the band structure of amorphous GST can be simplified to two parts: the extended state and the localization state. Thus, the following expression can be obtained.

$$\sigma = \sigma_0 \exp(-\Delta E_0 / K_B T) + \sigma_1 \exp(-\Delta E_1 / K_B T). \quad (9)$$

Equation (9) is a sum of two components. The high activation energy component matches the OFF region and the low activation energy component represents the ON region where trap-assisted transition happens. σ_0 and σ_1 are normalizing coefficients. ΔE_0 and ΔE_1 are the activation energies for the deeper trap-based and shallower trap-based transitions.

Recently, experimental data (shown in Fig. 4) has indicated that the module in Eq. (9) should be improved. With an increase of bias-current, a sudden break would occur, which is the proposed OTS. Such behavior could be caused by the electric-field. Coupling Eqs. (8) and (9), the thermoelectric theory is tenable by

$$\sigma = [1 - f(E)] \sigma_0 \exp(-\Delta E_0 / K_B T) + f(E) \sigma_1 \exp(-\Delta E_1 / K_B T). \quad (10)$$

Equation (10) is the specific model of thermoelectric theory, where $f(E)$ is an Eth-related function, and Eth is the threshold electric-field determined by the GST material only.

Above is the simplified module for amorphous GST. Considering the differences between the two kinds of GST band structure, a similar item for crystalline GST material can lead to a unified GST module.

$$\sigma = [1 - f(C_x)] \{ [1 - f(E)] \sigma_0 \exp(-\Delta E_0 / K_B T) + f(E) \sigma_1 \exp(-\Delta E_1 / K_B T) \} + f(C_x) \sigma_2 \exp(-\Delta E_2 / K_B T), \quad (11)$$

where $f(C_x)$ is the crystallinity, which can be obtained from the JMAK equation. In addition, $\sigma_2 \exp(-\Delta E_2 / K_B T)$ is the electrical conductivity description for crystalline GST. Since

Table 1. Specific parameters of the model.

Parameter	Value	Parameter	Value
V	$4 \times 10^{-14} \text{ cm}^3$	l	120 nm
E_{a0}	0.6 eV	E_{a1}	0.05 eV
E_{a2}	0.01 eV	σ_0	4.47×10^{10}
σ_1	7×10^2	σ_2	6×10^2
T_c	200 °C	T_m	600 °C
k	4.63×10^{-3} (J·cm)/(K·S)	K_B	1.380×10^{-23} J/K
E_{th}	9.6×10^4 V/cm		

Table 2. Bias current pulses definition^[10].

Character parameter	Value
Reset current I_{reset}	$1200 \mu\text{A}$
Set current I_{set}	$600 \mu\text{A}$
Reset pulse width T_{reset}	20 ns
Set pulse width T_{set}	100 ns
Read current I_{read}	$10 \mu\text{A}$
Read pulse width T_{read}	20 ns
Rise time T_{rise}	1 ns
Fall time T_{fall}	1 ns
Delay time T_{delay}	0 ns

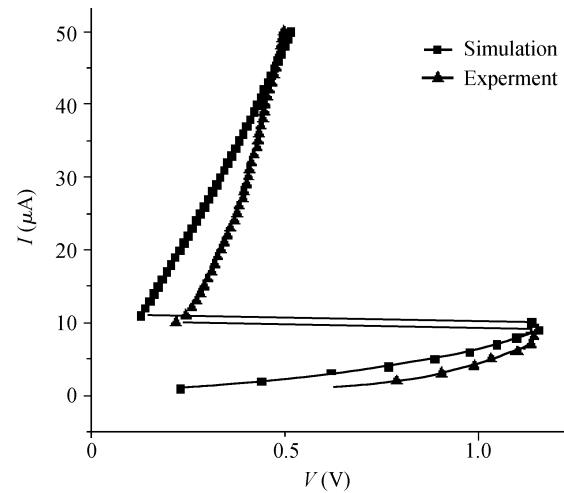


Fig. 4. Experimental data and model simulation results of I - V curves of amorphous GST.

the values of σ_0 , σ_1 , σ_2 and ΔE_0 , ΔE_1 , ΔE_2 are not reported elsewhere, their values can be obtained by fitting the experimental data.

3. Simulation and the results

A series of simulations using SPECTRE are executed. In the simulations, a programmable current resource is applied and the status of the cell can be observed over time by sensing the voltage in response.

In this model, all of the parameter values related to the material nature can be changed according to the physical prototype. Table 1 lists the parameters and their values that were used in this model for simulations. Table 2 lists the definition of the predetermined pulses for transient analysis.

Figure 4 is the direct current (DC) simulation result. We

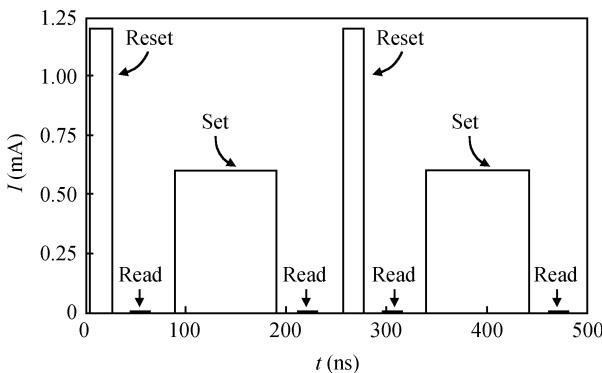


Fig. 5. The standard read/set/reset program current pulses for the PCM model.

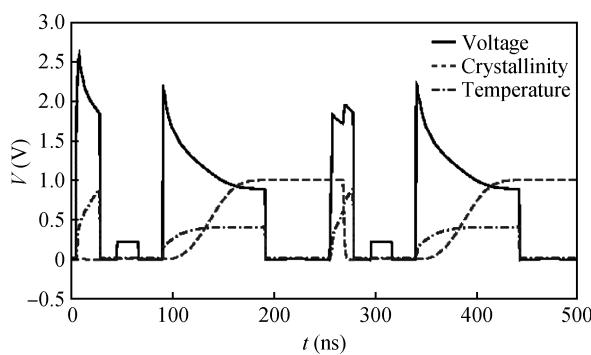


Fig. 6. Real-time results of the standard operations (including the cell voltage across curve, cell temperature curve and cell crystalline rate-curve. For temperature, 1 V in voltage implies for 1000 Kelvin in temperature, and for crystallinity, 1 V in voltage implies for 100 percent in crystallinity. In addition, the reason why the shape of the 2nd reset pulse is different from that of the 1st reset pulse is that they have different initial crystallinity, which can be seen in the figure as well, “0” for the 1st reset pulse while “1” for the 2nd reset pulse).

can easily find that the $I-V$ characteristic curve of the model is almost the same as that of the experiment profile. Figures 5 and 6 are the transient simulation results. Figure 5 is the predetermined pulses, and the dynamic characteristic curves in Fig. 6 reflect the real-time temperature and crystallinity of the memory cell during the programming process. The reset pulse causes the cell temperature to reach the melting point and then the crystallinity becomes “0”, correspondingly, the set pulse causes the cell temperature to reach the glass transition point and then the crystallinity becomes “1” according to the JMAK

law. In brief, they are analogous with the physical phenomena and consistent with the assumed conditions.

4. Conclusion

A simple yet reasonable solution for the SPICE model has been carried out in this paper by handling it with the optimized modules of heat distribution, threshold switching and crystallinity kinetics theory. The simulation results show that the simplified SPICE model can reproduce the GST behavior well. It is consistent with presupposed expectations and can facilitate PCM technology development not only at the device level, but also at the circuit level.

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