Design of ternary clocked adiabatic static random access memory*

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Abstract: Based on multi-valued logic, adiabatic circuits and the structure of ternary static random access memory (SRAM), a design scheme of a novel ternary clocked adiabatic SRAM is presented. The scheme adopts bootstrapped NMOS transistors, and an address decoder, a storage cell and a sense amplifier are charged and discharged in the adiabatic way, so the charges stored in the large switch capacitance of word lines, bit lines and the address decoder can be effectively restored to achieve energy recovery during reading and writing of ternary signals. The PSPICE simulation results indicate that the ternary clocked adiabatic SRAM has a correct logic function and low power consumption. Compared with ternary conventional SRAM, the average power consumption of the ternary adiabatic SRAM saves up to 68% in the same conditions.

Key words: multi-valued logic; adiabatic; ternary SRAM; circuit design
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1. Introduction

With the rapid development of CMOS technology, the density and operating speed of integrated circuit chips improve continuously. As a result, power dissipation has become increasing sharp. Power dissipation has become a bottleneck that hinders the development of integrated circuits, since it imposes restrictions on the design and performance of integrated circuit chips. As an important component in a system chip, due to large internal node capacitance and frequent data-accessing, static random access memory (SRAM) has enormous power dissipation. Thus reducing power consumption is one of the key issues in SRAM research. References [1–3], respectively, have proposed a new 8T SRAM cell, a 4T CMOS latch bit-cell and a 9T SRAM cell to reduce writing operation power consumption, reading/writing operation power consumption and bit-line leakage consumption, resulting in reducing the power consumption of the entire SRAM circuit. However, current research on low power SRAM mainly focuses on binary circuits[4, 5], which has not yet been developed for a multi-valued circuit. Multi-valued logic circuits can not only improve the single-line capacity of carried information and enhance the information density of integrated circuits, but also reduce the number of VLSI down-leads and pin-counts, and improve the circuit data-processing capacity[6−8]. Therefore, the study of low power SRAM has great significance.

With the characteristics of energy recovery, adiabatic technology breaks through the limitations of energy transmission mode in traditional CMOS circuits; an AC power supply is used to drive the circuits, and the transmission of energy is made to follow the way of power → capacitance → power, so the charges on the node capacitances can be recycled effectively to achieve energy recovery, and the adiabatic circuits have very low power consumption[9, 10]. Therefore, represented by a ternary circuit with the smallest radix, following the guidance of the theory of three essential circuit elements[11], this paper applies adiabatic technology to the design of ternary SRAM and proposes a novel ternary clocked adiabatic SRAM based on a double power clock ternary clocked transmission gate adiabatic logic (DTCTGAL) circuit[12]. The row/column address decoder, storage cell and sense amplifier of the SRAM are all realized with adiabatic circuits. The PSPICE simulation results verify the correct logic function and obvious low power consumption of the designed circuits.

2. Design of ternary AND gate, multiplexer based on DTCTGAL

The AND gate and multiplexer are basic functional units in complex digital circuits, widely used in electronic devices in industry, agriculture, health care, life sciences, national defense and other areas. Most conventional ternary AND gates and multiplexers are constructed from binary components. Binary signals have a large space requirement and low time utilization, which makes the circuits rather complex, and the area and power dissipation large. In order to reduce power consumption and chip area, a ternary two-input AND gate, a ternary 9 to 1 multiplexer and a ternary three-input AND gate are proposed with the theory of three essential circuit elements[11]and the design idea of DTCTGAL circuit[12], as shown in Fig. 1.

The circuits in Fig. 1 adopt two-phase non-overlapping power clocks. The specific operation is divided into two steps. The first step samples each input signal with NMOS transistors controlled by the clock $\overline{\phi}$, and makes the phase of input signals equivalent to $\overline{\phi}$. If data selection signals are given in the first step, the input signals can be further controlled whether or not they are sampled. Under the work rhythm of power clocks ϕ_1 and ϕ, the second step uses the input sampled values and cross-storage structure to discharge the output loads and recover the charge on the output loads. Where ϕ_1 and ϕ have

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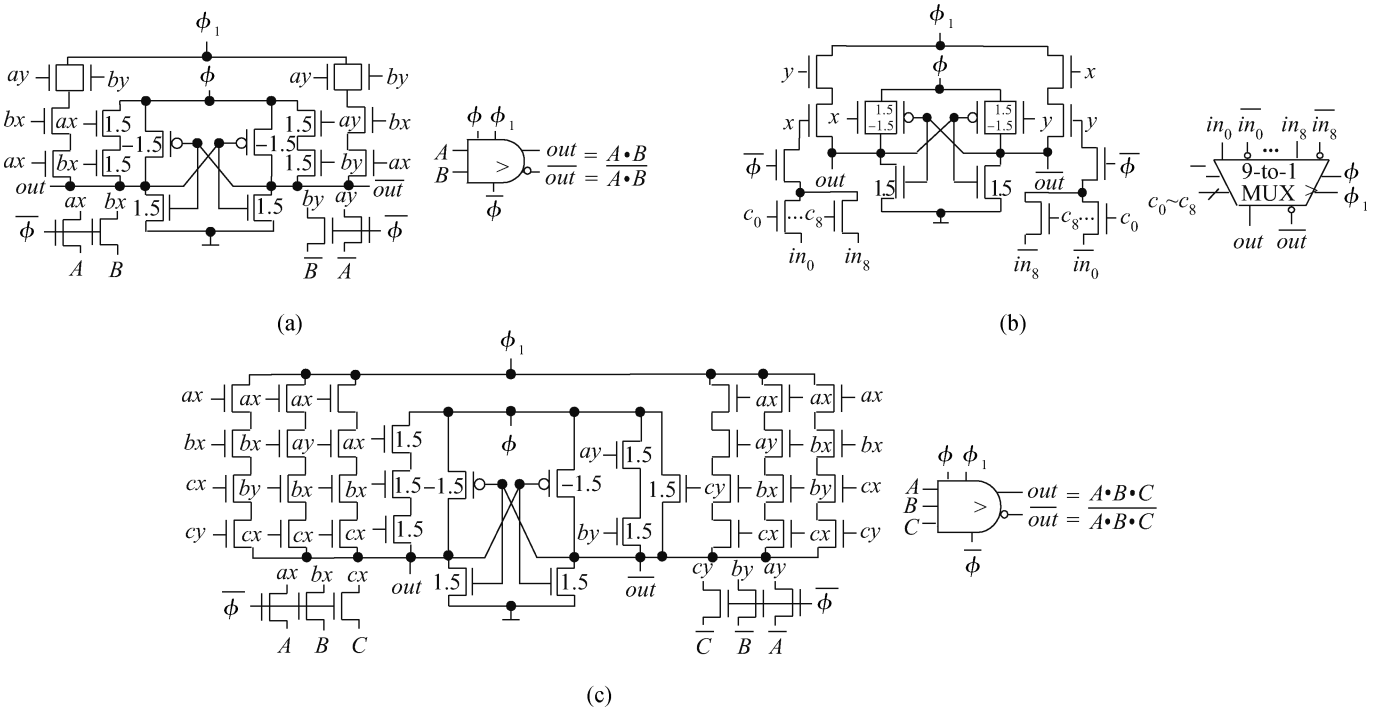


Fig. 1. DTCTGAL circuits. (a) Two-input AND gate. (b) 9 to 1 multiplexer. (c) Three-input AND gate.

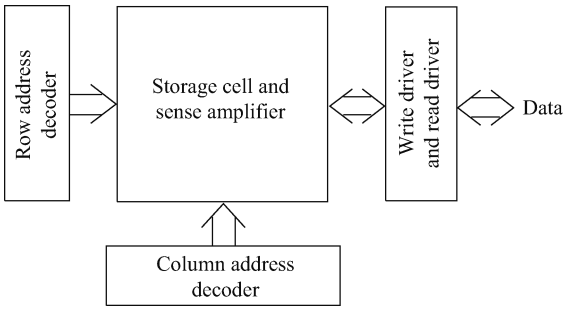


Fig. 2. Block diagram of ternary adiabatic SRAM.

the same phase but different amplitudes, the amplitude values of ϕ_1 and ϕ are $V_{DD}/2$ and V_{DD}, which correspond to logic 1 and logic 2, respectively, and their phase difference with $\overline{\phi}$ is 180° (the output phase is the same as ϕ_1 and ϕ). For the part nodes of similar circuits may appear floating, the above circuits use complementary output signals to eliminate, thus avoiding the uncertainty of the output signals.

3. Design of ternary adiabatic SRAM

By studying the structure and principle of conventional SRAM, taking 81 × 81 bits, for example, a ternary adiabatic SRAM is designed based on a DTCTGAL circuit. This consists of a row/column address decoder, a storage cell, a sense amplifier, a write driver and a read driver, as shown in Fig. 2. All the circuits are designed based on a DTCTGAL circuit, which can effectively recover the charges stored in the large switch capacitance of word lines, bit lines, a row/column address decoder and a sense amplifier, thereby the power consumption is reduced. The employment of the selection signals, which can cut off the power circuits of the storage cell and sense amplifier in inactivated subarrays, decreases unnecessary energy consumption, further reducing the power consumption of the SRAM circuit.

3.1. Row/column address decoder

The row/column address decoder is shown in Fig. 3. The ternary adiabatic SRAM based on a DTCTGAL circuit consists of 81 rows, each row with 9 subarrays, and each subarray with 9 storage cells, where the $A_3A_2A_1A_0$ indicates the row address and A_5A_4 indicates the column address. The row address decoder produces row selection signals through second-order decoding mode to activate a global word line GWL_i (i = 0–80), while the column address decoder produces a subarray selection signal c_j (j = 0–8) to select the corresponding subarray. A pair of corresponding read word line $RWL_{i,j}$ and write word line $WWL_{i,j}$ (i = 0–80, j = 0–8) is activated by a global word line, read/write enable signal and a subarray selection signal after a certain delay, and only the subarray connected to the activated read/write word line can read and write data in a single clock cycle. The storage cell cannot be read and written at the same time, thus in timing, a read-after-write operation style is employed, in which the write word line is activated followed by the activation of the read word line in a single clock cycle. Therefore, the read enable signal RE has one more buffer delay than the write enable signal WE in read/write word line generation.

3.2. Write/read driver

The ternary adiabatic SRAM has 9 subarrays per row, read/write bit lines of storage cells in the same column are connected together, and data are written into the write bit lines of the corresponding subarray with the write driver. The structure

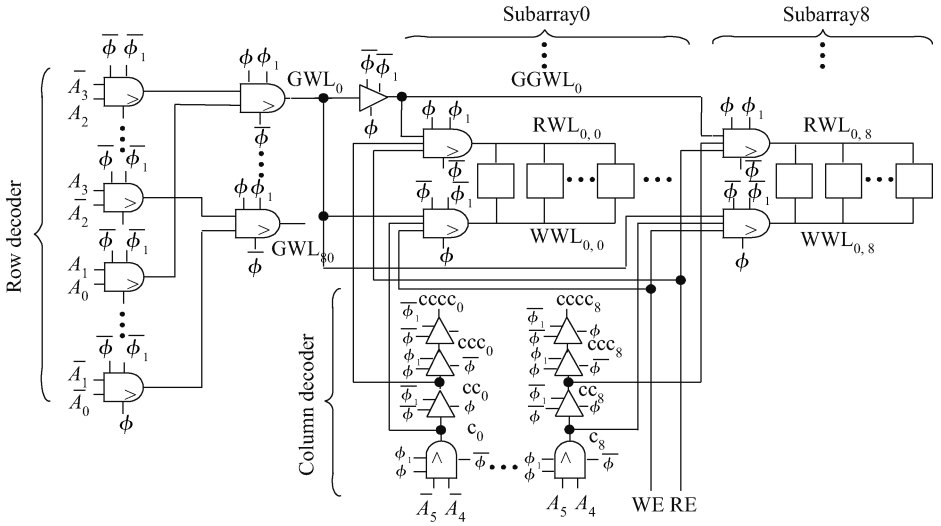
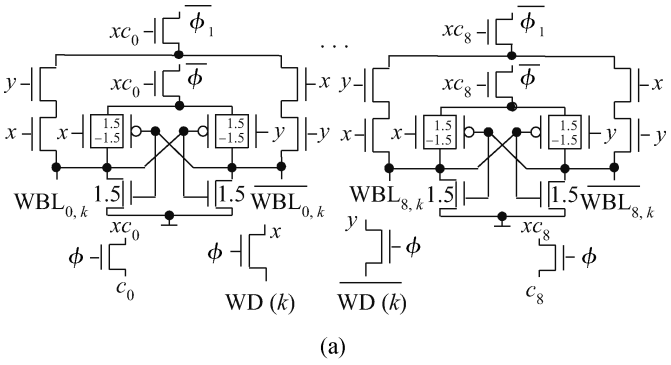


Fig. 3. Row/column address decoder.



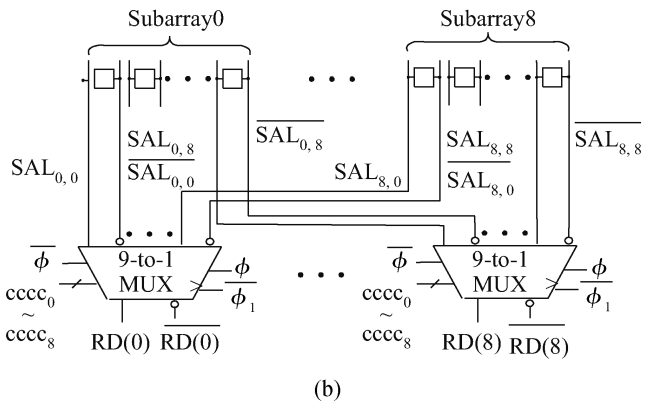
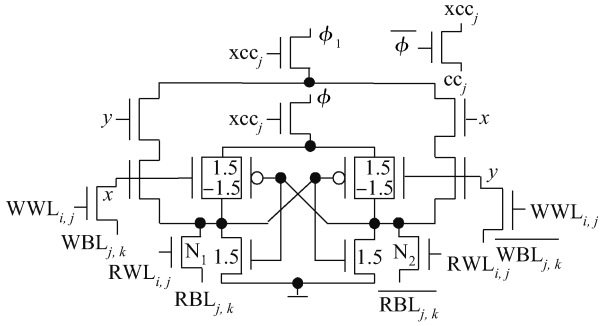


Fig. 4. (a) Write driver. (b) Read driver.



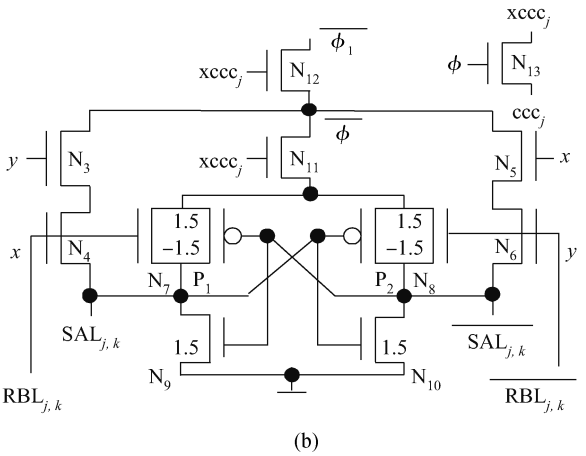


Fig. 5. (a) Storage cell. (b) Sense amplifier.

of the one-bit data write driver is shown in Fig. 4(a), and the write bit lines are charged and discharged in the adiabatic way, which is similar to a DTCTGAL circuit. The difference is that the write driver controls the power clocks $\overline{\phi}_1$ and $\overline{\phi}$ to turn on or turn off according to the sampled value xc_j (j = 0–8) of the subarray selection signal c_j (j = 0–8), thus avoiding the write bit lines of inactivated subarrays to be charged and discharged unnecessarily, so as to reduce the power consumption of the write driver. However, each subarray of ternary adiabatic SRAM has 9 storage cells, hence 9 bits of data WD(k) (k = 0–8) are needed to write once, so 9 write drivers are required. In a single clock cycle, only the write bit lines of the activated subarray will have data to write in, and the rest are clamped to zero voltage.

The read driver adopts a 9 to 1 multiplexer in Fig. 1(b), as shown in Fig. 4(b), and takes the output signals $\mathrm{SAL}_{j,k}$ (j = 0–8, k = 0–8) of sense amplifiers in all the subarrays as input signals, the signals cccc_j (j = 0–8) obtained after three buffer delay of subarray selection signals c_j (j = 0–8) as data selection signals. The 9 to 1 multiplexer samples the signals on $\mathrm{SAL}_{j,k}$ of the activated subarrays, then reads the data to the outputs RD(k) (k = 0–8), thus the selection of the data in the activated subarrays is realized.

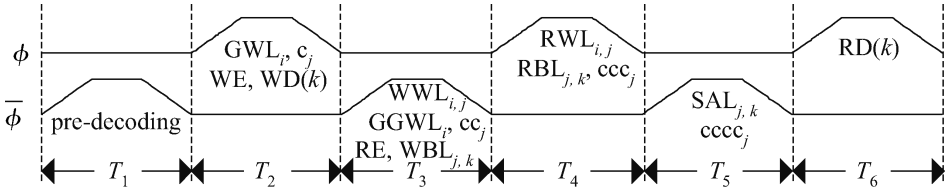


Fig. 6. Operation timing of ternary adiabatic SRAM.

3.3. Storage cell and sense amplifier

The storage cell of the ternary adiabatic SRAM is designed based on the DTCTGAL circuit, as shown in Fig. 5(a). The sampled values xcc$_j$ (j = 0–8) of the signals cc$_j$ (j = 0–8) after one buffer delay of subarray selection signals c_j (j = 0–8) control the power clocks ϕ_1 and ϕ to turn on or turn off, thus unnecessary energy consumption of storage cells is reduced in the inactivated subarrays. During the period of write operation, the write driver is clocked by the signals on the write word lines WWL$_{i,j}$ (i = 0–80, j = 0–8), and the data on the write bit lines WBL$_{j,k}$ (j = 0–8, k = 0–8) are sampled; the sampled values and cross-storage structure are utilized to write data into the storage cells of activated subarrays. During the period of read operation, the read word lines RWL$_{i,j}$ (i = 0–80, j = 0–8) activate the transistors N_1 and N_2, then the data in the storage cells are read to read bit lines RBL$_{j,k}$ (j = 0–8, k = 0–8). The storage arrays of ternary adiabatic SRAM consist of storage cells arranged in a horizontal or vertical way; the storage cells in the same subarray share a pair of read/write word line, while the storage cells in the same column share a pair of read/write bit lines.

The sense amplifier in Fig. 5(b) separates the output signals SAL$_{j,k}$ from read bit line RBL$_{j,k}$ (j = 0–8, k = 0–8), which is different from the one in the conventional SRAM. The signals ccc$_j$ (j = 0–8), i.e., subarray selection signals c_j (j = 0–8) after a two buffer delay, is sampled, and the sampled values xcccc$_j$ (j = 0–8) is used to control the power clocks $\overline{\phi}_1$ and $\overline{\phi}$ to turn on or turn off. Taking the read word line RWL$_{i,j}$ as the clocked signal, the transistors N_1 , N_2 in the storage cell and N_3, N_4, N_5, N_6, N_7, N_8, N_9, N_{10}, P_1 , P_2 in the sense amplifier constitute the DTCTGAL circuit. The data in the storage cells of activated subarrays are amplified in an adiabatic way, hence level jumping on SAL$_{j,k}$ of inactivated subarrays is reduced, thus the power consumption is reduced.

3.4. Operation timing of ternary adiabatic SRAM

The operation timing of ternary adiabatic SRAM is shown in Fig. 6. During period T_1, the row address decoder carries out first-order pre-decoding. During period T_2, the row address decoder carries out second-order decoding, and activates a global word line GWL$_i$ to select the corresponding row; the column address decoder produces a subarray selection signal c_j to select the corresponding subarray, meanwhile the write enable signal WE and the data WD(k) are obtained. During period T_3, the global word line GWL$_i$, subarray selection signal c_j and write enable signal WE activate a write word line WWL$_{i,j}$, so the data are written into storage cells in the activated subarrays by the write bit line WBL$_{j,k}$; a read enable signal RE is obtained, the signals GGWL$_i$ and cc$_j$, which are signals of global word line GWL$_i$ and subarray selection signal c_j after one buffer delay, respectively, are gained. During period T_4, GGWL$_i$, cc$_j$ and a read enable signal RE activate a read word line RWL$_{i,j}$, the data in the storage cells of activated subarrays are read to RBL$_{j,k}$, and the signal ccc$_j$ after two buffer delay of the subarray selection signal c_j is gained. During period T_5, the data on the read bit line RBL$_{j,k}$ are amplified to the output line SAL$_{j,k}$, and the signal cccc$_j$ after three buffer delay of the subarray selection signal c_j is obtained. During period T_6, the data RD(k) of activated subarrays are gained through selecting SAL$_{j,k}$ of each subarray with a 9 to 1 multiplexer.

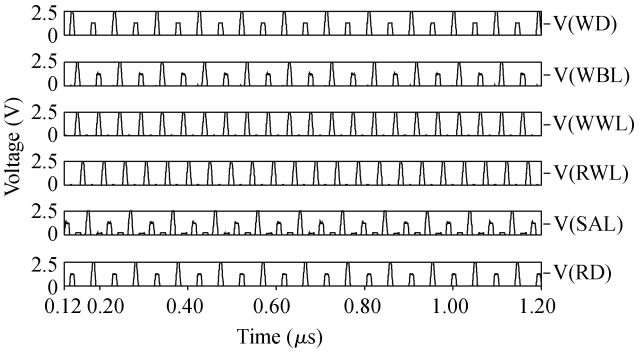


Fig. 7. Simulation waveforms of ternary adiabatic SRAM.

4. Computer simulation and conclusion

Using the parameters of the TSMC 0.25 μm CMOS device, the clock frequency is 41.7 MHz, one subarray of ternary adiabatic SRAM based on the DTCTGAL circuit designed above is simulated, and the output load capacitance is 10 fF. Where the amplitude voltages of the power clocks ϕ_1, $\overline{\phi}_1$ and ϕ, $\bar{\phi}$ correspond to 1.25 V and 2.5 V, and the device sizes of the NMOS and PMOS transistors are taken with W/L = 0.36 μm/0.24 μm and W/L = 0.72 μm/0.24 μm, respectively. Figure 7 shows the simulation waveforms of ternary adiabatic SRAM, where the data WD is "2121…". The read data RD are two more clock cycles delay than the write data WD, which satisfies the operation timing of ternary adiabatic SRAM. The simulation results indicate that the circuits designed have correct logic function and ideal output waveforms.

Under the same conditions, the transient energy consumption comparison between ternary adiabatic SRAM and ternary conventional SRAM is shown in Fig. 8. The ascending parts in the curves of the ternary adiabatic SRAM indicate that the power clocks charge the circuit, while the descending parts denote that the power clocks recover energy from the circuit; the gradual rise of concave bottoms in the curves shows the energy

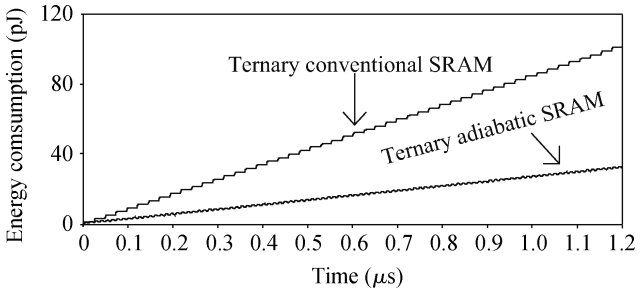


Fig. 8. Transient energy consumption comparison between ternary adiabatic SRAM and conventional SRAM.

consumption of the circuit. In 1.2 μs, the energy consumption of ternary conventional SRAM is 100.923 pJ, while the energy consumption of ternary adiabatic SRAM is 32.315 pJ, consequently energy consumption saves up to 68%, which shows that the designed circuit has the significant characteristic of low power consumption.

According to the theory of three essential circuit elements, this paper has introduced adiabatic technology into the design of ternary SRAM, two-phase non-overlapping power clocks and NMOS transistors with different thresholds are further adopted to achieve the design of ternary adiabatic SRAM based on a DTCTGAL circuit. By using the bootstrapped NMOS transistors and the CMOS-latch structure, the circuit ensures that the output always follows the power clocks ϕ_1 and ϕ to change, eliminating the non-adiabatic energy consumption caused by threshold voltage loss, thus effectively reducing the power consumption. The method utilized in the design can be further applied to design a higher-radix multi-valued adiabatic storage cell, so as to promote the development of multi-valued logic circuits.

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