Investigation and modeling of the avalanche effect in MOSFETs with non-uniform finger spacing*

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Abstract: This paper investigates the effect of a non-uniform gate-finger spacing layout structure on the avalanche breakdown performance of RF CMOS technology. Compared with a standard multi-finger device with uniform gate-finger spacing, a device with non-uniform gate-finger spacing represents an improvement of 8.5% for the drain–source breakdown voltage (BV_{ds}) and of 20% for the thermally-related drain conductance. A novel compact model is proposed to accurately predict the variation of BV_{ds} with the total area of devices, which is dependent on the different finger spacing sizes. The model is verified and validated by the excellent match between the measured and simulated avalanche breakdown characteristics for a set of uniform and non-uniform gate-finger spacing arranged nMOSFETs.

Key words: non-uniform; gate-finger spacing; avalanche breakdown; RF CMOS
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1. Introduction

There has been an increasing interest in designing RF power amplifiers (PAs) in CMOS technology, such as the 0.25-μm[1], 0.18-μm[2], 0.13-μm[3], 90-nm[4] and 65-nm[5] standard RF CMOS processes. Given that there is no restriction on the choice of drain bias, the breakdown characteristics of MOSFETs operated at high drain potentials determine the onset of gain compression and the maximum achievable output power. Using a MOSFET at best efficiency and full power often requires operation at the limit set by breakdown mechanisms[6]. Thus, novel layout structures which can improve the breakdown limit of MOSFETs without reducing the RF performance of devices are of utmost importance in RF PA design based on standard CMOS processes.

As an advanced layout method, the non-uniform finger spacing layout is traditionally claimed as an effective layout method to provide a uniform junction temperature across the fingers, thus significantly enhancing the power performance of power transistors such as the SiGe HBTs[7] and III–V FETs[8]. In this work, we propose that this kind of layout structure can also be used to effectively improve the breakdown limit of MOSFETs. In this paper, characteristics of a non-uniform finger spaced layout structure, which has a variable pitch between the gate-fingers that decreases uniformly from the central portion of a multi-finger nMOSFET to two opposite outer end portions, similar to Ref. [8], is investigated in 0.18-μm RF CMOS. In contrast to Refs. [7, 8], we specifically focus on the impact of the changing of the spacing size (corresponding to the increasing of the area of the device) on the corresponding drain–source breakdown voltage (BV_{ds}) and parasitic capacitances. For the first time, a novel compact model for accurately predicting the characteristics of the avalanche breakdown current of the devices with different gate-finger spacing is proposed. The measured BV_{ds} characteristics and the extracted equivalent circuit model parameters indicate that the employed layout approach can effectively improve the avalanche break-down effects, and only slightly reduce the cutoff frequency f_T and maximum oscillation frequency f_{max}, leading to an improvement in the design of high performance CMOS PAs.

2. Experimental setup, results and discussion

A simplified layout plane figure and the gate-finger spacing arrangement method of the investigated devices in this work are given in Fig. 1. Four 65-finger n-MOSFETs with $L_f = 0.18$ μm and $W_f = 7.5$ μm, named devices B, C, D and E, which have step varied pitches with 0.01, 0.02, 0.03 and 0.04 μm between the adjacent gate-fingers and with $S_M = 0.6, 0.92$, 1.24 and 1.56 μm were fabricated using the SMIC 0.18 μm 1P6M RF-CMOS process, respectively. For comparison, a uniformly spaced 65-finger nMOSFET with the same L_f and W_f, named device A, was also fabricated. The gate-finger spacing sizes between the two out end fingers of devices B, C, D and E are set equal to the spacing size used in device A, 0.28 μm.

The DC characteristics of the transistors are measured with the Agilent 4156C precision semiconductor parameter analyzer. Two RF measurement systems, the Agilent E5071C and the E8364B network analyzer are used to characterize the RF behaviour of transistors from 100 kHz to 1 GHz and 1 to 50 GHz, respectively. Parasitics introduced by GSG PAD are de-embedded by using the open-short de-embedding technique[9]. The breakdown voltage, BV_{ds}, is taken as the value of V_{ds} when dI_{ds}/dV_{ds} equal to $0.05(N_f W_f/L_f)$, as illustrated in Fig. 2. In this work, the BV_{ds} at $V_{gs} = 1.8$ V of the five devices are taken for comparison. For quantitative analysis, small-signal parameters C_{gs}, C_{gd} and R_g are extracted based on the following equations[10, 11]:

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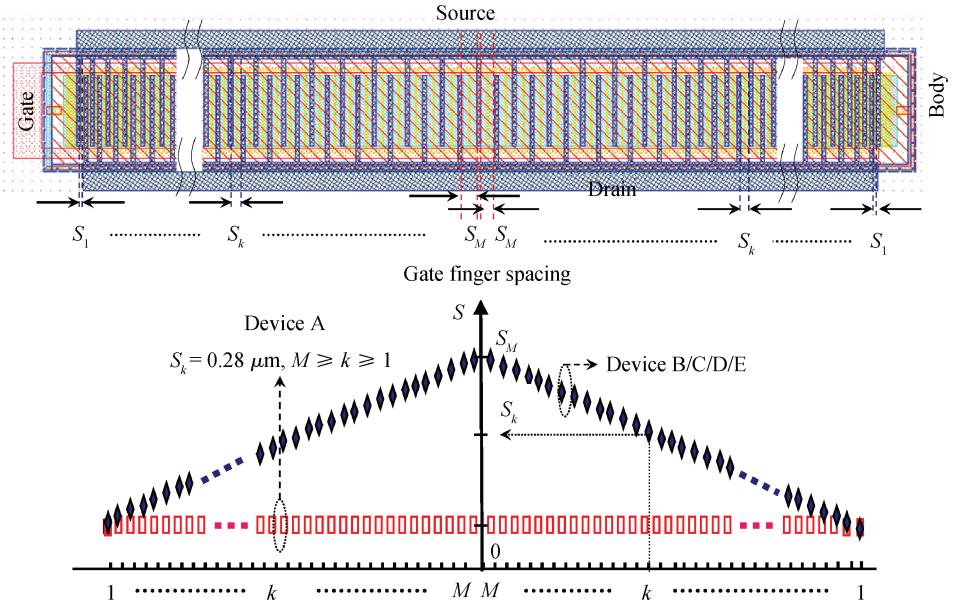

Fig. 1. Simplified layout plane figure (up) and the gate-finger spacing sizes arrangement method (down) of the investigated layout structures of nMOSFETs with an odd number of gate-fingers. The layout is arranged as a symmetric structure. When the number of gate-finger (N_f) is odd, $M = (N_f - 1)/2$, while $M = N_f/2 + 1$ for N_f is even. S_k ($M \geqslant k \geqslant 1$) represents the k^{st} gate-finger spacing size. Device A is a uniformly gate-finger spacing arranged transistor and the spacing size is 0.28 μm. Device B, C, D and E are non-uniformly gate-finger spacing arranged transistors, S_M represents the central portion spacing, 0.6, 0.92, 1.24 and 1.56 μm are used for the four devices, respectively.

Table 1. Description of nMOSFETs with different gate-finger spacing arrangements including extracted gate resistance, parasitic capacitances, DC current, transconductance, iso-thermal drain conductance and RF performance at $V_{DS} = V_{GS} = 1.8$ V. Δg_{ds} is calculated as $\Delta g_{ds} = g_{dsT} - g_{ds}$.

Parameter	Device A	Device B	Device C	Device D	Device E
$R_g(\Omega)$	1.20	1.18	1.24	1.19	1.21
C_{gs} (fF)	332.5	339.1	342.2	345.2	350.8
C_{gd} (fF)	134.1	134.4	135.4	136.2	137.2
C_{total} (fF)	476.6	473.5	477.6	481.4	488.0
I_{ds} (mA)	117.3	114.8	114.9	113.9	112.3
g_m (mS)	143.4	142.7	143.8	144.1	143.1
g_{ds} (mS)	8.3	8.32	8.5	8.35	8.48
g_{dsT} (mS)	16.74	16.48	15.84	15.54	15.24
Δg_{ds} (mS)	8.44	8.16	7.34	7.19	6.76
f_T (GHz)	48.9	47.96	47.92	47.64	46.67
f_{max} (GHz)	100.3	99.91	96.93	98.52	96.12

$$C_{gs} = [\mathrm{Im}(Y_{11} + Y_{12})]/\omega, \tag{1}$$

$$C_{gd} = [-\mathrm{Im}(Y_{12})]/\omega, \tag{2}$$

$$R_g = \mathrm{Re}(Y_{11})/\left[\mathrm{Im}(Y_{11})\right]^2. \tag{3}$$

The g_{dsT} listed in Table 1 represents the iso-thermal drain conductance, which is extracted by using the frequency dependent characterization of the drain conductance[12].

The values of C_{gs}, C_{gd} and R_g listed in Table 1 were extracted from S-parameters and averaged in the range of 2–15 GHz, and C_{total} equals $C_{gs} + C_{gd}$. The f_T and f_{max} of the five devices are estimated from the equivalent circuit model parameters as follows (simplified from Ref. [13]):

$$f_T = g_m/2\pi C_{total}, \tag{4}$$

$$f_{max} = f_T/2\sqrt{R_g\left(g_{ds} + 2\pi f_T C_{gd}\right)}. \tag{5}$$

The measured BV_{ds} characteristics of the five devices and the extracted equivalent circuit parameters are given in Fig. 3 and Table 1, respectively. Although the drain current I_{ds} in device E is reduced by $\sim 4\%$ compared with that in device A, g_m and R_g of devices B, C, D and E keep close to those of device A. Compared with that in device A, C_{total} is slightly increased by $\sim 2.4\%$ for device E, and there is only a small reduction of 2.23 GHz and 4.18 GHz in f_T and f_{max} of Device E as seen from Table 1, respectively. Two points worth mentioning are that the BV_{ds} in Device E is improved by $\sim 8\%$ compared with that in device A, from 2.95 to 3.2 V, and the thermally related drain conductance doublet (i.e. Δg_{ds} listed in Table 1) is improved by $\sim 20\%$ for device E, compared with that in device A. As can be seen from Fig. 3, BV_{ds} of the four transistors with non-uniform finger spacing arrangement are higher than that of the

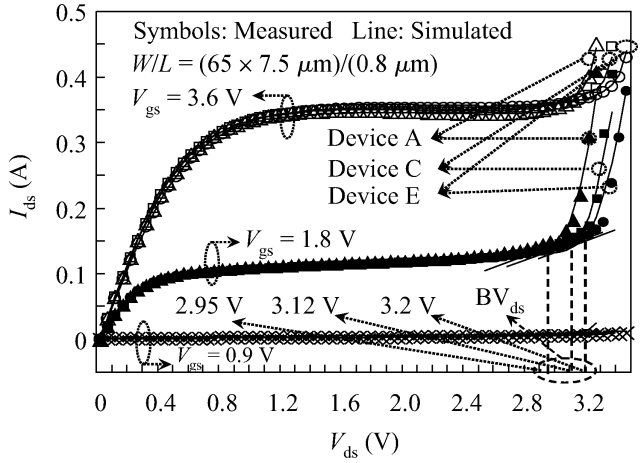

Fig. 2. Comparison of simulated I_{ds}–V_{ds} characteristics including the breakdown region with and measured results for the devices A, C and E. BV_{ds} is taken be the value of V_{ds} when dI_{ds}/dV_{ds} equal to $0.05(N_f W_f/L_f)$.

device A. This should be a joint result of the improved thermal characteristics and the change in g_{ds} of transistors with the increasing of S_M, i.e. the increased layout area of devices.

3. Scalable drain current modeling

The drain current model considering the breakdown effect proposed here is defined as

$$I_{ds} = \frac{I_{dse}}{1 + m_1 P_{diss}} \left(1 + b_1 \exp \frac{V_{gd}}{b_2 V_{tv}} + \frac{V_{gd}^2}{b_3 V_{tv}^2} \exp \frac{V_{ds}}{b_4 V_{tv}}\right), \tag{6}$$

where V_{tv} is the thermal voltage, I_{dse} represents the drain current without avalanche breakdown effect, m_1 is introduced to consider the thermal-related power dissipation effect of transistors, while b_1, b_2, b_3 and b_4 are experimentally introduced to consider the influence of the layout area change caused by the finger spacing sizes changing. The power dissipation, P_{diss}, is defined as

$$P_{diss} = I_{dse} V_{ds}. \tag{7}$$

For scalable modeling[14], the five parameters, m_1, b_1, b_2, b_3 and b_4 are dependent on the nominal active area of transistor (A_{nor}). For a layout structure with an odd number of gate-fingers depicted in Fig. 1, A_{nor} can be calculated as

$$A_{nor} = A_0 W_f \left(L_f N_f + 2 \sum_{k=1}^{M} S_k\right), \tag{8}$$

$$S_k = \frac{k-1}{M-1} (S_M - S_1) + S_1, \quad M \geqslant k \geqslant 1, \tag{9}$$

where A_0 is 1.0×10^{12}, which is used as the nominal active area of transistor. The functions used for the scalable m_1, b_1, b_2, b_3 and b_4 with regard to A_{nor} are defined as

$$m_1 = (M_{10} + M_{11} A_{nor})^{-1}, \tag{10}$$

$$b_1 = B_{10} e^{B_{11} A_{nor}}, \tag{11}$$

Table 2. Values of the model parameter extracted from five devices with different gage-finger spacing arrangements.

Parameter	Value
M_{10}	5.04
M_{11}	1.344×10^{-2}
B_{10}	1.63×10^{-35}
B_{11}	9.178×10^{-3}
B_{20}	−6.83
B_{21}	4.52×10^{-2}
B_{30}	−488
B_{31}	3.795
B_{40}	1.964
B_{41}	5.075×10^{-2}

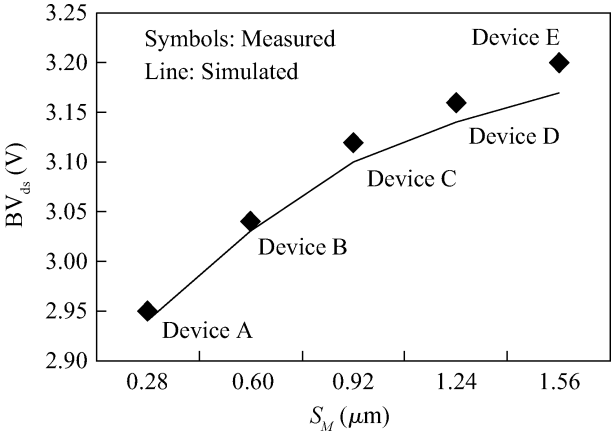

Fig. 3. Comparison of the measured and scalable model BV_{ds} characteristics of the five devices at $V_{gs} = 1.8$ V. BV_{ds} of transistors is increased with the increasing of S_M.

$$b_2 = B_{20}^{-1} + (B_{21} A_{nor})^{-1}, \tag{12}$$

$$b_3 = B_{30}^{-1} + (B_{31} A_{nor})^{-1}, \tag{13}$$

$$b_4 = B_{40}^{-1} + (B_{41} A_{nor})^{-1}, \tag{14}$$

where M_{10}, M_{11}, B_{10}, B_{11}, B_{20}, B_{21}, B_{30}, B_{31}, B_{40} and B_{41} are model parameters.

To verify the validity of the proposed model, the Verilog-A based PSP102.3 model is modified using Eq. (8) and implemented in an Agilent advanced design system (ADS) for simulation. The model parameters for the five transistors are directly extracted by using a simple optimization procedure. The extracted parameters are listed in Table 2 in ADS directly. Figure 2 depicts an excellent agreement between the measured and simulated drain current avalanche breakdown characteristics of devices A, C and E, at $V_{gs} = 0.9$, 1.8 and 3.6 V, respectively. An excellent agreement between the extracted and simulated BV_{ds} characteristics of all the five devices is achieved and illustrated in Fig. 3.

4. Conclusion

In this paper, the performance of RF MOSFETs with a non-uniform gate-finger spacing arrangement has been inves-

tigated. The employed non-uniform gate-finger spacing layout method demonstrated the enhanced breakdown voltage of transistors. A novel active area dependent avalanche breakdown model has been presented. The accuracy of the proposed scalable model is validated through the excellent agreement between the predicted and measured avalanche breakdown current and the breakdown voltage of uniformly and non-uniformly gate-finger spacing arranged RF MOSFETs.

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