

Analytical modeling of drain current and RF performance for double-gate fully depleted nanoscale SOI MOSFETs

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Abstract: A new 2D analytical drain current model is presented for symmetric double-gate fully depleted nanoscale SOI MOSFETs. Investigation of device parameters like transconductance for double-gate fully depleted nanoscale SOI MOSFETs is also carried out. Finally this work is concluded by modeling the cut-off frequency, which is one of the main figures of merit for analog/RF performance for double-gate fully depleted nanoscale SOI MOSFETs. The results of the modeling are compared with those obtained by a 2D ATLAS device simulator to verify the accuracy of the proposed model.

Key words: double-gate; fully depleted; silicon-on-insulator; Poisson's equation; radio frequency; ATLAS

DOI: 10.1088/1674-4926/33/2/024001

EEACC: 2570

1. Introduction

A double-gate silicon-on-insulator MOSFET has been studied extensively in recent years and is projected as the device for future processors. Among the different configurations of double-gate MOSFETs, the device physics of symmetric double-gate MOSFETs has been well studied and many compact models have been developed^[1-11]. A rigorous channel potential based drain current model for asymmetric double-gate MOSFETs has been developed by Taur's group by using direct integration, with the symmetric operation included as a special case^[12].

Recently, we have developed a potential and threshold voltage model for a double-gate fully depleted nanoscale SOI MOSFET based on the solution of Poisson's equation using Green's function solution technique^[13]. In this paper, it is extended to model drain current, transconductance and cut-off frequency.

Drain current and transconductance dependence on parameters such as channel length, channel doping, channel thickness, gate oxide thickness and gate to source voltage is discussed. Cut-off frequency dependence on gate oxide thickness, channel doping, gate-to-source voltage and drain-to-source voltage is also discussed. Accuracy of the model is verified by comparing the model results with simulations using a 2D ATLAS device simulator^[14]. A close match with published results confirms the validity of the model.

2. Analytical model for drain current

The basic structure of a fully depleted double-gate nanoscale SOI MOSFET is shown in Fig. 1.

Neglecting the fixed oxide charge effect, for a strongly inverted n-type double-gate fully depleted nanoscale SOI MOSFET, the current^[15] in the channel is given by

$$I_{DS} = W\mu_n(x)Q_n(x)\frac{d\phi_c(x)}{dx}, \quad (1)$$

where I_{DS} is current in the channel, $0 \leq x \leq L$, W is the channel width, $\mu_n(x)$ is the mobility of electrons given as

$$\mu_n(x) = \frac{\mu_{no}}{\left[1 + \left(\frac{E(x)}{E_c}\right)^2\right]^{1/2}}, \quad (2)$$

where μ_{no} is low field mobility^[16], $E(x)$ is the longitudinal field given by

$$E(x) = \frac{C_{ox} [V_{fb,f} - V_{gs} + \phi_c(x)]}{\epsilon_{si}}, \quad (3)$$

and E_c is the critical field given by

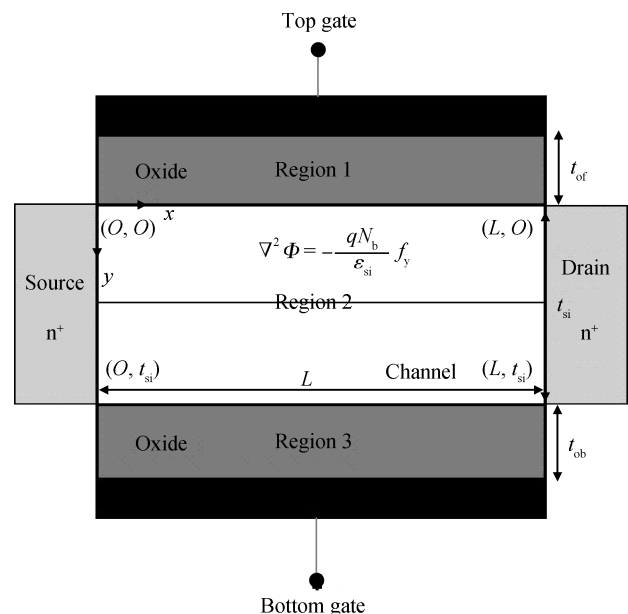


Fig. 1. Schematic diagram of a double-gate fully depleted nanoscale SOI MOSFET.

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Received 6 August 2011, revised manuscript received 25 September 2011

$$E_C = 6.01 \times 10^2 T^{3/2}. \quad (4)$$

$V'_{gs} = V_{gs} - V_{fb,f}$. V_{gs} is gate-to-source voltage, $V_{fb,f}$ is flat band voltage of the front gate, $Q_n(x)$ is inversion charge density given as

$$Q_n(x) = 2[Q_s(x) - Q_d(x)], \quad (5)$$

$Q_s(x)$ is surface charge density given as

$$Q_s(x) = -C_{ox} [V_{gs} - V_{fb,f} - \phi_c(x)], \quad (6)$$

and $Q_d(x)$ is depletion charge density given as

$$Q_d(x) = \sqrt{2qN_b\epsilon_{si}}\sqrt{\phi_s(x)}. \quad (7)$$

Substituting the value of $\mu_n(x)$, $Q_n(x)$, $Q_s(x)$ and $Q_d(x)$ from Eqs. (2), (5), (6) and (7) in Eq. (1), we have

$$I_{DS}dx = \frac{2W\mu_{no}}{\left[1 + \left(\frac{E(x)}{E_C}\right)^2\right]^{1/2}} \left[-C_{ox} (V'_{gs} - \phi_c(x)) - (2qN_b\epsilon_{si})^{1/2} \sqrt{\phi_s(x)}\right] d\phi_c(x). \quad (8)$$

The relationship between surface potential $\phi_s(x)$ and centre potential $\phi_c(x)$ is^[17] given as

$$\phi_c(x) = (H + 1)\phi_s(x) - HV'_{gs}, \quad H = \epsilon_{ox}t_{si}/4\epsilon_{si}t_{ox}. \quad (9)$$

Substituting the value of $\phi_c(x)$ from Eq. (9) in Eq. (8), we have

$$I_{DS}dx = \frac{-2W\mu_{no}}{\left[1 + \left(\frac{E(x)}{E_C}\right)^2\right]^{1/2}} \left[C_{ox} (V'_{gs} - (H + 1)\phi_s(x) + HV'_{gs}) + (2qN_b\epsilon_{si})^{1/2} \sqrt{\phi_s(x)}\right] d\phi_c(x). \quad (10)$$

Substituting the value of $E(x)$ from Eq. (3) in Eq. (10), we have

$$I_{DS}dx = -2W\mu_{no} \left[C_{ox} (V'_{gs} - (H + 1)\phi_s(x) + HV'_{gs}) + (2qN_b\epsilon_{si})^{1/2} \sqrt{\phi_s(x)}\right] \left[1 + \frac{C_{ox}^2}{\epsilon_{si}^2 E_C^2} (-V'_{gs} + (H + 1)\phi_s(x) - HV'_{gs})^2\right]^{1/2} d\phi_c(x),$$

$$I_{DS}dx = 2W\mu_{no} \left[-C_{ox} (V'_{gs} - (H + 1)\phi_s(x) + HV'_{gs}) - T_1 \sqrt{\phi_s(x)}\right] \left[1 + \frac{C_{ox}^2}{\epsilon_{si}^2 E_C^2} (-V'_{gs} + (H + 1)\phi_s(x) - HV'_{gs})^2\right]^{1/2} d\phi_c(x),$$

$$I_{DS}dx = 2W\mu_{no} \left[-C_{ox} (1 + H)(V'_{gs} - \phi_s(x)) - T_1 \sqrt{\phi_s(x)}\right] \times \left[1 + T_2 (\phi_s(x) - V'_{gs})^2\right]^{1/2} (1 + H) d\phi_s(x),$$

$$I_{DS}dx = \frac{2W\mu_{no} \left[T_4 (-V'_{gs} + \phi_s(x)) - T_1 \sqrt{\phi_s(x)}\right]}{\left[1 + T_2 (\phi_s(x) - V'_{gs})^2\right]^{1/2}} \times (1 + H) d\phi_s(x),$$

$$I_{DS}dx = \frac{2W\mu_{no} \left[T_4 (\phi_s(x) - V'_{gs}) - T_1 \sqrt{\phi_s(x)}\right]}{\left[1 + T_2 (\phi_s(x) - V'_{gs})^2\right]^{1/2}} \times (1 + H) d\phi_s(x),$$

or

$$I_{DS} = \int \frac{T_3 \left[T_4 (\phi_s(x) - V'_{gs}) - T_1 \sqrt{\phi_s(x)}\right]}{\left[1 + T_2 (\phi_s(x) - V'_{gs})^2\right]^{1/2}} d\phi_s(x), \quad (11)$$

where $T_1 = \sqrt{2qN_b\epsilon_{si}}$, $T_2 = \frac{C_{ox}^2(1+H)^2}{\epsilon_{si}^2 E_C^2}$, $T_3 = \frac{2W\mu_{no}(1+H)}{L}$, and $T_4 = C_{ox} (1 + H)$.

Integrating Eq.(11) between the limits V_{bi} and $V_{bi} + V_{DS}$, I_{DS} is given by

$$I_{DS} = \int \frac{T_3 \left[T_4 (\phi_s(x) - V'_{gs}) - T_1 \sqrt{\phi_s(x)}\right]}{\left[1 + T_2 (\phi_s(x) - V'_{gs})^2\right]^{1/2}} d\phi_s(x). \quad (12)$$

Rewriting

$$I_{DS} = I_1 + I_2, \quad (13)$$

where

$$I_1 = T_3 T_4 \int_{\theta_1}^{\theta_2} \frac{\phi_s(x) - V'_{gs}}{\left[1 + T_2 (\phi_s(x) - V'_{gs})^2\right]^{1/2}} d\phi_s(x),$$

and

$$I_2 = \int_{\theta_1}^{\theta_2} \frac{T_1 T_3 \sqrt{\phi_s(x)}}{\left[1 + T_2 (\phi_{S1}(x) - V'_{gs})^2\right]^{1/2}} d\phi_s(x),$$

where $\tan \theta = \sqrt{T_2} (\phi_s(x) - V'_{gs})$, $d\phi_s(x) = \frac{\sec^2 \theta}{\sqrt{T_2}} d\theta$,

$$\theta = \tan^{-1}[\sqrt{T_2}(\phi_s(x) - V'_{gs})],$$

$$\theta_1 = \tan^{-1}[\sqrt{T_2}(V_{bi} - V'_{gs})],$$

$$\theta_2 = \tan^{-1}[\sqrt{T_2}(V_{bi} + V_{ds} - V'_{gs})].$$

3. Calculation of g_m

The transconductance of channel of a double-gate fully depleted nanoscale SOI MOSFET is obtained by differentiating drain current with respect to the gate-to-source voltage V_{GS} and is given by

$$g_m = \frac{\partial I_{DS}}{\partial V_{gs}}, \quad V_{ds} = \text{constant.} \quad (14)$$

Since $I_{DS} = I_1 + I_2$,

$$\frac{\partial I_1}{\partial V_{gs}} = \frac{T_3 T_4}{\sqrt{T_2}} \times \left[\frac{\sec \theta_2 \tan \theta_2 (-\sqrt{T_2})}{1 + T_2 (V_{bi} + V_{ds} - V'_{gs})^2} - \frac{\sec \theta_1 \tan \theta_1 (-\sqrt{T_2})}{1 + T_2 (V_{bi} - V'_{gs})^2} \right],$$

$$\frac{\partial I_1}{\partial V_{gs}} = -\frac{T_3 T_4}{\sqrt{T_2}} \times \left[\frac{\sec \theta_2 \tan \theta_2 (\sqrt{T_2})}{1 + T_2 (V_{bi} + V_{ds} - V'_{gs})^2} - \frac{\sec \theta_1 \tan \theta_1 (\sqrt{T_2})}{1 + T_2 (V_{bi} - V'_{gs})^2} \right],$$

$$\begin{aligned} \frac{\partial I_2}{\partial V_{gs}} &= \frac{T_1 T_3}{T_2} \times \left[\frac{\sec \theta_2 \tan \theta_2 (-\sqrt{T_2})}{1 + T_2 (V_{bi} + V_{ds} - V'_{gs})^2} - \frac{\sec \theta_1 \tan \theta_1 (-\sqrt{T_2})}{1 + T_2 (V_{bi} - V'_{gs})^2} \right] \\ &+ \frac{T_1 T_3}{\sqrt{T_2}} [\ln(\sec \theta_2 + \tan \theta_2) - \ln(\sec \theta_1 + \tan \theta_1)] \\ &+ \frac{T_1 T_3}{\sqrt{T_2}} V'_{gs} \left[\frac{\sec \theta_2 \tan \theta_2 \sqrt{T_2} (-1)}{\sec \theta_2 \tan \theta_2 [1 + T_2 (V_{bi} + V_{ds} - V'_{gs})^2]} + \frac{\sec^2 \theta_2 (-\sqrt{T_2})}{1 + T_2 (V_{bi} + V_{ds} - V'_{gs})^2} \right] - \frac{1}{\sec \theta_1 + \tan \theta_1} \\ &\times \left[\frac{\sec \theta_1 \tan \theta_1 (-\sqrt{T_2})}{1 + T_2 (V_{bi} - V'_{gs})^2} + \frac{\sec^2 \theta_2 (-\sqrt{T_2})}{1 + T_2 (V_{bi} - V'_{gs})^2} \right], \end{aligned}$$

$$\begin{aligned} \frac{\partial I_2}{\partial V_{gs}} &= \frac{T_1 T_3}{T_2} (-\sqrt{T_2}) \\ &\times \left[\frac{\sec \theta_2 \tan \theta_2}{1 + T_2 (V_{bi} + V_{ds} - V'_{gs})^2} - \frac{\sec \theta_1 \tan \theta_1}{1 + T_2 (V_{bi} - V'_{gs})^2} \right] \\ &+ \frac{T_1 T_3}{\sqrt{T_2}} [\ln(\sec \theta_2 + \tan \theta_2) - \ln(\sec \theta_1 + \tan \theta_1)] \\ &+ \frac{T_1 T_3}{\sqrt{T_2}} V'_{gs} (-T_2) \times \left[\frac{\sec \theta_2}{1 + T_2 (V_{bi} + V_{ds} - V'_{gs})^2} - \frac{\sec \theta_1}{1 + T_2 (V_{bi} + V_{ds} - V'_{gs})^2} \right]. \end{aligned}$$

4. Calculation of cut-off frequency

On a sub-100 nm scale, MOSFETs are expected to undergo rapid fundamental changes, which are likely to include variations of SOI MOSFETs and double-gate MOSFETs. Double-gate SOI MOSFETs are also widely recognized as one of the most promising devices because of their short channel effect immunity, reduced leakage current and greater scaling potential. In addition to digital circuits, symmetric double-gate fully depleted nanoscale SOI MOSFET devices will be strong contenders for analog RF applications in the wireless communication market. The majority of these RF CMOS studies, however, place the emphasis on understanding a few RF figure of merits such as cut-off frequency, linearity, maximum oscillation frequency and the noise figure. In this paper, the authors have carried out an analytical analysis of the cut-off frequency for a symmetric double-gate fully depleted nanoscale SOI MOSFET. Cut-off frequency f_T is one of the important figures of merit of low-voltage, high-speed devices.

f_T is calculated using

$$f_T = \frac{g_m}{2\pi L W C_T}, \quad (15)$$

where g_m is transconductance, L is channel length, W is channel width and C_T is device capacitance.

5. Calculation of capacitance C_T

An equivalent circuit of a symmetric double-gate fully depleted nanoscale SOI MOSFET for its capacitance determination is shown in Fig. 2.

$$C_T = \frac{C_{ox} (C_{dp} + C_{ss})}{C_{ox} + 2 (C_{dp} + C_{ss})}. \quad (16)$$

The interface capacitance^[18] is given by $C_{ss} = qN_{ss}$, where N_{ss} is the interface surface density and C_{ox} is the oxide layer capacitance, given by $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$, $C_{dp} = \frac{C_d}{2}$, C_d is the depletion layer capacitance and is obtained by differentiating Q_d with respect to V_{gs} , therefore,

$$C_d = \sqrt{\frac{qN_b \epsilon_{si}}{2\phi_s(x)}} \frac{d\phi_s(x)}{dV_{gs}}. \quad (17)$$

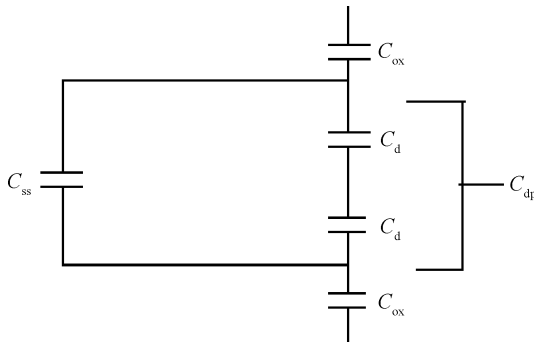


Fig. 2. Equivalent circuit for device capacitance.

$\phi_S(x)$, D_{sf} , D_{sb} , d_0 , d_1 , d_2 , h_{1m} , h_{3m} , t_{mn1} , t_{mn3} for double-gate fully depleted nanoscale SOI MOSFETs are defined elsewhere^[13] are given as

$$\begin{aligned} \phi_S(x) &= \frac{-qN_b}{\epsilon_{si}}x(L-x) + V_{bi} + \frac{x}{L}V_{ds} \\ &- \sum_{m=1}^{\infty} \frac{\sin \frac{m\pi}{L}x}{\epsilon_{si} \frac{m\pi}{L} \sinh \frac{m\pi}{L}t_{si}} \times \left[D_{sf} \cosh \left(\frac{m\pi}{L}t_{si} \right) - D_{sb} \right], \\ D_{sf} &= \frac{\epsilon_{si}}{d_0} \frac{m\pi}{L} \left[\frac{Ld_2}{\sinh \left(\frac{m\pi}{L}t_{si} \right)} - Ld_1 \left\{ \frac{1}{\tanh \left(\frac{m\pi}{L}t_{si} \right)} \right. \right. \\ &\quad \left. \left. + \frac{\epsilon_{si}}{\epsilon_{ox}} \tanh \left(\frac{m\pi}{L}t_{ob} \right) \right\} \right], \\ D_{sb} &= \frac{\epsilon_{si}}{d_0} \frac{m\pi}{L} \left[Ld_2 \left\{ \frac{1}{\tanh \left(\frac{m\pi}{L}t_{si} \right)} + \frac{\epsilon_{si}}{\epsilon_{ox}} \tanh \left(\frac{m\pi}{L}t_{of} \right) \right\} \right. \\ &\quad \left. - \frac{Ld_1}{\sinh \left(\frac{m\pi}{L}t_{si} \right)} \right] \\ d_0 &= \frac{1}{\left(\sinh \frac{m\pi}{L}t_{si} \right)^2} - \left(\frac{1}{\tanh \frac{m\pi}{L}t_{si}} + \frac{\epsilon_{si}}{\epsilon_{ox}} \tanh \frac{m\pi}{L}t_{of} \right) \\ &\quad \times \left(\frac{1}{\tanh \frac{m\pi}{L}t_{si}} + \frac{\epsilon_{si}}{\epsilon_{ox}} \tanh \frac{m\pi}{L}t_{ob} \right), \\ d_1 &= -piq + \frac{4L}{\pi} \frac{V_{gs}}{\cosh \left(\frac{m\pi}{L}t_{of} \right)} + h_{1m}, \\ d_2 &= -piq + \frac{4L}{\pi} \frac{V_{bs}}{\cosh \left(\frac{m\pi}{L}t_{ob} \right)} + h_{3m}, \end{aligned}$$

$$\begin{aligned} h_{1m} &= t_{mn1} \left[M_{1s} + (-1)^{m+1} M_{1d} \right], \\ h_{3m} &= t_{mn3} \left[P_{3s} + (-1)^{m+1} P_{3d} \right], \\ t_{mn1} &= \frac{L^2}{m\pi} \left[1 + \frac{L^2 (n-0.5)^2}{t_{of}^2 m^2} \right]^{-1}, \\ t_{mn3} &= \frac{L^2}{m\pi} \left[1 + \frac{L^2 (n-0.5)^2}{t_{ob}^2 m^2} \right]^{-1}, \end{aligned}$$

$$\begin{aligned} \frac{d\phi_s}{dV_{gs}} &= - \sum_{m=1}^{\infty} \frac{\sin \frac{m\pi}{L}x}{\epsilon_{si} \frac{m\pi}{L} \sinh \left(\frac{m\pi}{L}t_{si} \right)} \\ &\quad \times \left[\frac{dD_{sf}}{dV_{gs}} \cosh \left(\frac{m\pi}{L}t_{si} \right) - \frac{dD_{sb}}{dV_{gs}} \right]. \end{aligned} \quad (18)$$

Now:

$$\begin{aligned} \frac{dD_{sf}}{dV_{gs}} &= \frac{\epsilon_{si}}{d_0} \frac{m\pi}{L} \left[\frac{L}{\sinh \left(\frac{m\pi}{L}t_{si} \right)} \frac{dd_2}{dV_{gs}} - L \frac{dd_1}{dV_{gs}} \right. \\ &\quad \left. \times \left(\frac{1}{\tanh \left(\frac{m\pi}{L}t_{si} \right)} + \frac{\epsilon_{si}}{\epsilon_{ox}} \tanh \left(\frac{m\pi}{L}t_{ob} \right) \right) \right], \\ \frac{dd_1}{dV_{gs}} &= \frac{4L}{\pi} \frac{1}{\cosh \left(\frac{m\pi}{L}t_{of} \right)} + \frac{dh_{1m}}{dV_{gs}}, \\ \frac{dh_{1m}}{dV_{gs}} &= t_{mn1} \left[\frac{dM_{1s}}{dV_{gs}} + (-1)^{m+1} \frac{dM_{1d}}{dV_{gs}} \right] = 0, \\ \frac{dd_1}{dV_{gs}} &= \frac{4L}{\pi} \frac{1}{\cosh \left(\frac{m\pi}{L}t_{of} \right)}, \\ \frac{dd_2}{dV_{gs}} &= \frac{dh_{3m}}{dV_{gs}} = t_{mn3} \frac{d}{dV_{gs}} \left[P_{3s} + (-1)^{m+1} P_{3d} \right] = 0, \\ \frac{dD_{sf}}{dV_{gs}} &= \frac{\epsilon_{si}}{d_0} (-L) \frac{4L}{\pi} \frac{1}{\cosh \left(\frac{m\pi}{L}t_{of} \right)} \\ &\quad \times \left[\frac{1}{\tanh \left(\frac{m\pi}{L}t_{si} \right)} + \frac{\epsilon_{si}}{\epsilon_{ox}} \tanh \left(\frac{m\pi}{L}t_{ob} \right) \right], \\ \frac{dD_{sf}}{dV_{gs}} &= - \frac{\epsilon_{si}(4Lm)}{d_0 \cosh \left(\frac{m\pi}{L}t_{of} \right)} \\ &\quad \times \left[\frac{1}{\tanh \left(\frac{m\pi}{L}t_{si} \right)} + \frac{\epsilon_{si}}{\epsilon_{ox}} \tanh \left(\frac{m\pi}{L}t_{ob} \right) \right], \end{aligned} \quad (19)$$

$$\frac{dD_{sb}}{dV_{gs}} = \frac{\epsilon_{si}}{d_0} \frac{m\pi}{L} \left[L \frac{dd_2}{dV_{gs}} \left\{ \frac{1}{\tanh\left(\frac{m\pi}{L}t_{si}\right)} + \frac{\epsilon_{si}}{\epsilon_{ox}} \tanh\left(\frac{m\pi}{L}t_{ob}\right) \right\} - \frac{Ldd_1}{dV_{gs}} \frac{1}{\sinh\left(\frac{m\pi}{L}t_{si}\right)} \right], \quad (20)$$

$$\frac{dD_{sb}}{dV_{gs}} = \frac{\epsilon_{si}}{d_0} \frac{m\pi}{L} \left[-L \frac{4L}{\pi} \frac{1}{\cosh\left(\frac{m\pi}{L}t_{of}\right)} \frac{1}{\sinh\left(\frac{m\pi}{L}t_{si}\right)} \right],$$

$$\frac{dD_{sb}}{dV_{gs}} = -\frac{\epsilon_{si}(4Lm)}{d_0 \sinh\left(\frac{m\pi}{L}t_{si}\right)} \frac{1}{\cosh\left(\frac{m\pi}{L}t_{of}\right)},$$

$$\frac{d\phi_s}{dV_{gs}} = -\sum_{m=1}^{\infty} \left\{ \frac{\sin\left(\frac{m\pi}{L}x\right)}{\epsilon_{si} \frac{m\pi}{L} \sinh\left(\frac{m\pi}{L}t_{si}\right)} \times \left[\frac{dD_{sf}}{dV_{gs}} \cosh\left(\frac{m\pi}{L}t_{si}\right) - \frac{dD_{sb}}{dV_{gs}} \right] \right\}$$

Substituting for $\frac{dD_{sf}}{dV_{gs}}$ and $\frac{dD_{sb}}{dV_{gs}}$ from Eqs. (19) and (20) in Eq. (18), we have

$$\begin{aligned} \frac{d\phi_s}{dV_{gs}} = & -\sum_{m=1}^{\infty} \frac{\sin\left(\frac{m\pi}{L}x\right)}{\epsilon_{si} \frac{m\pi}{L} \sinh\left(\frac{m\pi}{L}t_{si}\right)} \\ & \times \left\{ -\frac{\epsilon_{si}(4Lm)}{d_0 \cosh\left(\frac{m\pi}{L}t_{of}\right)} \right. \\ & \times \left[\frac{1}{\tanh\left(\frac{m\pi}{L}t_{si}\right)} + \frac{\epsilon_{si}}{\epsilon_{ox}} \tanh\left(\frac{m\pi}{L}t_{ob}\right) \right] \\ & \left. \times \cosh\left(\frac{m\pi}{L}t_{si}\right) - \frac{\epsilon_{si}(4Lm)}{d_0 \sinh\left(\frac{m\pi}{L}t_{si}\right)} \frac{1}{\cosh\left(\frac{m\pi}{L}t_{of}\right)} \right\} \end{aligned}$$

or

$$\frac{d\phi_s}{dV_{gs}} = -b \left[-\frac{\epsilon_{si}(4Lm)}{d_0 p} \left(\frac{1}{u} + \frac{\epsilon_{si}}{\epsilon_{ox}} w \right) s - \frac{\epsilon_{si}(4Lm)}{d_0 v} \frac{1}{p} \right], \quad (21)$$

where $b = \sum_{m=1}^{\infty} \frac{\sin\left(\frac{m\pi}{L}x\right)}{\epsilon_{si}\left(\frac{m\pi}{L}\right) \sinh\left(\frac{m\pi}{L}t_{si}\right)}$, $p = \cosh\left(\frac{m\pi}{L}t_{of}\right)$, $w = \tanh\left(\frac{m\pi}{L}t_{ob}\right)$, $v = \sinh\left(\frac{m\pi}{L}t_{si}\right)$, $s = \cosh\left(\frac{m\pi}{L}t_{si}\right)$, $u = \tanh\left(\frac{m\pi}{L}t_{si}\right)$.

Substituting for $\frac{d\phi_s(x)}{dV_{gs}}$ from Eq. (21) in Eq. (17), we have

$$C_d = \sqrt{\frac{qN_b\epsilon_{si}}{2\phi_s(x)}} - b \left[-\frac{\epsilon_{si}(4Lm)}{d_0 p} \left(\frac{1}{u} + \frac{\epsilon_{si}}{\epsilon_{ox}} w \right) s - \frac{\epsilon_{si}(4Lm)}{d_0 v} \frac{1}{p} \right]. \quad (22)$$

Since $C_T = \frac{C_{ox}(C_{dp} + C_{ss})}{C_{ox} + 2(C_{dp} + C_{ss})}$ and $C_{dp} = \frac{C_d}{2}$, $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$,

$$C_T = \frac{C_{ox}(C_d/2 + C_{ss})}{C_{ox} + 2(C_d/2 + C_{ss})}$$

$$C_T = \frac{C_{ox}(0.5C_d + C_{ss})}{C_{ox} + (C_d + 2C_{ss})}$$

$$C_T = \frac{0.5C_d C_{ox}}{C_{ox} + C_d + 2C_{ss}} + \frac{C_{ox} C_{ss}}{C_{ox} + C_d + 2C_{ss}}. \quad (23)$$

Now substituting for g_m from Eqs. (17) and (18) in Eq. (19) we have

$$\begin{aligned} f_T = & -\frac{T_3 T_4}{\sqrt{T_2}} \times \\ & \left[\frac{\sec \theta_2 \tan \theta_2 (\sqrt{T_2})}{\left[1 + T_2 (V_{bi} + V_{ds} - V'_{gs})^2 \right]} - \frac{\sec \theta_1 \tan \theta_1 (\sqrt{T_2})}{\left[1 + T_2 (V_{bi} - V'_{gs})^2 \right]} \right] \\ & + \frac{T_1 T_3}{T_2} (-\sqrt{T_2}) \left[\frac{\sec \theta_2 \tan \theta_2}{\left(1 + T_2 (V_{bi} + V_{ds} - V'_{gs})^2 \right)} - \frac{\sec \theta_1 \tan \theta_1}{\left(1 + T_2 (V_{bi} - V'_{gs})^2 \right)} \right] \\ & + \frac{T_1 T_3}{\sqrt{T_2}} [\ln(\sec \theta_2 + \tan \theta_2) - \ln(\sec \theta_1 + \tan \theta_1)] \\ & + \frac{T_1 T_3}{\sqrt{T_2}} V'_{gs} (-T_2) \left[\frac{\sec \theta_2}{\left(1 + T_2 (V_{bi} + V_{ds} - V'_{gs})^2 \right)} - \frac{\sec \theta_1}{\left(1 + T_2 (V_{bi} + V_{ds} - V'_{gs})^2 \right)} \right] \times \frac{1}{2\pi L W C_T}. \quad (24) \end{aligned}$$

6. Results and discussion

The simulated device structure is a symmetric double-gate fully depleted SOI MOSFET with source/drain regions doped

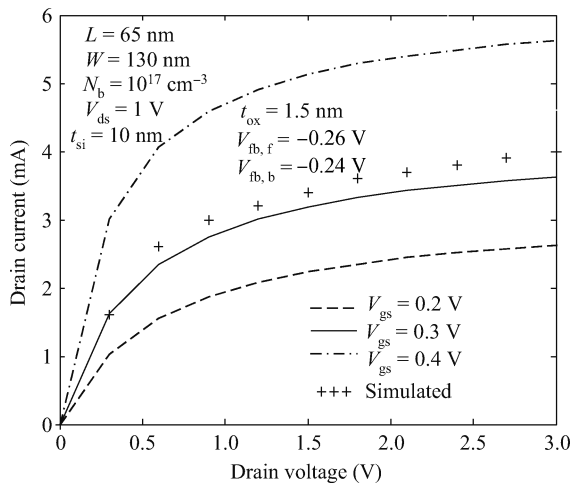


Fig. 3. Drain current versus drain voltage of a symmetric double-gate fully depleted nanoscale SOI MOSFET with different values of gate-to-source voltage.

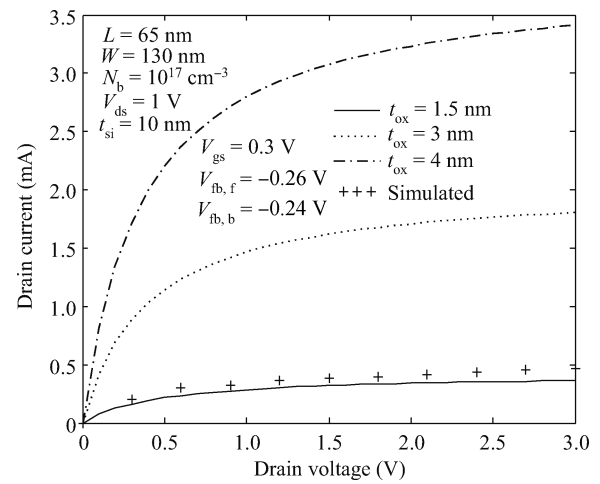


Fig. 5. Drain current versus drain voltage of a symmetric double-gate fully depleted nanoscale SOI MOSFET with different values of gate oxide thickness.

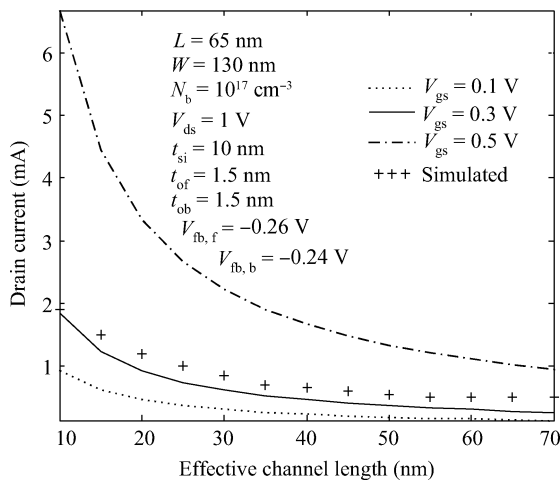


Fig. 4. Drain current versus channel length of a symmetric double-gate fully depleted nanoscale SOI MOSFET with different values of gate-to-source voltage.

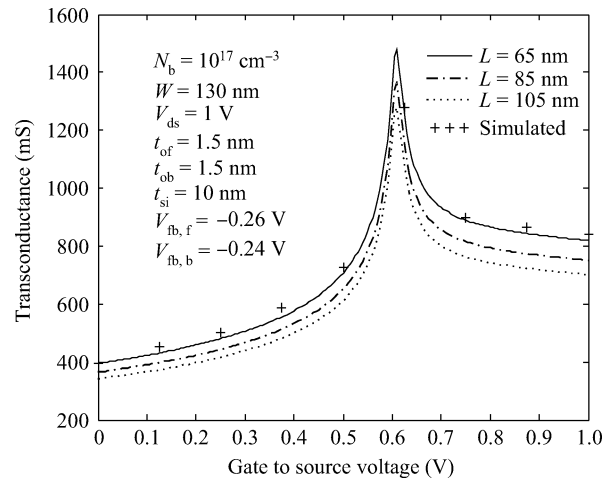


Fig. 6. Transconductance as function of gate-to-source voltage of a symmetric double-gate fully depleted nanoscale SOI MOSFET with different values of channel length.

at 10^{20} m^{-3} , a lightly doped channel with doping levels of p-type SOI layer is 10^{17} m^{-3} . The channel length is 65 nm, channel width is 130 nm, source/drain lengths are 10 nm, the top and bottom gate oxide thickness are $t_{of} = t_{ob} = t_{ox} = 1.5 \text{ nm}$, the silicon layer thickness (t_{si}) of the simulated SOI nMOSFET devices is 10 nm. The silicon layer thickness is chosen to avoid quantum mechanical influences perpendicular to the gate oxide/silicon layer interface because it is anticipated that a sub-5-nm thick silicon layer would cause many quantum mechanical effects to the detriment of the transport characteristics. The metal gate work function is 4.25 eV. The same gate voltage V_{gs} is applied to both gates. Low field mobility (μ_{no}) is $750 \text{ cm}^2/(\text{V}\cdot\text{s})$ and all simulations were carried out at room temperature i.e. at $T = 300 \text{ K}$.

Figure 3 shows the variation of drain-to-source current in the channel with drain voltage for different values of gate-to-source voltages. As shown in Fig. 3, for a given value of $V_{gs} \geq V_{TH}$, drain current increases initially with an increase in drain voltage and finally reaches saturation as V_{ds} is made

large. Drain current saturation is due to pinching off the channel near the drain end. Pinch-off takes place when the voltage across the oxide falls below a critical value and results in a reduction in the electric field. When the electric field decreases to such a extent that it cannot support sufficient mobile charges in a given part of the channel then that region decreases to almost zero thickness and pinch-off takes place. Also drain current increases as gate-to-source voltage increases.

Figure 4 shows the variation of drain current with channel length for different values of gate-to-source voltages. This shows that the drain current increases when channel length decreases. This increase in drain current is due to channel length modulation. Figure 5 shows variation of drain current with drain-to-source voltage for different values of gate oxide thickness. As oxide thickness increases, mobility and hence drain current increases due to less surface-induced scattering.

Figure 6 shows plots of transconductance versus gate-to-source voltage for different values of channel length. Transconductance increases with an increase in gate-to-source voltage

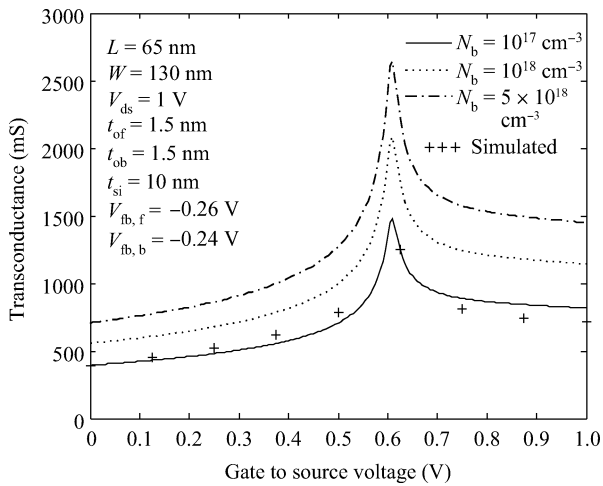


Fig. 7. Transconductance as a function of gate-to-source voltage of a symmetric double-gate fully depleted nanoscale SOI MOSFET with different values of channel doping concentration.

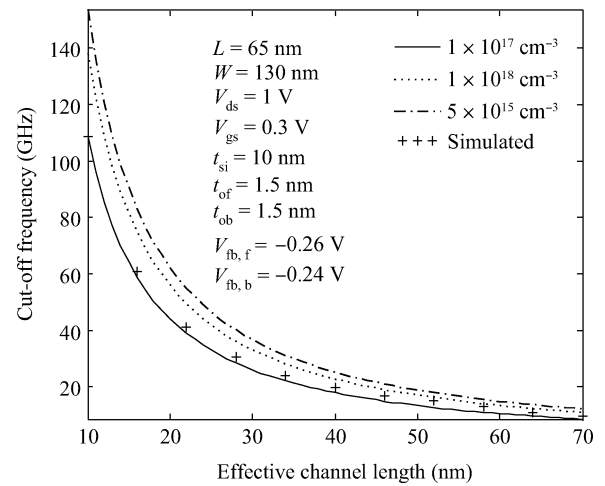


Fig. 9. Cut-off frequency versus channel length for different values of doping concentration.

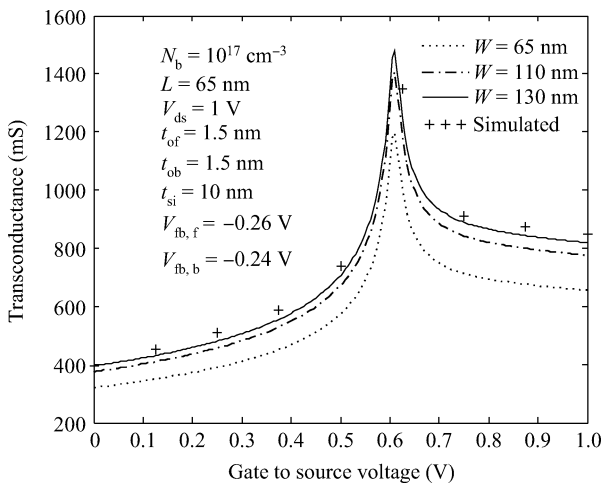


Fig. 8. Transconductance as function of gate-to-source voltage of a symmetric double-gate fully depleted nanoscale SOI MOSFET with different values of channel width.

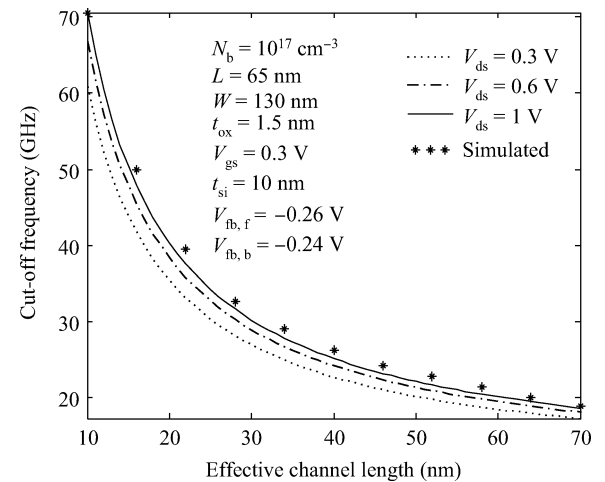


Fig. 10. Cut-off frequency versus channel thickness for different values of drain-to-source voltage.

because of an increased number of carriers moving close to the surface from the source to the drain region making a channel more conducting. Also transconductance depends on the device dimensions. Figure 7 shows the variation of transconductance with gate-to-source voltage for different values of doping concentrations. Transconductance increases as doping concentration increases due to an increased number of charge carriers.

Figure 8 shows the variation of transconductance with the gate-to-source voltage for different values of channel width. As channel width increases, current driving capability increases, hence transconductance increases. Figure 9 shows the variation of cut-off frequency with effective channel length for different values of doping concentrations. An increase in doping concentration increases the cut-off frequency due to an increase in the number of charge carriers.

Figure 10 shows the variation of cut-off frequency with effective channel length for different values of drain-to-source voltages. As the drain-to-source voltage increases, the number of charge carriers increases, which in turn increases the current

and transconductance. Since cut-off frequency is directly proportional to transconductance, an increase in transconductance increases the cut-off frequency. Figure 11 shows a variation in cut-off frequency with effective channel length for different gate oxide layer thicknesses. Figure 12 shows a variation of cut-off frequency with silicon layer thickness for different values of channel length. Cut-off frequency is inversely proportional to silicon layer thickness. As the silicon layer thickness increases, cut-off frequency decreases because of increased device capacitance and decreased transconductance.

7. Conclusion

A two dimensional analytical drain current model for a symmetric double-gate fully depleted nanoscale SOI MOSFET is proposed in this paper. The dependence of drain current, transconductance and cut-off frequency on parameters such as channel length, channel width, channel doping, channel thickness, gate oxide thickness, gate-to-source voltage and drain-to-source voltage are discussed. The model results are found to be well matched with the commercially available 2D ATLAS de-

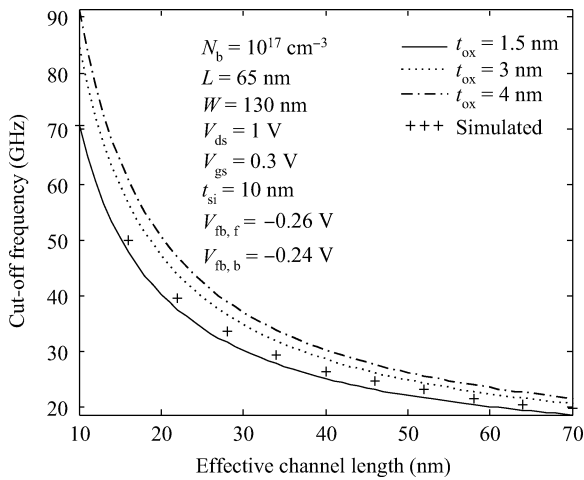


Fig. 11. Cut-off frequency versus channel length for different values of oxide layer thickness.

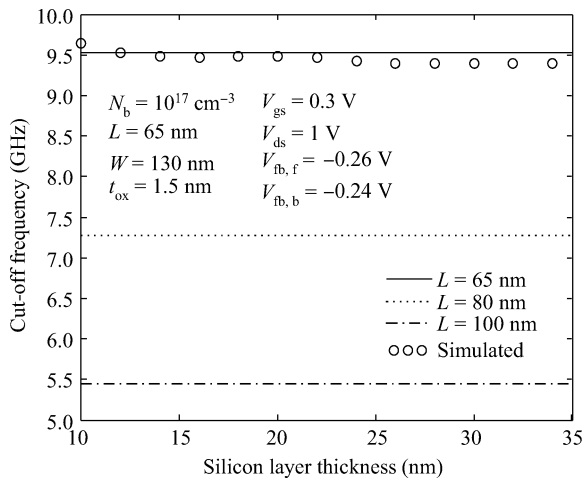


Fig. 12. Cut-off frequency versus silicon layer thickness for different values of channel length.

vice simulation results.

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