Analytical modeling of drain current and RF performance for double-gate fully depleted nanoscale SOI MOSFETs

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Abstract: A new 2D analytical drain current model is presented for symmetric double-gate fully depleted nanoscale SOI MOSFETs. Investigation of device parameters like transconductance for double-gate fully depleted nanoscale SOI MOSFETs is also carried out. Finally this work is concluded by modeling the cut-off frequency, which is one of the main figures of merit for analog/RF performance for double-gate fully depleted nanoscale SOI MOSFETs. The results of the modeling are compared with those obtained by a 2D ATLAS device simulator to verify the accuracy of the proposed model.

Key words: double-gate; fully depleted; silicon-on-insulator; Poisson’s equation; radio frequency; ATLAS

1. Introduction

A double-gate silicon-on-insulator MOSFET has been studied extensively in recent years and is projected as the device for future processors. Among the different configurations of double-gate MOSFETs, the device physics of symmetric double-gate MOSFETs has been well studied and many compact models have been developed¹⁻¹¹. A rigorous channel potential based drain current model for asymmetric double-gate MOSFETs has been developed by Taur’s group by using direct integration, with the symmetric operation included as a special case¹². Recently, we have developed a potential and threshold voltage model for a double-gate fully depleted nanoscale SOI MOSFET based on the solution of Poisson’s equation using Green’s function solution technique¹³. In this paper, it is extended to model drain current, transconductance and cut-off frequency.

Drain current and transconductance dependence on parameters such as channel length, channel doping, channel thickness, gate oxide thickness and gate to source voltage is discussed. Cut-off frequency dependence on gate oxide thickness, channel doping, gate-to-source voltage and drain-to-source voltage is also discussed. Accuracy of the model is verified by comparing the model results with simulations using a 2D ATLAS device simulator¹⁴. A close match with published results confirms the validity of the model.

2. Analytical model for drain current

The basic structure of a fully depleted double-gate nanoscale SOI MOSFET is shown in Fig. 1.

Neglecting the fixed oxide charge effect, for a strongly inverted n-type double-gate fully depleted nanoscale SOI MOSFET, the current¹⁵ in the channel is given by

\[
I_{DS} = W\mu_n(x)\frac{d\phi_c(x)}{dx},
\]

where \(I_{DS}\) is current in the channel, \(0 \leq x \leq L\), \(W\) is the channel width, \(\mu_n(x)\) is the mobility of electrons given as

\[
\mu_n(x) = \frac{\mu_{no}}{1 + \left(\frac{E(x)}{E_c}\right)^2}^{1/2},
\]

where \(\mu_{no}\) is low field mobility¹⁶, \(E(x)\) is the longitudinal field given by

\[
E(x) = \frac{C_{ox}\left(V_{fb,t} - V_{gs} + \phi_c(x)\right)}{\varepsilon_{si}},
\]

and \(E_c\) is the critical field given by

\[
E_c = \frac{1}{2}\frac{\mu_{no}}{\mu_{hi}}
\]

where \(\mu_{hi}\) is high field mobility.

Fig. 1. Schematic diagram of a double-gate fully depleted nanoscale SOI MOSFET.
\[ E_C = 6.01 \times 10^2 T^{3/2}. \]  
\[ V'_gs = V_{gs} - V_{fb,f}. \text{ } V_{gs} \text{ is gate-to-source voltage, } V_{fb,f} \text{ is flat band voltage of the front gate, } Q_n(x) \text{ is inversion charge density given as} \]
\[ Q_n(x) = 2[Q_s(x) - Q_d(x)]. \]  
\[ Q_s(x) \text{ is surface charge density given as} \]
\[ Q_s(x) = -C_{ox}[V_{gs} - V_{fb,f} - \phi_c(x)]. \]
\[ Q_d(x) \text{ is depletion charge density given as} \]
\[ Q_d(x) = \sqrt{2qN_b\varepsilon_{si}}\phi_c(x). \]

Substituting the value of \( \mu_n(x), Q_n(x), Q_s(x) \) and \( Q_d(x) \) from Eqs. (2), (5), (6) and (7) in Eq. (1), we have
\[ I_{DSdx} = \frac{-2W\mu_n}{1 + \left( \frac{E(x)}{E_C} \right)^2} \left[ -C_{ox}\left(V'_gs - \phi_c(x)\right) \right. \]
\[ \left. - (2qN_b\varepsilon_{si})^{1/2} \phi_c(x) \right] d\phi_c(x). \]

The relationship between surface potential \( \phi_s(x) \) and centre potential \( \phi_c(x) \) is given as
\[ \phi_c(x) = (H + 1)\phi_s(x) - HV'_gs, \quad H = \varepsilon_{ox}\varepsilon_{si}/4\varepsilon_{si}\varepsilon_{ox}. \]

Substituting the value of \( \phi_c(x) \) from Eq. (9) in Eq. (8), we have
\[ I_{DSdx} = \frac{-2W\mu_n}{1 + \left( \frac{E(x)}{E_C} \right)^2} \left[ C_{ox}\left(V'_gs - (H + 1)\phi_s(x) \right) \right. \]
\[ \left. + HV'_gs \right] + (2qN_b\varepsilon_{si})^{1/2} \phi_c(x) d\phi_c(x). \]

Substituting the value of \( E(x) \) from Eq. (3) in Eq. (10), we have
\[ I_{DSdx} = -2W\mu_n \left[ C_{ox}(V'_gs - (H + 1)\phi_s(x) + HV'_gs) \right. \]
\[ \left. + (2qN_b\varepsilon_{si})^{1/2} \phi_c(x) \right] \left[ 1 + \frac{C_{ox}^2}{\varepsilon_{si}^2 E_C^2} \right] \left[-V'_gs \right. \]
\[ \left. + (H + 1)\phi_s(x) - HV'_gs \right]^{1/2} / \
\[ \left. d\phi_c(x) \right]. \]

\[ I_{DSdx} = 2W\mu_n \left[ -C_{ox}(V'_gs - (H + 1)\phi_s(x) + HV'_gs) \right. \]
\[ \left. - T_1\sqrt{\phi_c(x)} \right] \left[ 1 + \frac{C_{ox}^2}{\varepsilon_{si}^2 E_C^2} \right] \left[-V'_gs \right. \]
\[ \left. + (H + 1)\phi_s(x) - HV'_gs \right]^{21/2} / \
\[ \left. d\phi_c(x) \right]. \]
3. Calculation of \( g_m \)

The transconductance of channel of a double-gate fully depleted nanoscale SOI MOSFET is obtained by differentiating drain current with respect to the gate-to-source voltage \( V_{GS} \) and is given by

\[
g_m = \frac{\partial I_{DS}}{\partial V_{GS}}, \quad V_{ds} = \text{constant.} \tag{14}
\]

Since \( I_{DS} = I_1 + I_2 \),

\[
\frac{\partial I_1}{\partial V_{GS}} = \frac{T_3 T_4}{T_2} \times \left[ \frac{\sec \theta_2 \tan \theta_2 \left(-\sqrt{T_2}\right)}{1 + T_2 \left(V_{bi} + V_{ds} - V'_{gs}\right)^2} \right.
\]

\[
\left. - \frac{\sec \theta_1 \tan \theta_1 \left(-\sqrt{T_2}\right)}{1 + T_2 \left(V_{bi} - V'_{gs}\right)^2} \right],
\]

\[
\frac{\partial I_1}{\partial V_{GS}} = -\frac{T_3 T_4}{T_2} \times \left[ \frac{\sec \theta_2 \tan \theta_2 \left(\sqrt{T_2}\right)}{1 + T_2 \left(V_{bi} + V_{ds} - V'_{gs}\right)^2} \right.
\]

\[
\left. - \frac{\sec \theta_1 \tan \theta_1 \left(\sqrt{T_2}\right)}{1 + T_2 \left(V_{bi} - V'_{gs}\right)^2} \right],
\]

\[
\frac{\partial I_2}{\partial V_{GS}} = \frac{T_1 T_3}{T_2} \times \left[ \frac{\sec \theta_2 \tan \theta_2 \left(-\sqrt{T_2}\right)}{1 + T_2 \left(V_{bi} + V_{ds} - V'_{gs}\right)^2} \right.
\]

\[
\left. - \frac{\sec \theta_1 \tan \theta_1 \left(-\sqrt{T_2}\right)}{1 + T_2 \left(V_{bi} - V'_{gs}\right)^2} \right] + \frac{T_1 T_3}{\sqrt{T_2}} \left[ \ln(\sec \theta_2 + \tan \theta_2) - \ln(\sec \theta_1 + \tan \theta_1) \right]
\]

\[
+ \frac{T_1 T_3}{\sqrt{T_2}} V'_{gs} \left[ \frac{\sec \theta_2 \tan \theta_2 \sqrt{T_2} (-1)}{1 + T_2 \left(V_{bi} + V_{ds} - V'_{gs}\right)^2} \right]
\]

\[
+ \frac{\sec^2 \theta_2 \left(-\sqrt{T_2}\right)}{1 + T_2 \left(V_{bi} + V_{ds} - V'_{gs}\right)^2} - \frac{1}{\sec \theta_1 + \tan \theta_1} \cdot \frac{\sec \theta_1 \tan \theta_1 \left(-\sqrt{T_2}\right)}{1 + T_2 \left(V_{bi} - V'_{gs}\right)^2} + \frac{\sec^2 \theta_2 \left(-\sqrt{T_2}\right)}{1 + T_2 \left(V_{bi} - V'_{gs}\right)^2} \right],
\]

\[
\frac{\partial I_2}{\partial V_{GS}} = \frac{T_1 T_3}{T_2} \left( -\sqrt{T_2} \right)
\]

\[
\times \left[ \frac{\sec \theta_2 \tan \theta_2}{1 + T_2 \left(V_{bi} + V_{ds} - V'_{gs}\right)^2} - \frac{\sec \theta_1 \tan \theta_1}{1 + T_2 \left(V_{bi} - V'_{gs}\right)^2} \right]
\]

\[
+ \frac{T_1 T_3}{\sqrt{T_2}} \left[ \ln(\sec \theta_2 + \tan \theta_2) - \ln(\sec \theta_1 + \tan \theta_1) \right]
\]

\[
+ \frac{T_1 T_3}{\sqrt{T_2}} V'_{gs} \left( -T_2 \right) \times \left[ \frac{\sec \theta_2}{1 + T_2 \left(V_{bi} + V_{ds} - V'_{gs}\right)^2} \right]
\]

\[
- \frac{\sec \theta_1 \tan \theta_1}{1 + T_2 \left(V_{bi} - V'_{gs}\right)^2} \right].
\]

4. Calculation of cut-off frequency

On a sub-100 nm scale, MOSFETs are expected to undergo rapid fundamental changes, which are likely to include variations of SOI MOSFETs and double-gate MOSFETs. Double-gate SOI MOSFETs are also widely recognized as one of the most promising devices because of their short channel effect immunity, reduced leakage current and greater scaling potential. In addition to digital circuits, symmetric double-gate fully depleted nanoscale SOI MOSFET devices will be strong contenders for analog RF applications in the wireless communication market. The majority of these RF CMOS studies, however, place the emphasis on understanding a few RF figure of merits such as cut-off frequency, linearity, maximum oscillation frequency and the noise figure. In this paper, the authors have carried out an analytical analysis of the cut-off frequency for a symmetric double-gate fully depleted nanoscale SOI MOSFET. Cut-off frequency \( f_T \) is one of the important figures of merit of low-voltage, high-speed devices.

\[
f_T = \frac{g_m}{2\pi L W C_T}, \tag{15}
\]

where \( g_m \) is transconductance, \( L \) is channel length, \( W \) is channel width and \( C_T \) is device capacitance.

5. Calculation of capacitance \( C_T \)

An equivalent circuit of a symmetric double-gate fully depleted nanoscale SOI MOSFET for its capacitance determination is shown in Fig. 2.

\[
C_T = \frac{C_{ox} \left( C_{dp} + C_{as} \right)}{C_{ox} + 2 \left( C_{dp} + C_{as} \right)}. \tag{16}
\]

The interface capacitance \( \left[ \text{18} \right] \) is given by \( C_{as} = q N_{as} \), where \( N_{as} \) is the interface surface density and \( C_{ox} \) is the oxide layer capacitance, given by \( C_{ox} = \frac{\varepsilon_s}{d}, C_{dp} = \frac{\varepsilon_p}{d}, C_d \) is the depletion layer capacitance and is obtained by differentiating \( Q_d \) with respect to \( V_{gs} \), therefore,

\[
C_d = \left[ \frac{q N_{bi} \varepsilon_s}{2\phi_s(x)} \right] \frac{d\phi_s(x)}{dV_{gs}}. \tag{17}
\]
\[ \phi_{S}(x) = \frac{-qN_{b}}{\varepsilon_{si}} x(L - x) + V_{bi} + \frac{x}{L} V_{gs} \]

\[ D_{sf} = \frac{\varepsilon_{si} m \pi}{d_{0}} \left[ \frac{L d_{2}}{\sinh \left( \frac{m \pi}{L} t_{si} \right)} - L d_{1} \right] \left\{ \tan \left( \frac{m \pi}{L} t_{si} \right) \right\}, \]

\[ D_{ab} = \frac{\varepsilon_{si} m \pi}{d_{0}} \left[ L d_{2} \left\{ \frac{1}{\tan \left( \frac{m \pi}{L} t_{si} \right)} + \frac{\varepsilon_{si}}{\varepsilon_{ox}} \tan \left( \frac{m \pi}{L} t_{of} \right) \right\} \right. \]

\[ = \frac{L d_{1}}{\sinh \left( \frac{m \pi}{L} t_{si} \right)} \]

\[ d_{0} = \frac{1}{\sinh \left( \frac{m \pi}{L} t_{si} \right)} \left[ \frac{1}{\tan \left( \frac{m \pi}{L} t_{si} \right)} + \frac{\varepsilon_{si}}{\varepsilon_{ox}} \tan \left( \frac{m \pi}{L} t_{of} \right) \right], \]

\[ d_{1} = -p i q + \frac{4L}{\pi} \frac{V_{gs}}{\cosh \left( \frac{m \pi}{L} t_{of} \right)} + h_{1m}, \]

\[ d_{2} = -p i q + \frac{4L}{\pi} \frac{V_{gs}}{\cosh \left( \frac{m \pi}{L} t_{of} \right)} + h_{3m}. \]
where \( b = \sum_{m=1}^{\infty} \frac{\sin (\frac{m \pi}{L} x)}{\varepsilon_m \frac{m \pi}{L} \sinh (\frac{m \pi}{L} t_{si})} \), \( p = \cosh (\frac{m \pi}{L} t_{of}) \),
\( w = \tanh (\frac{m \pi}{L} t_{si}) \), \( v = \sinh (\frac{m \pi}{L} t_{si}) \), \( s = \cosh (\frac{m \pi}{L} t_{si}) \), \( u = \tanh (\frac{m \pi}{L} t_{si}) \).

6. Results and discussion

The simulated device structure is a symmetric double-gate fully depleted SOI MOSFET with source/drain regions doped
at $10^{20}$ m$^{-3}$, a lightly doped channel with doping levels of p-type SOI layer is $10^{17}$ m$^{-3}$. The channel length is 65 nm, channel width is 130 nm, source/drain lengths are 10 nm, the top and bottom gate oxide thicknesses are $t_{ox} = 1.5$ nm, the silicon layer thickness ($t_{si}$) of the simulated SOI nMOSFET devices is 10 nm. The silicon layer thickness is chosen to avoid quantum mechanical influences perpendicular to the gate oxide/silicon layer interface because it is anticipated that a sub-5-nm thick silicon layer would cause many quantum mechanical effects to the detriment of the transport characteristics. The metal gate work function is 4.25 eV. The same gate voltage $V_{gs}$ is applied to both gates. Low field mobility ($\mu_{s0}$) is 750 cm$^2$/V-s and all simulations were carried out at room temperature i.e. at $T = 300$ K.

Figure 3 shows the variation of drain-to-source current in the channel with drain voltage for different values of gate-to-source voltages. As shown in Fig. 3, for a given value of $V_{gs} \geq V_{TH}$, drain current increases initially with an increase in drain voltage and finally reaches saturation as $V_{ds}$ is made large. Drain current saturation is due to pinching off the channel near the drain end. Pinch-off takes place when the voltage across the oxide falls below a critical value and results in a reduction in the electric field. When the electric field decreases to such an extent that it cannot support sufficient mobile charges in a given part of the channel then that region decreases to almost zero thickness and pinch-off takes place. Also drain current increases as gate-to-source voltage increases.

Figure 4 shows the variation of drain current with channel length for different values of gate-to-source voltages. This shows that the drain current increases when channel length decreases. This increase in drain current is due to channel length modulation. Figure 5 shows variation of drain current with drain-to-source voltage for different values of gate oxide thickness. As oxide thickness increases, mobility and hence drain current increases due to less surface-induced scattering.

Figure 6 shows plots of transconductance versus gate-to-source voltage for different values of channel length. Transconductance increases with an increase in gate-to-source voltage.
Fig. 7. Transconductance as a function of gate-to-source voltage of a symmetric double-gate fully depleted nanoscale SOI MOSFET with different values of channel doping concentration. Because of an increased number of carriers moving close to the surface from the source to the drain region making a channel more conducting. Also transconductance depends on the device dimensions. Figure 7 shows the variation of transconductance with gate-to-source voltage for different values of doping concentrations. Transconductance increases as doping concentration increases due to an increased number of charge carriers.

Figure 8 shows the variation of transconductance with the gate-to-source voltage for different values of channel width. As channel width increases, current driving capability increases, hence transconductance increases. Figure 9 shows the variation of cut-off frequency with effective channel length for different values of doping concentrations. An increase in doping concentration increases the cut-off frequency due to an increase in the number of charge carriers.

Figure 10 shows the variation of cut-off frequency with effective channel length for different values of drain-to-source voltage. As the drain-to-source voltage increases, the number of charge carriers increases, which in turn increases the current and transconductance. Since cut-off frequency is directly proportional to transconductance, an increase in transconductance increases the cut-off frequency. Figure 11 shows a variation in cut-off frequency with effective channel length for different gate oxide layer thicknesses. Figure 12 shows a variation of cut-off frequency with silicon layer thickness for different values of channel length. Cut-off frequency is inversely proportional to silicon layer thickness. As the silicon layer thickness increases, cut-off frequency decreases because of increased device capacitance and decreased transconductance.

7. Conclusion

A two dimensional analytical drain current model for a symmetric double-gate fully depleted nanoscale SOI MOSFET is proposed in this paper. The dependence of drain current, transconductance and cut-off frequency on parameters such as channel length, channel width, channel doping, channel thickness, gate oxide thickness, gate-to-source voltage and drain-to-source voltage are discussed. The model results are found to be well matched with the commercially available 2D ATLAS de-
Fig. 11. Cut-off frequency versus channel length for different values of oxide layer thickness.

Fig. 12. Cut-off frequency versus silicon layer thickness for different values of channel length.

References


