A low-phase-noise LC-VCO with an enhanced-Q varactor for use in a high-sensitivity GNSS receiver*

Yin Xizhen(尹喜珍)[1,†], Ma Chengyan(马成炎)[1,2], Ye Tianchun(叶甜春)[1], Xiao Shimao(肖时茂)[1], and Jin Yuhua(金玉花)[2]

[1]Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China
[2]Hangzhou Zhongke Microelectronics Co. Ltd, Hangzhou 310053, China

Abstract: An LC-VCO with an enhanced quality factor (Q) varactor for use in a high-sensitivity GNSS receiver is presented. An enhanced A-MOS varactor is composed of two accumulation-mode MOS (A-MOS) varactors and two bias voltages, which show the improved Q and linearization capacitance–voltage (C–V) curve. The VCO gain (K_{VCO}) is compensated by a digital switched varactors array (DSVA) over entire sub-bands. Based on the characteristics of an A-MOS, the varactor in a DSVA is a high Q fixed capacitor as it is switched off, and a moderate Q tuning varactor when it is switched on, which keeps the maximal Q for the LC-tank. The proposed circuit is fabricated in a 0.18 μm 1P6M CMOS process. The measured phase noise is better than –122 dBc/Hz at a 1 MHz offset while the measured tuning range is 58.2% and the variation of K_{VCO} is close to $\pm$21% over the whole of the sub-bands and the effective range of the control voltage. The proposed VCO dissipates less than 5.4 mW over the whole operating range from a 1.8 V supply.

Key words: A-MOS; voltage controlled oscillator; quality factor; VCO gain compensation; CMOS
DOI: 10.1088/1674-4926/33/5/055002 **EEACC:** 1230B; 2570D

1. Introduction

In line of sight (LOS) propagation conditions, the Earth can receive GNSS signal strength of about –130 dBm. The LOS between the satellite and receiver encounters forests, buildings, mountains and other potential obstacles, which can decay a GNSS signal by 10–25 dBm. To enable positioning and navigation under forest canyons, in urban areas, and even inside buildings, high-sensitivity GNSS receivers should be able to receive signals below –155 dBm, which requires that the receiver's local oscillator phase noise is smaller than –120 dBc/Hz @ 1 MHz[1, 2]. This typically requires the choice of passive LC tanks with a high-quality factor (Q). On-chip spire inductors have been popularly used for monolithic LC-tank CMOS oscillators. Many studies have been published that aim at improving the Q of the inductor in order to achieve lower phase noise[3, 4]. Varactors as the tuning element are applied broadly in LC-VCO resonators; they affect the tuning range and phase noise. However, research of increasing the Q of varactors is rare.

VCO gain (K_{VCO}) suffers more than 3× variation over different sub-bands in a conventional wide-band VCO. It is caused by the ratio of varactor to total tank capacitance being reduced along with the band number increase. Furthermore, the K_{VCO} has a large variation over different control voltages (V_{ctrl}) owing to the non-linear relation between capacitance and voltage. The noise sensitivity of a VCO varies with the huge fluctuation of K_{VCO}, and the phase noise is degraded as the VCO gain increases[5]. At the same time, the loop band width of the PLL is changed as the K_{VCO} alters, thus impacting the phase noise and loop stability.

In this paper, high-Q varactor configurations are presented. A linear tuning curve and improved Q are obtained when it as the core varactor. A KVCO compensation with a digital switched varactors array (DSVA) is introduced, which increases the VCO gain at low sub-bands and keeps the maximum Q for the LC tank. The proposed VCO is manufactured in a 0.18 μm CMOS process to demonstrate the low phase noise and K_{VCO} compensation characteristic.

2. Proposed enhanced-Q varactor

2.1. A-MOS varactor

Four types of varactor are mainly used in CMOS processes, they are the: P–N junction varactor, MOS varactor, inversion-mode MOS varactor and accumulation-mode MOS (A-MOS) varactor. The A-MOS, with its wider tuning range and lower parasitical resistor, is the dominant choice in RF oscillators[6, 7]. An A-MOS is formed by placing an NMOS in an N-well, as shown in the top of Fig. 1(a), the gate is the voltage plus port, and the source and drain connected together as the voltage minus port. The simulated character curves of A-MOS varactor are illustrated in Fig. 1(b), the monotonic ascending capacitance–voltage (C–V) curve is shown in top of Fig. 1(b) as the voltage difference, which is varied from –1.8 to 1.8 V, between plus and minus ports, and the capacitance is normalized by C_{max}. The varactor gain (K_{var}) is the derivative of capacitance to the voltage difference, as shown in the middle of Fig. 1(b), and the C–V curve can be divided into three regions based on the K_{var} variation. The voltage difference limited in

* Project supported by the National Significant Science and Technology Projects (No. 2009ZX01031-002-008) and the National High Technology Research and Development Program of China (No. 2009AA011601).
† Corresponding author. Email: yinxizhen@casic.ac.cn
Received 26 September 2011, revised manuscript received 28 November 2011

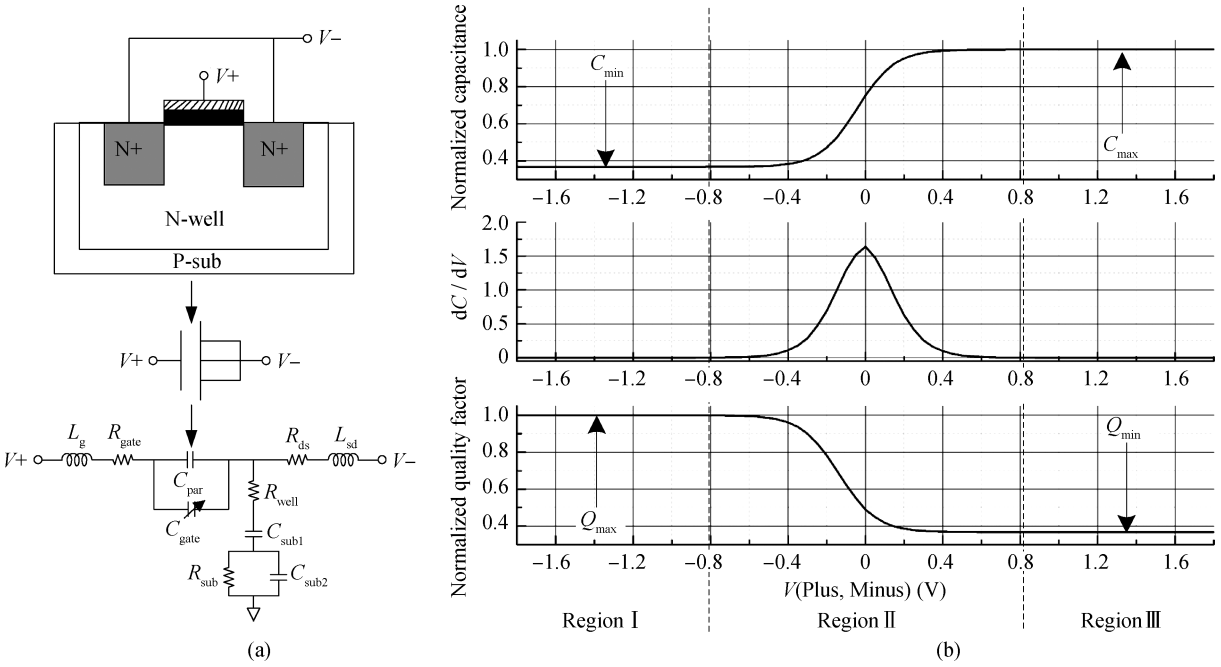

Fig. 1. (a) A-MOS structure and model. (b) Characteristic curves of A-MOS.

the [–1.8, –0.8] V range is called region I, located in area [–0.8, 0.8] V is called region II, and situated in district [0.8, 1.8] V is entitled region III. It could be seen that when the K_{var} is almost zero, the corresponding capacitance is nearly invariable in regions I and III, by and large; the A-MOS varactor is a fixed capacitance. The K_{var} varies with the voltage, and it reaches the maximum when the voltage difference is zero in region II. The monotonic descendent quality factor–voltage (Q–V) curve is shown in the bottom of Fig. 1(b), and the Q is normalized by Q_{max}. The Q equals Q_{max} in region I, and it reaches the minimum Q_{min} in region III, the Q is varied from Q_{max} to Q_{min} in region II.

2.2. Improved Q and tuning curve linearization of E-AMOS

The conventional A-MOS varactror has a narrow linear tuning region with a low quality factor and a high quality factor region with a flat C–V curve, which brings on a small tuning range and high phase noise when used in a VCO. A novel A-MOS varactor scheme is proposed in Fig. 2(a), two serial connected A-MOSs, C_{var1} and C_{var2}, with offset DC bias voltages V_{B1} and V_{B2} comprise the enhanced A-MOS (E-AMOS), with a similar connection, for differential symmetry. V_{B1} and V_{B2} are the DC biases of the A-MOS plus ports; V_{ctrl} is the control voltage and connects to the minus ports through a resistor R.

A model of the A-MOS varactor[8] is modified as shown at the bottom of Fig. 1(a), where R_{gate} is the gate resistor, R_{ds} is the drain–source resistor, L_g and L_{sd} are the parasitic inductance of gate and source/drain individually, C_{gate} is the variable capacitance of the A-MOS varactor, C_{par} is the parasitic capacitance, R_{well}, R_{sub}, C_{sub1}, C_{sub2} are the substrate-related components. Owing to the operating frequency far lower than its resonant frequency, the L_g and L_{sd} are negligible. The quality factor Q_{AMOS} of the A-MOS is defined as

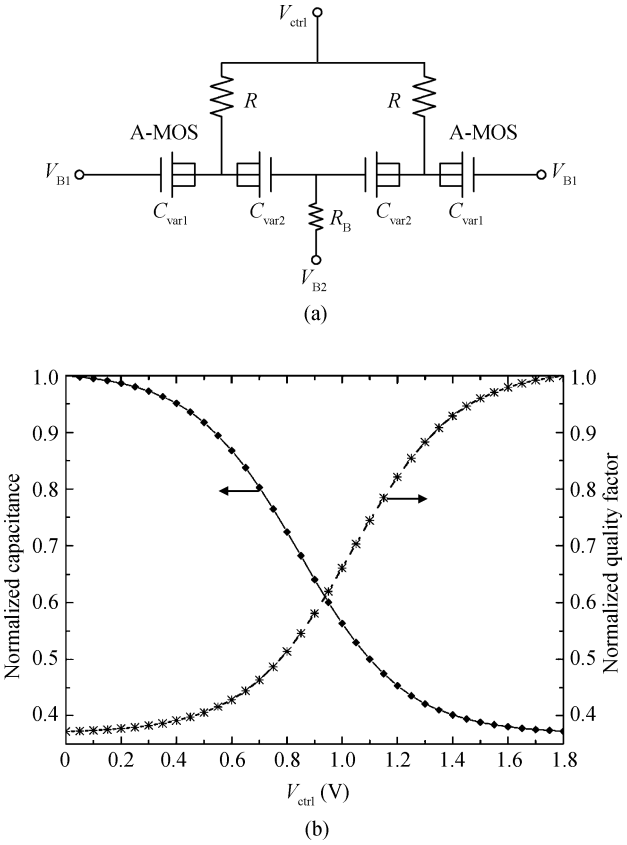

Fig. 2. (a) Scheme of E-AMOS. (b) C–V and Q–V curves of E-AMOS.

$$Q_{AMOS} = \frac{1}{\omega C_{var} R_{var}}, \tag{1}$$

where C_{var} is the effective capacitance and R_{var} is effective series resistor. They can be modeled from the two-port S-

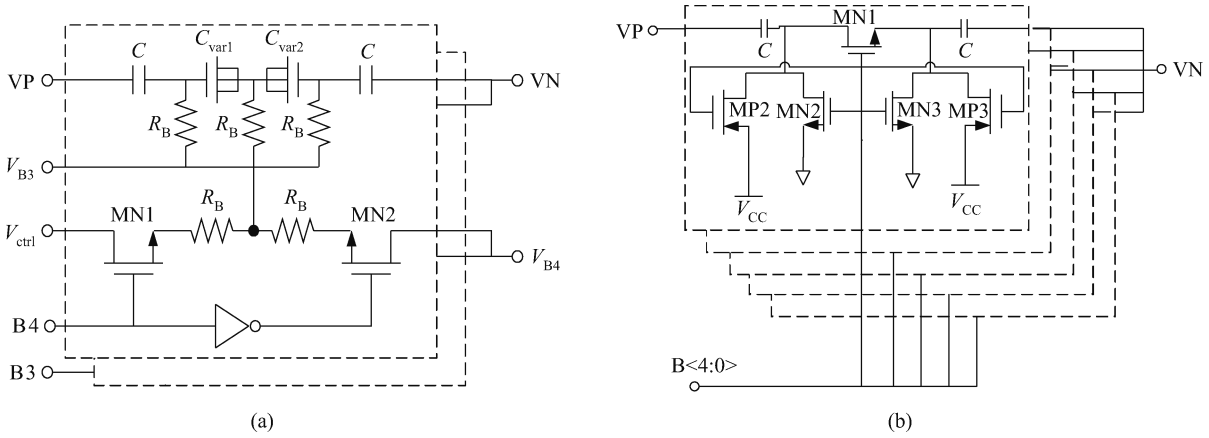

Fig. 3. (a) Proposed DSVA. (b) Proposed DSCA.

parameters by a network analyzer; the admittance looking from the minus port, the equivalent R_{var} and capacitance C_{var} is calculated in Eq. (2).

$$Y = Y_o\frac{1-S_{11}}{1+S_{11}}, \quad R_{var} = \frac{1}{\mathrm{Re}(Y)}, \quad C_{var} = \frac{\mathrm{Im}(Y)}{2\pi f}. \quad (2)$$

The proposed E-AMOS is the two A-MOS varactors in series, so the equivalent quality factor Q_{eq} of E-AMOS is

$$\frac{1}{Q_{eq}} = \frac{1}{Q_{var1}} + \frac{1}{Q_{var2}}, \quad (3)$$

where Q_{var1}, Q_{var2} are the quality factor of C_{var1} and C_{var2} respectively. The proposed E-AMOS Q–V curve is simulated as shown in Fig. 2(b), which is normalized by Q_{max}. The Q_{eq} is more than 0.4 as control voltage V_{ctrl} hyper-0.45 V. However, the quality factor of A-MOS varactor is lower than 0.4 when the voltage difference between plus and minus ports hyper-0.2 is as shown at the bottom of Fig. 1. Therefore, the quality factor of the proposed E-AMOS is improved as compared to an ordinary A-MOS varactor mostly in the range of V_{ctrl}.

Figure 2(b) shows the C–V curve of the E-AMOS, a linear relation between capacitance and control voltage is obtained when V_{ctrl} shifts from 0.2 to 1.6 V. Consequently, the C–V curve linearization and improved quality factor of the proposed E-AMOS are achieved by adopting different capacitances of A-MOSs and setting unequal DC biases.

2.3. Proposed DSVA with high Q

A wide tuning range is achieved by switching capacitors in popular wide-band VCOs, the switched capacitors are fixed capacitors or varactors. MIM or MOM capacitors are chosen in a fixed capacitor structure[9] and a high quality factor is obtained. However, the resistor load is introduced by MOS switches, thus increasing the power of the VCO. Moreover, K_{VCO} varies greatly over different sub-bands in this structure. Varactors as switched capacitors have worse phase noise due to varactors with a lower quality factor than fixed capacitors and noise from MOS switches directly being modulated by varactors to phase noise. Hence, switched capacitor arrays with MIM capacitors are used for their low phase noise. Whereas, K_{VCO} compensation is needed to conquer the problem that K_{VCO} has a varies greatly over different sub-bands.

A DSVA is presented in Fig. 3(a), which has K_{VCO} compensation and retains the maximum quality factor of LC tank. The proposed DSVA has a two bit differential symmetrical configuration, An A-MOS varactor is connected to a MIM cap in series, the DC bias V_{B3} is connected to A-MOS plus port by resistor R_B. The plus–minus voltage difference of the A-MOS varactor is $V_{B3} - V_{ctrl}$ when MN1 is switched on and MN2 switched off, and the voltage difference of C_{var1} is $V_{B3} - V_{B4}$ as MN2 is switched on and MN1 switched off. Hence, the A-MOS varactor can be controlled in different states by switching MN1 and MN2 on and off. A conclusion is drawn from the character of the A-MOS varactor, as shown in Fig. 1(b). An A-MOS varactor has fixed minimal capacitance and a maximal quality factor in region I, the nearly linear C–V curve and moderate Q in region II, the fixed maximal capacitance and minimal quality factor in region III. As a result, the DSVA is set in region I on higher-frequency sub-bands, which as a fixed minimal capacitance with maximal Q avoids noise being modulated to phase noise by the A-MOS. Then the DSVA is biased in region II as a varactor to compensate VCO gain in lower frequency sub-bands.

3. Proposed VCO design

PMOS VCOs can obtain a lower phase noise than NMOS VCOs, owing to $1/f$ noise and the hot carrier effect of PMOS transistors being much less than NMOS transistors. In addition, the noise disturbances from the current source to the varactor through the use of a ground-referenced tank are minimized. The power-supply noise is suppressed well in PMOS VCOs with a top-biased current source[10]. Figure 4 shows the proposed LC-VCO schematic using a cross-coupled PMOS differential topology with a PMOS current source for better phase noise performance. A low-pass filter consists of R1 and MP5 to reject flicker and thermal noise from the bias circuit of I_{ref}. I_{ref} is programmable for optimizing phase noise and power over different sub-bands. The inductor L1 and a capacitor array are inserted as a noise filter to suppress the troublesome noise frequency at the second harmonic in the current source[11].

The tuning network is composed of the inductor L_0, and the proposed E-AMOS, DSCA and DSVA. A symmetric center-tap inductor L_0 is optimized according to power, phase

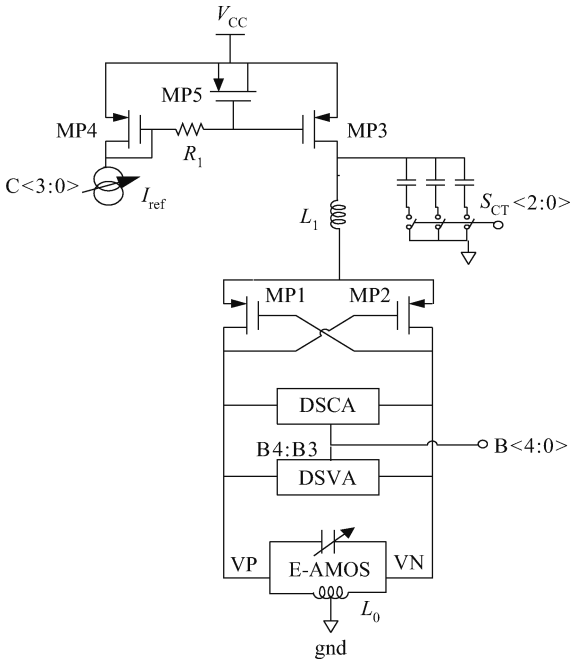

Fig. 4. Schematic of the proposed LC-VCO.

Table 1. Working mode of the proposed DSVA.

Group	Mode B4B3	Corresponding sub-bands
1	00	0–7
2	01	8–15
3	10	16–23
4	11	24-31

noise and tuning range, L_0 and E-AMOS compose the fine tuning mechanism. The DC bias V_{B1} of the E-AMOS is nearly 0 V, which are connected to differential output ports VP and VN. Also, V_{B2} is biased at 0.9 V, the DC offset $V_{B2} - V_{B1}$ is 0.9 V, which is an optimization for linear C–V curves and a higher-quality factor of E-AMOS. Coarse tuning is composed of a five bit DSCA and a two bit DSVA for a wide tuning range with K_{VCO} equalization over different sub-bands. The proposed DSCA is shown in Fig. 3(b), two symmetrical MIM caps C are controlled by switching MN1 on and off. In order to avoid floating DC of C, this degrades phase noise because MN1 works in the weak-inversion region. MN2 and MN3 support a DC bias to source and drain of MN1 when MN1 is switched on, the source and drain of MN1 are biased by MP2, MP3 when MN1 is switched off. MIM cap C and switch MN1 are binary-weighted structure for consecutive tuning in DSCA. For the sake of lessening the VCO gain variation within the whole operating range, the 32 DSCA sub-bands are divided into 4 sub-groups and each sub-group corresponds to a working mode of the proposed DSVA. For example, the sub-group which covers the sub-bands between 15 and 8 will correspond to the working mode 01. Then B3 controls the varactors connected to V_{ctrl}; they work in region II on the condition that $|V_{B3} - V_{ctrl}| < 0.8$ V; B4 controls the varactors working in region I and connected to V_{B4}, they equal high-Q fixed capacitors when $V_{B3} - V_{B4} < -0.8$ V. Consequently, the DC bias V_{B3} is 0.9 V, also V_{B4} is 1.8 V. A detailed configuration of DSVA to all sub-bands is listed in Table 1.

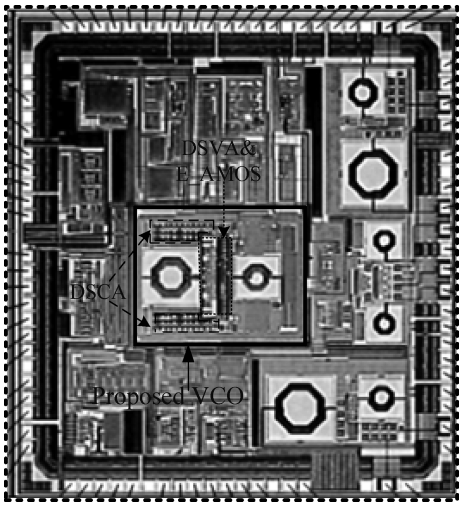

Fig. 5. Die microphotograph.

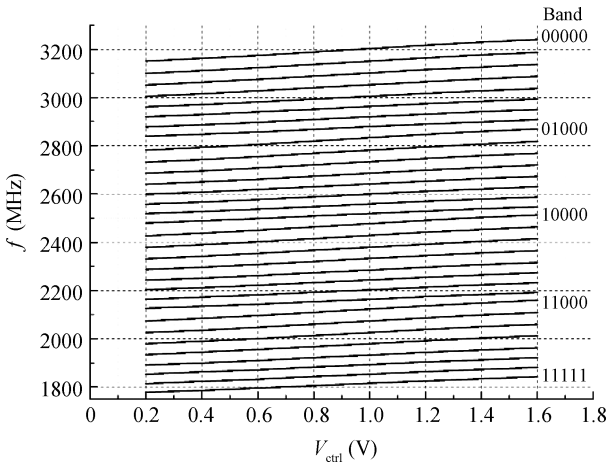

Fig. 6. Measured VCO f–V curve.

4. Measurement results

The proposed VCO was implemented in 0.18 μm one-poly six-metal CMOS technology. Figure 5 shows the chip microphotograph; the circuit occupies 900 × 653 μm^2. The frequency–voltage (f–V) curve is measured by altering control voltage V_{ctrl} and the sub-bands, which is shown in Fig. 6. The operation frequency from is 1.78 to 3.24 GHz, when V_{ctrl} is tuned in its effective range 0.2–1.6 V and sub-bands are changed from 31 to 0, the f–V curve is almost linear over the whole tuning range. VCO gain (K_{VCO}) varies ±21% over the entire sub-bands and effective tuned range of V_{ctrl}, which is shown in Fig. 7. Variation of K_{VCO} in the proposed circuit is much smaller than that in conventional oscillators. Over the entire tuning range, the circuit consumes 3 mA from a 1.8 V power supply.

Figure 8 shows that the measured phase noise is better than –122 dBc/Hz at a 1 MHz offset over different sub-bands. A performance comparison of the proposed VCO with a recently published LC-VCO is listed in Table 2. The figure of merit with

Table 2. Comparison of recently published LC-VCOs and this work.

Parameter	Ref. [13]	Ref. [14]	Ref. [15]	Ref. [16]	This work
Process (μm)	0.065	0.18	0.09	0.13	0.18
Supply voltage (V)	1.2	2	1.2	1	1.8
Center frequency (GHz)	12.8	1.79	3.3	5.28	2.51
Tuning range	31.3%	21.8%	46.2%	14	58.2%
Phase noise (dBc/Hz)	–116 @ 1 MHz	–128 @ 1 MHz	–156 @ 20 MHz	–132.8 @ 3 MHz	–122 @ 1 MHz
Power (mW)	22.5	7.2	22.8	1.4	5.4
FOM_T	194	191.2	201.5	198.4	197.6

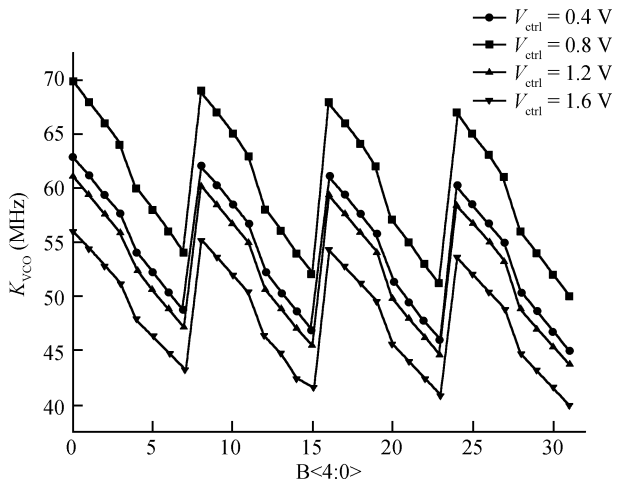

Fig. 7. Measured VCO gain variation.

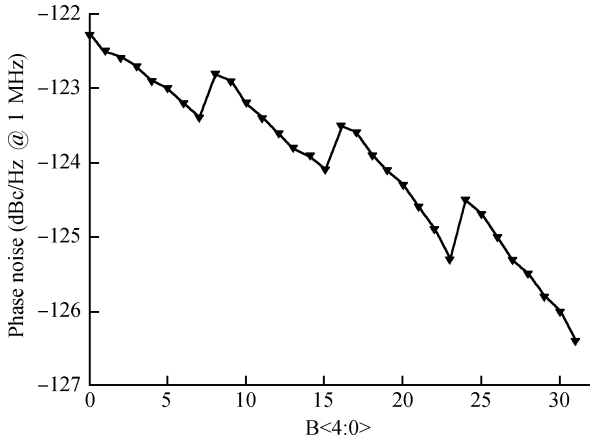

Fig. 8. Measured phase noise of the proposed VCO.

tuning range (FOM_T) is calculated as[12]

$$\begin{aligned} \mathrm{FOM_T} &= -L(\Delta\omega) + 20\lg(\omega_0/\Delta\omega) \\ &\quad - 10\lg(P/1\,\mathrm{mW}) + 20\lg(\mathrm{FTR}/10), \\ \mathrm{FTR} &= [(\omega_{\max} - \omega_{\min})/\omega_c] \times 100\%, \end{aligned} \tag{4}$$

where ω_0 is the VCO oscillation frequency, ω_{max}, ω_{min} are the maximal, minimal operation frequency, respectively, ω_c is the centre oscillation frequency, $L(\Delta\omega)$ is the measured phase noise at offset $\Delta\omega$, and P is the power consumption in mW.

5. Conclusion

In this paper, a K_{VCO} compensation LC-VCO using a high-quality factor varactor is presented. By using the E-AMOS, DSCA with DSVA compensation, a 58.2% tuning range is achieved and variation of VCO gain is close to $\pm$21% over the whole sub-bands and V_{ctrl}. The measured phase noise is lower than –122 dBc/Hz at a 1 MHz offset, which benefits from the improved Q of the varactors in the E-AMOS and DSVA. This proposed VCO has been successfully applied in high-sensitivity multi-mode GNSS receivers.

References

[1] Falletti E, Pini M, Presti L. Are C/N_0 algorithms equivalent in all situations. GNSS Solutions, Inside GNSS, 2010, 5(1): 20

[2] Razavi B. RF microelectronics. America: Pearson Education, 1998

[3] Tanabe A, Hijioka K, Nagase H, et al. A novel variable inductor using a bridge circuit and its application to a 5–20 GHz tunable LC-VCO. IEEE J Solid-State Circuits, 2011, 46(4): 883

[4] Long J R, Copeland M A. The modeling, characterization, and design of monolithic inductors for silicon RF IC's. IEEE J Solid-State Circuits, 1997, 32(3): 357

[5] Levantino S, Samori C, Bonfanti A, et al. Frequency dependence on bias current in 5-GHz CMOS VCOs: impact on tuning range and flicker noise upconversion. IEEE J Solid-State Circuits, 2002, 37(8): 1003

[6] Fong N W, Plouchart J O, Zamdmer N, et al. Design of wide-band CMOS VCO for multiband wireless LAN applications. IEEE J Solid-State Circuits, 2003, 38(8): 1333

[7] Soltanian B, Ainspan H, Rhee W, et al. An ultra-compact differentially tuned 6-GHz CMOS LC-VCO with dynamic common-mode feedback. IEEE J Solid-State Circuits, 2007, 42(8): 1635

[8] Song S S, Shin H. An RF model of the accumulation-mode MOS varactor valid in both accumulation and depletion regions. IEEE Trans Electron Devices, 2003, 50(9): 1997

[9] Berny A D, Niknejad A M, Meyer R G. A 1.8-GHz LC VCO with 1.3-GHz tuning range and digital amplitude calibration. IEEE J Solid-State Circuits, 2005, 40(4): 909

[10] Jerng A, Sodini C G. The impact of device type and sizing on phase noise mechanisms. IEEE J Solid-State Circuits, 2005, 40(2): 360

[11] Hegazi E, Sjöland H, Abidi A A. A filtering technique to lower LC oscillator phase noise. IEEE J Solid-State Circuits, 2001, 36(12): 1921

[12] Kim J, Plouchart J O, Zamdmer N, et al. A 44 GHz differentially tuned VCO with 4 GHz tuning range in 0.12 μm SOI CMOS. IEEE Int Solid-State Circuits Conf, Dig Tech Papers, 2005, 1: 416

[13] Deng Z M, Niknejad A M. A 4-port-inductor-based VCO coupling method for phase noise reduction. IEEE J Solid-State

Circuits, 2011, 46(8): 1772
[14] Li X Y, Shekhar S, Allstot D J. G_m-boosted common-gate LNA and differential Colpitts VCO/QVCO in 0.18-μmCMOS. IEEE J Solid-State Circuits, 2005, 40(12): 2609
[15] Andreani P, Kozmin K, Sandrup P, et al. A TX VCO for WCDMA/EDGE in 90 nm RF CMOS. IEEE J Solid-State Circuits, 2011, 46(7): 1618
[16] Mazzanti A, Andreani P. Class-C harmonic CMOS VCOs, with a general result on phase noise. IEEE J Solid-State Circuits, 2008, 43(12): 2716