A PNPN tunnel field-effect transistor with high-k gate and low-k fringe dielectrics*

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Abstract: A PNPN tunnel field effect transistor (TFET) with a high-k gate dielectric and a low-k fringe dielectric is introduced. The effects of the gate and fringe electric fields on the TFET's performance were investigated through two-dimensional simulations. The results showed that a high gate dielectric constant is preferable for enhancing the gate control over the channel, while a low fringe dielectric constant is useful to increase the band-to-band tunneling probability. The TFET device with the proposed structure has good switching characteristics, enhanced on-state current, and high process tolerance. It is suitable for low-power applications and could become a potential substitute in next-generation complementary metal–oxide–semiconductor technology.

Key words: TFET; subthreshold swing; high-k dielectric; low-k dielectric; fringe electric field
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1. Introduction

Since complementary metal–oxide–semiconductor (CMOS) technology has scaled down from the micrometer to the nanometer regime, power dissipation has become a serious problem in metal–oxide–semiconductor field-effect transistors (MOSFETs)[1]. One way to decrease the power dissipation is to reduce the subthreshold swing (SS), which means lowering the off-state current of the device for the same threshold voltage. However, it is well known that for conventional MOSFETs, SS has a theoretical limit of 60 mV/dec at room temperature due to these devices' inherent drift–diffusion mechanism[2]. One of the most promising approaches for overcoming this limitation is to introduce additional current-controlling mechanisms such as band-to-band tunneling (BTBT). Tunnel field-effect transistors (TFETs), based on the BTBT mechanism, have attracted extensive attention because their SS values can be below 60 mV/dec and short-channel effects (SCEs) are almost completely suppressed[3−5]. The PNPN TFET device is a MOS-gated $P^+P^-N^+$ diode with an ultrathin N^+ pocket region inserted between the P^+ source region and the P^- channel region, which is used to increase the tunneling probability[6−8]. In order to boost the on-state current (I_{on}) of TFET devices, high-k dielectrics such as HfO_2 and TiO_2 are proposed to reduce the equivalent oxide thickness (EOT) and enhance the gate control over the channel[9, 10]. In most previous studies, the gate dielectric was assigned to cover the whole device, including the source and drain regions[11, 12]. However, this configuration suffers from high capacitance, which has a detrimental effect on SS that will be covered later in this paper.

To analyze the influence of the fringe electric field induced by the gate in PNPN TFETs, a low-k dielectric was used as a fringe insulator and its performance was compared to that of a high-k dielectric. Previous simulation results demonstrated that the fringe electric field significantly affected the electrical behavior of double-gate PIN TFET devices[13], however, the physical relationship between the fringe electric field and the device performance was not clearly revealed. Based on these observations, a new double-gate PNPN TFET with high-k gate and low-k fringe dielectrics was developed. This device was shown to work effectively at low supply voltages with superior SS and I_{on} current characteristics compared to other PNPN TFETs, and it could have potential applications in next-generation CMOS technology.

2. Device structure and simulation

The device simulations were conducted with the Sentaurus Device simulator[14] using a dynamic nonlocal BTBT model that describes a physical picture of the real space carrier transport through the barrier. Electrons and holes are generated nonlocally at the end of the tunneling path, and the generation rate is obtained from nonlocal path integration. The dynamic nonlocal BTBT model provides a very complex BTBT probability expression, which is decided by the potential profile and the electric field. Furthermore, the BTBT rate can be reduced to Kane and Keldysh models in the uniform electric field limit[15]:

$$G_{\mathrm{BTBT}} = A\left(\frac{\xi}{\xi_0}\right)^P \exp\left(-\frac{B}{\xi}\right), \tag{1}$$

where ξ is the magnitude of the electric field, ξ_0 is 1 V/cm, and $P = 2.5$ for the indirect tunneling process. Parameters A and B are fitting coefficients, and they were obtained through the fitting with experimental Zener diode characteristics[16]. The Kane two-band dispersion relation was utilized due to silicon being an indirect bandgap material. A bandgap narrowing model and Fermi statistics were employed to take into account the effect of high doping concentration in the source and drain regions. The standard drift–diffusion carrier transport model

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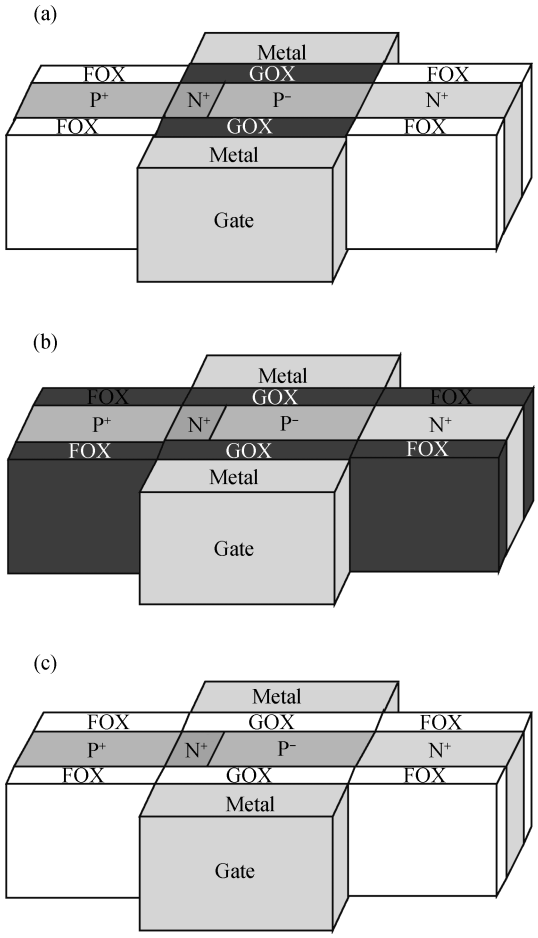

Fig. 1. Schematic diagram of the three PNPN TFETs. (a) HLK TFET with a high-k gate dielectric and a low-k fringe dielectric. (b) HK TFET with only a high-k dielectric. (c) LK TFET with only a low-k dielectric. HfO_2 is used for the high-k dielectric and SiO_2 is used for the low-k oxide.

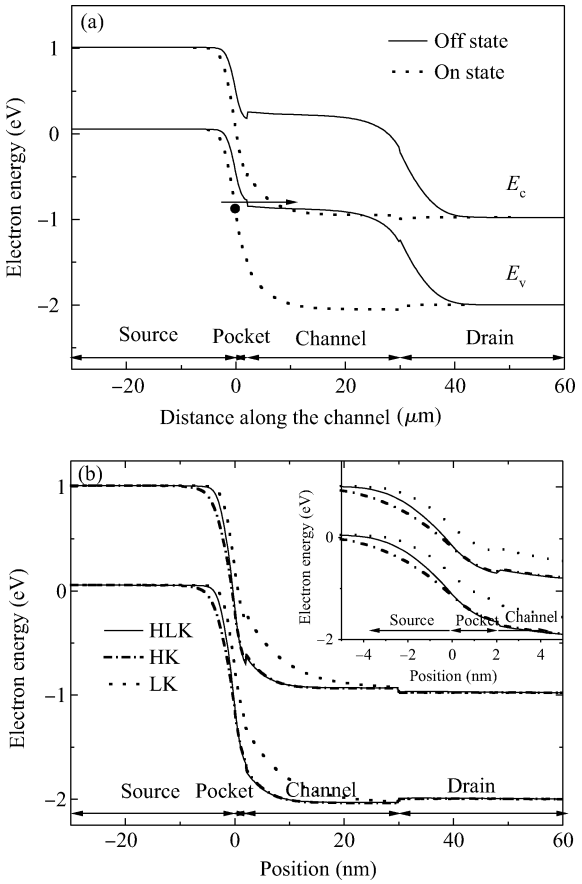

Fig. 2. (a) Simulated energy band diagram of the HLK TFET in the off-state and the on-state. (b) Simulated energy band diagram of the HLK TFET compared with the HK TFET and the LK TFET. The inserted picture displays the energy band of these three devices near source/channel junction.

and the Shockley–Read–Hall recombination model were also used.

A schematic diagram of our proposed PNPN TFET device is presented in Fig. 1(a). The device, known as the HLK TFET, has a double-gate structure that consists of a high-k dielectric (HfO_2) and a low-k dielectric (SiO_2) covering the gate region and the fringe source/drain regions, respectively. Figures 1(b) and 1(c) show devices that are completely covered with a high-k dielectric (HfO_2) and a low-k dielectric (SiO_2), respectively; these devices are referred to as HK and LK TFETs, respectively. In the simulations, all the HLK, HK, and LK TFET devices are 90 nm long; the channel, source, and drain regions are each 30 nm long. The physical thickness of the HfO_2 gate dielectric is 3 nm and its dielectric constant is 22, while the silicon film is 10 nm thick. The source and drain regions are heavily boron-doped (10^{20} cm^{-3}) and phosphorous-doped (10^{19} cm^{-3}), respectively. This asymmetrical doping profile between the source and drain regions is commonly used for reducing ambipolar effects. The channel region is lightly boron-doped (10^{17} cm^{-3}), and an ultrathin fully depleted N^+ pocket layer (10^{20} cm^{-3}) inserted between the source and channel region is used to decrease the tunneling barrier width and increase the lateral electric field. All the doping junctions are assumed to be abrupt in order to improve device performance.

Figure 2(a) shows the energy band diagram of our proposed HLK TFET. Since the operation of PNPN TFETs is based on the BTBT mechanism, the N^+ drain region is always biased with positive voltage for n-type devices and the P^+ source region is set at zero voltage. The gate voltage can vary from 0 to 1 V; when it is 0 V, the TFET is in the off-state (solid lines in Fig. 2(a)) because the source-to-channel PN junction is reverse-biased and BTBT is forbidden. The energy band in the channel is pushed down when positive gate voltage is applied. Once the conduction band (E_c) in the channel region is lower than the valence band (E_v) in the source region, the device turns on (dotted lines in Fig. 2(a)); in this situation, significant electron tunneling occurs from E_v in the source region to E_c in the channel region. Figure 2(b) shows the energy band diagram of HLK, HK and LK TFETs. It can be observed that the energy band of HLK TFET follows that of LK TFET in the source region, and follows the trend of HK TFET in the channel region.

In general, the tunneling current can be expressed as follows[17]:

$$I = \int F_{s,V}(E)[1 - F_{c,C}(E)]N_V(E)N_C(E)T_{tunnel}dE, \quad (2)$$

where N_v and N_c are the effective densities of states in the

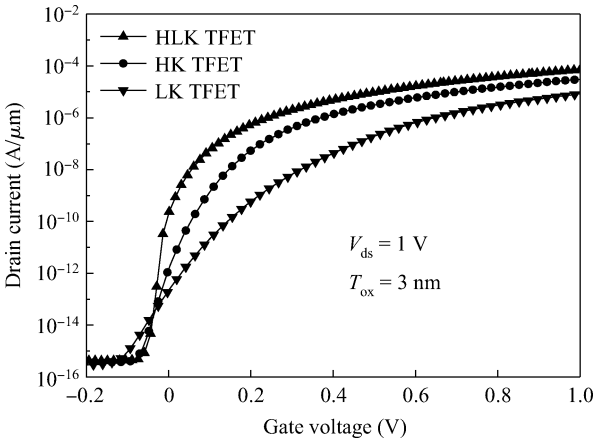

Fig. 3. Transfer characteristics of HLK, HK, and LK TFETs when V_{ds} = 1 V.

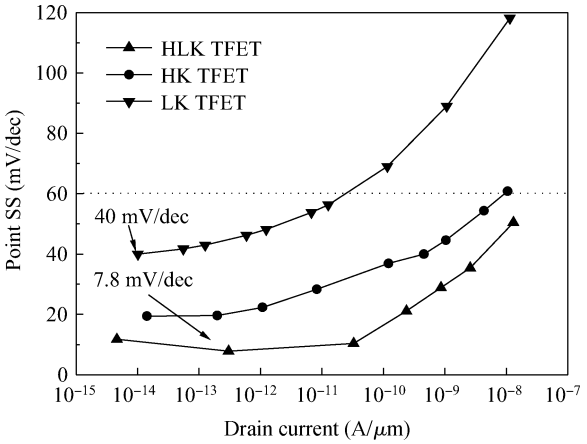

Fig. 4. Point SS versus drain current for HLK, HK, and LK TFETs while V_{ds} = 1 V.

valence and the conduction band, respectively; F_c and F_s are the Fermi–Dirac distribution functions in the channel and the source region, respectively; and T_{tunnel} is the tunneling probability. It is important to note that the tunneling current is decided not only by the tunneling barrier width but also by the availability of occupation states in the source region and vacant states in the channel region. Therefore, one effective approach for boosting the tunneling current is to increase the number of available states.

3. Results and discussion

3.1. PNPN TFET with a high-*k* gate dielectric and a low-*k* fringe dielectric

In order to investigate the transfer behavior of the HLK, HK, and LK TFETs, the transfer curves among these devices were compared when V_{ds} = 1 V. From Fig. 3, it is clear that the curves of these devices are similar: when V_{gs} reaches the turn-on voltage, the BTBT mechanism dominates and the drain current increases significantly and becomes saturated in the high gate voltage. These curves differ mainly in terms of threshold voltage and on-state current. To describe the relationship between SS and drain current, the point SS values of these three structures were extracted from the transfer characteristics in Fig. 3 with drain current varying from 1 fA/μm to 0.1 μA/μm. Point SS is defined as the slope of different points of the transfer curves, and the I_{on} current is defined as the drain current when $V_{gs} = V_{ds}$ = 1 V.

Consistent with the results of previous studies[12], the HK TFET had a superior I_{on} current and SS compared to the LK TFET (as shown in Figs. 3 and 4, respectively). This is because the HK TFET has a smaller EOT compared to the LK TFET even though the physical thickness of the gate oxide is the same for both devices, leading to an increase in gate control over the channel. Overall, the HLK TFET achieved the best performance of the three devices; its I_{on} current reached 71.4 μA/μm, which was higher than both the HK and LK TFETs (Fig. 3), and its minimum point SS value was 7.8 mV/dec, which was almost 1/5 of that of the LK TFET (Fig. 4). The I_{on}/I_{off} ratio of the HLK TFET was 10^{11} at 1 V supply voltage, which was the highest of the three devices.

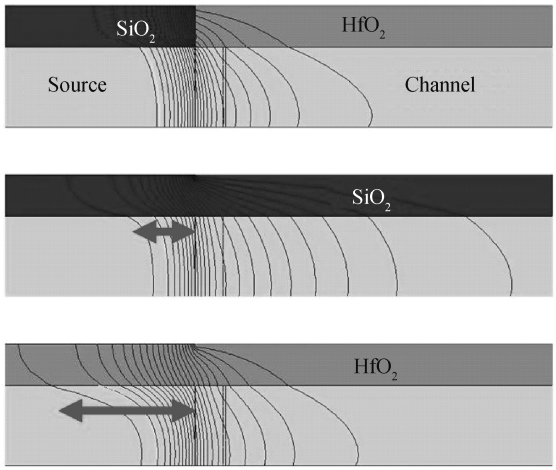

Fig. 5. Electrical potential contours of the HLK (top), LK (middle), and HK (bottom) TFETs biased at $V_{gs} = V_{ds}$ = 1 V.

As shown in Fig. 4, point SS increased as drain current increased for all TFETs. For the LK TFET, the values of point SS were below 60 mV/dec over only three decades of drain current; for the HLK TFET, they were below 50 mV/dec over almost seven decades of drain current. Furthermore, the values of point SS of the HLK TFET were lower than those of the LK and HK TFETs over the entire range. These results suggest that the use of a low-*k* fringe dielectric resulted in better gate coupling which decreased the subthreshold slope and enhanced the on-state current.

Figure 5 shows the electrical potential contours of the three TFETs. The tunneling distance of the HLK TFET is shorter than the others because its source depletion width is the smallest of the three devices. When positive gate voltage is applied, the gate pushes down the energy band in the channel region, leading to an increase of the equivalent density of vacant states. However, in the HK TFET, the source region can also be influenced by the positive gate voltage due to the induced fringe electrical field; the holes are excluded by the gate, and the equivalent density of the occupation states in the source region decreases, resulting in a lower on-state current compared to the HLK TFET. This finding is illustrated further in Fig. 6,

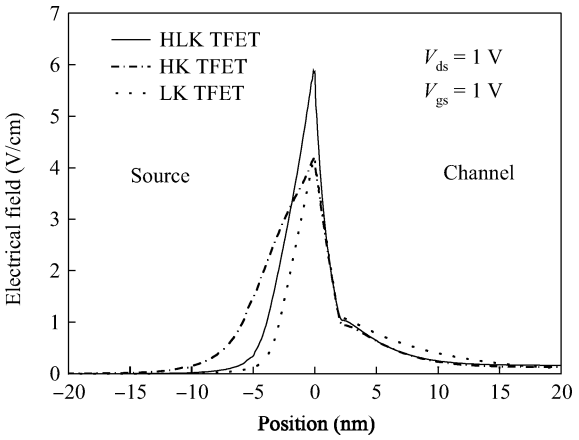

Fig. 6. Lateral electric field across the tunneling source-channel junction biased at $V_{gs} = V_{ds} = 1$ V.

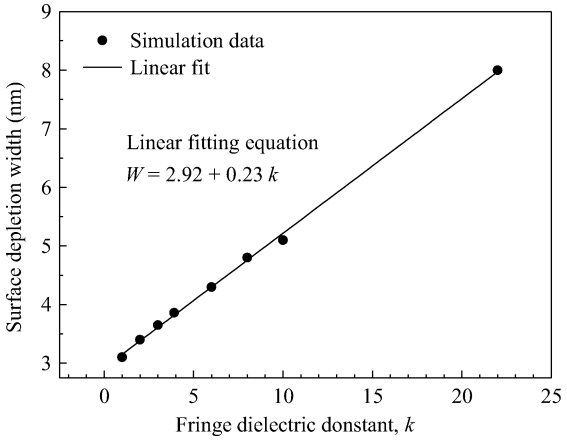

Fig. 8. Quantitative relationship between fringe dielectric constant and surface depletion width.

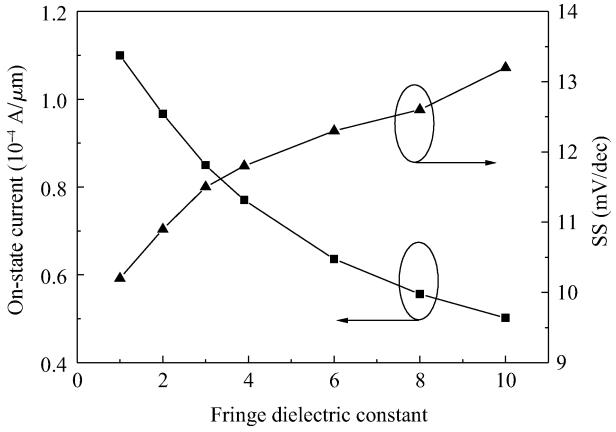

Fig. 7. Impact of varying the k value of the fringe dielectric on the I_{on} and SS of the HLK TFET.

in which the lateral electric field near the source and channel interface is presented. As described in Eq. (1), in the BTBT tunneling model, a stronger electric field implies a greater tunneling probability. As shown in Fig. 6, the maximum electric field of the HLK TFET is about 1.5 times greater than that of the HK and the LK TFETs. Therefore, it can be concluded that the HLK TFET has the highest on-state current of the three devices, which is consistent with the results shown in Fig. 3.

3.2. Influence of the fringe dielectric constant

The impact of the fringe electric field on the device performance of the HLK TFET was examined by varying the k value of the fringe dielectric while keeping the gate oxide unchanged. Figure 7 shows the effect of varying the fringe dielectric constant on the I_{on} current and the SS. It can be observed that the I_{on} current increased and the SS decreased as the fringe dielectric constant decreased. In other words, an increase in the k value of the fringe dielectric led to a corresponding degradation of the device performance of the HLK TFET in terms of both the I_{on} current and the SS.

In other words, the enlarged fringe electric field resulted in a decrease of the I_{on} in the PNPN TFETs due to the extension of surface depletion in the source region. Figure 8 shows the quantitative relationship between fringe dielectric constant and surface depletion width. The surface depletion width increased from 3 to 8 nm as the fringe dielectric constant increased from 1 to 22. In general, surface potential is related to gate voltage, source doping concentration, fringe dielectric thickness, and fringe dielectric permittivity. However, in this case, the other parameters were kept unchanged, so surface depletion width was determined only by fringe dielectric permittivity.

$$W_{\text{surface}}\left(k, T, V_g, N_A\right) = W_{\text{surface}}\left(k\right). \tag{3}$$

We can expand the equation for surface depletion width as follows:

$$W_{\text{surface}}(k) \approx W_0 + \frac{\partial W}{\partial k}k. \tag{4}$$

W_0 is constant when the fringe dielectric constant is set at zero, and it can be calculated as the bulk depletion width in the center of the silicon film. As shown in Fig. 8, bulk depletion width in the source region of the HLK TFET was about 3 nm when $V_{gs} = V_{ds} = 1$ V, which is consistent with the fitted data in Fig. 8; the value of the first derivative coefficient is approximately 0.23. Thus, the surface depletion width in the source region is a linear function of the fringe dielectric constant:

$$W_{\text{surface}}\left(k\right) \approx 2.92 + 0.23k. \tag{5}$$

3.3. Influence of the gate dielectric

In order to investigate the impact of the gate electric field in the channel region, the HLK TFET was also simulated with different k values of the gate dielectric by keeping its physical thickness constant. SiO_2 was used as the fringe dielectric, and the other parameters remained the same. In the simulations, the k values were 9, 50, 100, and 200, corresponding to Al_2O_3, $BiFeO_3$, TiO_2, and $SrTiO_3$, respectively. It is well known that a higher dielectric constant implies a smaller EOT, resulting in an increased surface electric field under the gate and a greater tunneling probability. Figure 9 illustrates minimum SS and I_{on} current as a function of gate dielectric constant. As the k value of the gate dielectric increased from 3.9 to 200, the SS decreased from 40 to 5 mV/dec, and the I_{on} current increased from 10 to 160 μA/μm. These results indicate that

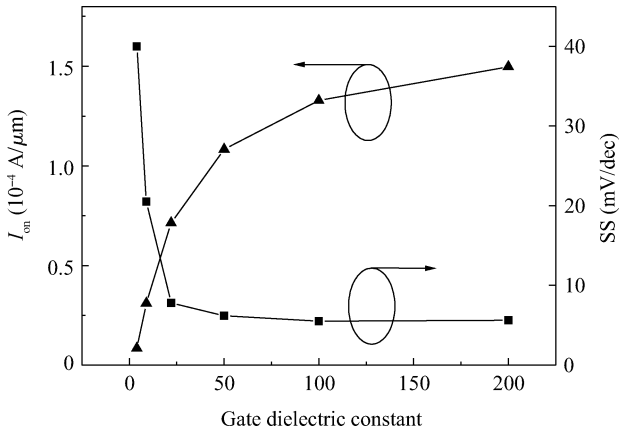

Fig. 9. Impact of varying the k value of the gate dielectric on the I_{on} and SS of the HLK TFET while $V_{ds} = 1$ V.

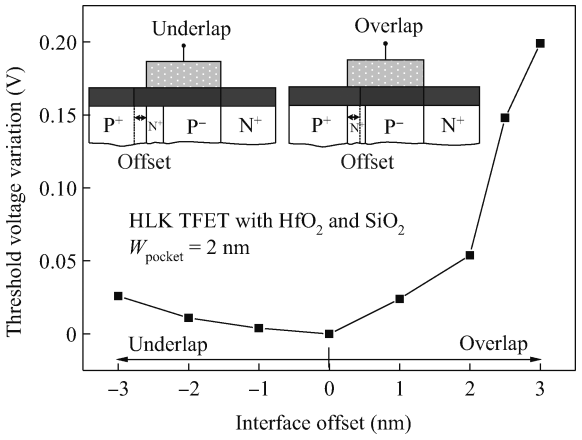

Fig. 11. Threshold voltage variation versus gate and fringe dielectric interface offset.

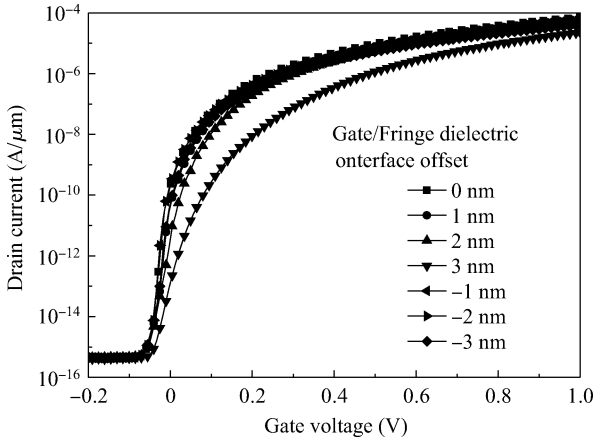

Fig. 10. Sensitivity of the proposed HLK TFET's performance on the gate dielectric and fringe oxide interface offset while $V_{ds} = 1$ V.

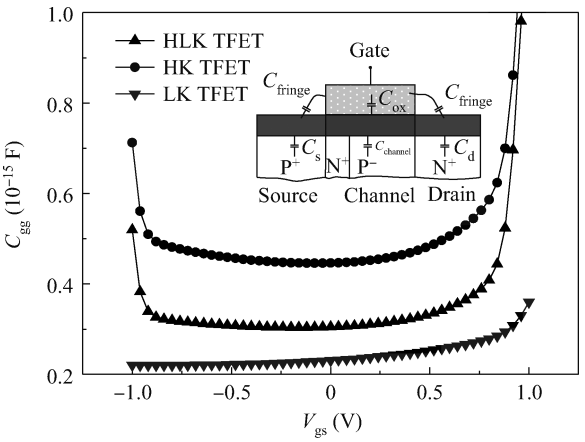

Fig. 12. Capacitance–voltage characteristics showing gate–gate C_{gg} capacitance as a function of gate–source voltage V_{gs} for the HLK, HK, and LK TFETs.

device performance of the HLK TFET was improved by using a higher gate dielectric constant while keeping its physical thickness unchanged.

3.4. Process tolerance

Since the thickness of the N+ pocket region was designed to be 2 nm in the HLK TFET, the interface of the HfO_2 and the SiO_2 might not be on the exact edge of the gate in practice. Accordingly, the sensitivity of the HLK TFET's performance on the gate and fringe oxide interface offset was investigated. In the simulations, the gate and fringe dielectric interface was assigned to move from –3 to 3 nm, corresponding to the cases of gate–source overlap and gate–source underlap, respectively. Figure 10 shows the impact of gate position with respect to the tunneling junction on the transfer characteristics of the HLK TFET. Gate threshold voltage was extracted at 10^{-7} A/μm. The threshold voltage shifted less than 25 mV when the interface offset was below 1 nm. However, the threshold voltage increased by 50 mV while the offset exceeded 2 nm (Fig. 11). This demonstrates that if the high-k dielectric film overlaps the source, the SS is similar to that of the HK TFET. On the other hand, when the low-k oxide fully overlaps the N+ pocket, the tunneling region is controlled by the low-k oxide, and the SS is similar to that of the LK TFET. Therefore, it is clear that accurate gate alignment is critical.

3.5. AC characteristics

The capacitance characteristics of TFET devices are one of the most important factors that affect device performance because they determine the on-state current and the delay of TFET-based inverters[18, 19]. In general, previous studies examining capacitance properties have focused on the impact of the device structure itself. In this paper, since the structure of the TFET device is a double-gate structure and the only difference is the effect of different gate and fringe dielectrics, gate–gate capacitance C_{gg} was investigated. As shown in Fig. 12, the C_{gg} of the HK TFET was greater than that of the HLK and the LK TFETs, corresponding to their average equivalent dielectric constants.

4. Conclusions

In summary, we have analyzed the influence of gate and fringe dielectrics in PNPN TFETs through various numerical simulations, which demonstrated that these dielectrics play dif-

ferent roles in terms of affecting device characteristics. A high gate electric field is useful for increasing BTBT probability, while a low fringe electric field is required to boost the on-state current. In addition, it was shown that surface depletion width in the source region increases linearly with fringe dielectric permittivity, which led to an enlarged tunneling path. The PNPN TFET utilizing a high-k gate dielectric and a low-k fringe dielectric demonstrated superior performance with a lower SS and a higher I_{on}/I_{off} ratio compared with its counterpart TFETs. Moreover, this novel device was shown to have a wide range of process tolerance. Therefore, the HLK TFET is suitable for future low-power applications and could have potential uses in next-generation CMOS technology.

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