A novel high performance ESD power clamp circuit with a small area*

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Abstract: A MOSFET-based electrostatic discharge (ESD) power clamp circuit with only a 10 ns RC time constant for a 0.18-μm process is proposed. A diode-connected NMOSFET is used to maintain a long delay time and save area. The special structure overcomes other shortcomings in this clamp circuit. Under fast power-up events, the gate voltage of the clamp MOSFET does not rise as quickly as under ESD events, the special structure can keep the clamp MOSFET thoroughly off. Under a falsely triggered event, the special structure can turn off the clamp MOSFET in a short time. The clamp circuit can also reject the power supply noise effectively. Simulation results show that the clamp circuit avoids fast false triggering events such as a 30 ns/1.8 V power-up, maintains a 1.2 μs delay time and a 2.14 μs turn-off time, and reduces to about 70% of the RC time constant. It is believed that the proposed clamp circuit can be widely used in high-speed integrated circuits.

Key words: electrostatic discharge; clamp circuit; false triggering; turn-off mechanism
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1. Introduction

Electrostatic discharge (ESD) has been acknowledged as the most urgent task on the product reliability of CMOS integrated circuits. Almost 70% of IC (integrated circuit) failures are caused by ESD and associated EOS (electrical over stress)[1]. With the scaling down of the feature size of CMOS technology, the thin gate oxide and shallow junction bring more issues in the design of ESD protection circuits. The whole chip ESD protection should contain a power supply ESD clamp circuit to prevent the thermoelectric breakdown in the internal circuit of ICs[2]. Up to now, although there has been much research on new ESD protection, the structures of novel ESD protection are very few.

The clamp circuit based on MOSFET with a triggering circuit has three crucial advantages: no extra process steps, relaxed layout constraints and easy EDA simulation[3]. In this paper, a novel MOSFET-based RC triggering ESD power clamp circuit is presented, which adopts a special structure to avoid the false triggering effectively, maintain enough delay time, allow a turn-off mechanism, and save layout area. The delay time is one of the most important parameters in a clamp circuit. The triggering circuit should turn on the clamp MOSFET and keep it "on" during the whole ESD event so that the clamp circuit can discharge the ESD energy (up to 500 ns to 1 μs for Human body model[3]). At the same time, it should be guaranteed that the clamp MOSFET is turned "off" under normal operating conditions.

2. Operation of transient ESD clamps

One of the first RC triggering active clamp circuits was proposed by Merrill *et al.*[4]. As shown in Fig. 1, the overall structure of a general clamp circuit consists of three parts: the clamp device, the delay element and the detect element. The clamp device is a very large MOSFET. The detect element is used to detect the ESD event and send a signal to the back-end circuits. The rise time of an ESD event is usually between 100 ps and 60 ns[3], whereas the rise time of a normal power-up event is in the millisecond range. Therefore, the detect element can be implemented with an RC network of which the RC time constant is set to the order of μs. The ESD event can be easily distinguished from the normal power-up events. Nevertheless, for some special applications, such as "Hot Plug" operations or switching networks, or controlling sleep power mode in the low-power and high-performance microprocessors, the fast rise time is usually shorter than a microsecond or is even in the order of hundreds of nanoseconds[3]. Thus, the clamp circuit might be triggered under normal operating conditions, which is regarded as false triggering.

Figure 2 shows the classic RC triggered clamp circuit. In this circuit the detect element is the RC network and the "CLK"

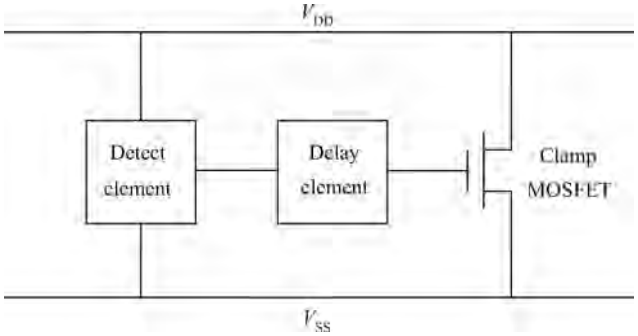

Fig. 1. Overall structure of the general clamp circuit.

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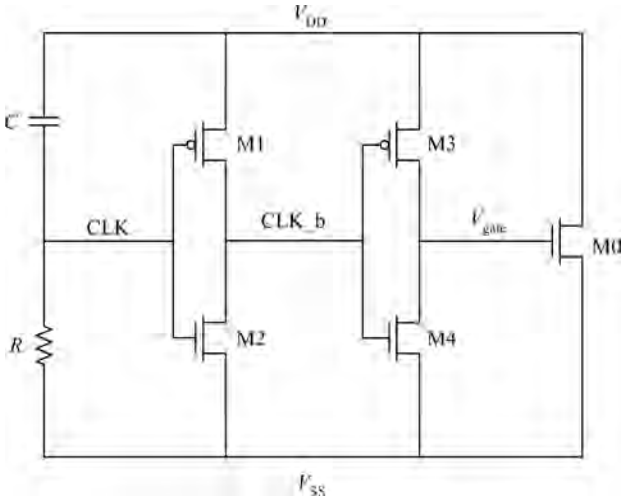

Fig. 2. Schematic of the classic clamp circuit.

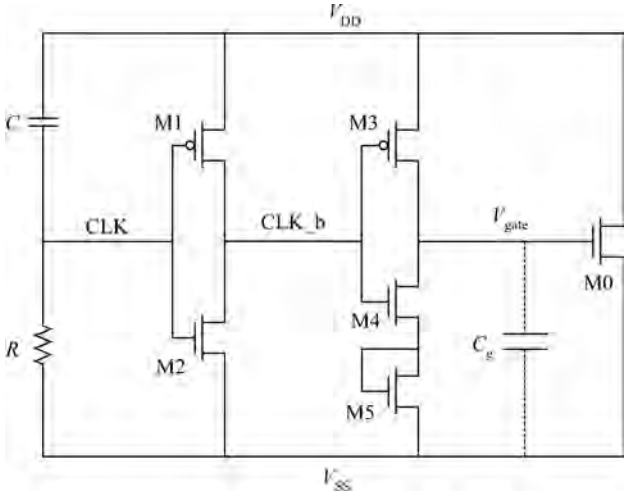

Fig. 3. Schematic of clamp circuit with delay element.

signal is the detect result. However, the RC network also accomplishes a delay function, because the large RC time constant can guarantee that the "CLK" keeps "1" for a long time, the clamp MOSFET can be turned on for a long time to discharge the ESD energy. The two inverters are used to recover the voltage. It is evident that this circuit needs a very large layout area to put the resistor and capacitor. On the other hand, the clamp circuit with a large RC constant is more easily false triggered, and the clamp MOSFET is turned on and the energy is consumed.

3. Design of the novel ESD clamp circuit

3.1. Design of the delay element

Clamp circuits with a feedback network are thoroughly investigated[5−10]. The feedback network can hold on V_{gate} for a long time so the RC time constant is reduced substantially. If the clamp circuit is falsely triggered for any reason, the clamp MOSFET can be turned off by the difference in the leakage current of the transistors[6]. This means that the clamp circuit allows the turn-off mechanism. The clamp circuit with flip-flop[11] has a similar turn-off mechanism. However, the turn-off time is about 200 μs[11], which is so long that much extra energy may be leaked. Moreover, the turn-off time under this turn-off mechanism varies sharply with temperature[6].

Another valuable method to implement a delay element is presented in Ref. [12]. The gate voltage of the clamp MOSFET is charged to "1" under the ESD event, and the gate parasitic capacitance stores quantities of charges. So, a resistor as large as 45 kΩ is added between the source of M4 and V_{SS}, V_{gate} falls at a slow rate, and the delay time becomes longer. In this paper, we use M5 to replace the resistor in order to save the layout area as shown in Fig. 3. C_g is the gate parasitic capacitance of M0. When the ESD event comes, M2 pulls "CLK_b" to V_{SS}, M4 is turned off and M3 charges C_g to V_{DD}, then M0 is turned on. After the ESD power-up pulse, "CLK" gradually goes back to 0 and "CLK_b" rises to "1". Then M3 is turned off, and the charges on C_g discharge to V_{SS} through M4 and M5. Since M5 is diode-connected, the V_{gs} of M5 decreases in the discharge procedure, so the equivalent resistance of M5 increases, V_{gate} falls more and more slowly, and the clamp MOSFET has enough time to discharge the ESD energy.

3.2. Design of the detect element

In the classic RC based clamp circuit, since the RC network is not only used as the detect element but also the delay element, the RC constant is very large. However, in the circuit which has a separate delay element, the RC network only needs to detect the ESD event. When the ESD event occurs, "CLK" rises to V_{DD}, the detect element sends this triggering signal to back-end circuit. Then M3 is turned on to charge C_g and drives the M0. Once C_g is fully charged, M3 does not need to keep conducting, and "CLK" can go back to 0. In other words, the task of the RC network is only to turn on M3 and fully charge C_g. So the RC constant is reduced to a small value (10 ns).

3.3. Problems of the proposed delay element

In order to obtain a long enough delay time (∼0.5–1 μs), a small W/L ratio of M4 and M5 should be designed to obtain a large equivalent resistance. However, this design will cause a coupling problem. Because the large R_{M45} (the conducting resistance of M4 and M5) enhances the coupling effect of M0 under the power-up event, the circuit may be false triggered more easily. It is therefore necessary to understand the coupling effect of M0. This issue is also mentioned in Ref. [13], where it is observed that V_{gate} reaches $0.34V_{DD}$ at first.

Figure 4 shows the equivalent circuit of a delay element under a fast power up event. C_{gd}, C_{gs}, and C_{gb} are gate-to-drain, gate-to-source, and gate-to-body parasitic capacitances of M0 respectively. When the false triggering pulse comes, V_{gate} rises and forms the voltage peak due to a coupling effect. Figure 5 shows the voltage peak of V_{gate} when V_{DD} rises from 0 to 1.8 V within 300 ns (300 ns/1.8 V). V_{gate} reaches approximately 0.6 V at first. Then, R_{M45} discharges the induced charges on V_{gate}. Finally V_{gate} is pulled down to V_{SS}. The voltage peak can turn on M0 when the false triggering happens. It may be regarded as "sub_mistriggering". The above phenomenon appears when the rise time of V_{DD} is shorter than 600 ns.

It should be noted that the voltage peak has no relationship with M3.The false triggering pulse is not strong enough to turn

Table 1. Function of special structure.

Event	Function of special structure
ESD	Does not affect the discharge
False triggering	Avoids false triggering
Power supply noise	Rejects power supply noise
Normal operation	Thoroughly turns off the clamp MOSFET

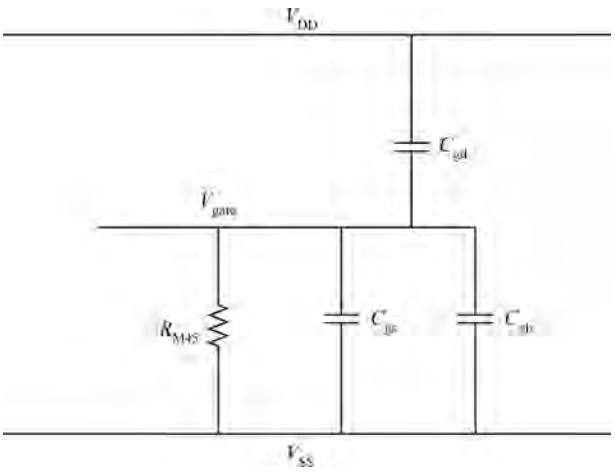

Fig. 4. Equivalent circuit of coupling effect of M0.

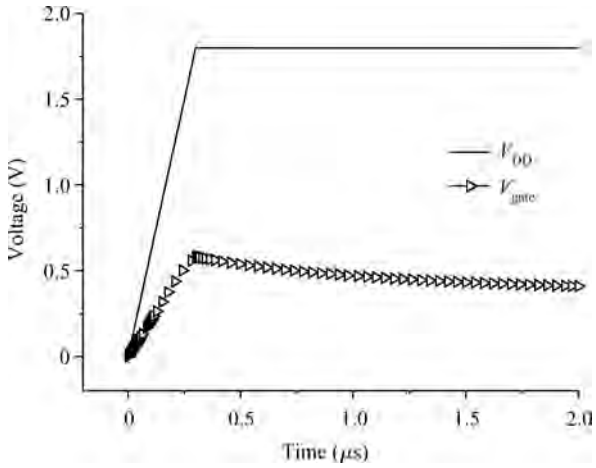

Fig. 5. The voltage peak caused by coupling.

on M3. In fact, the large R_{M45} can be treated as infinity initially. V_{gate} is pulled up due to the coupling effect.

Furthermore, since M5 is diode-connected, under normal operating conditions, V_{gate} cannot be thoroughly pulled to V_{SS} ($\sim$170 mV), and M0 may leak energy. The large R_{M45} makes the clamp circuit more sensitive to the power supply noise. So, a special structure is added to the clamp circuit to solve these problems in the following section of this paper.

3.4. Special structure

A special structure is presented to improve the delay element, and the schematic of the novel clamp circuit is shown in Fig. 6. The function of the special structure is shown in Table 1.

The special structure consists of D1, M6, M7 and M8. D1 is a diode. Here the anode of D1 should be connected with V_{gate},

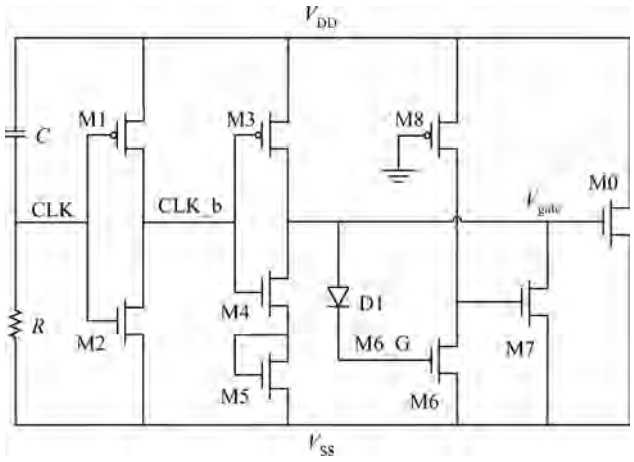

Fig. 6. Schematic of the novel clamp circuit with special structure.

and the cathode should be connected with "M6_G". M8 is a gate grounded PMOS, and the W/L ratio of M8 is five times smaller than that of M6. When the ESD event comes, M3 is turned on and V_{gate} is charged to V_{DD} quickly. The potential of "M6_G" keeps lower than V_{gate} for a diode conducting voltage in the ESD procedure, so the potential of "M6_G" is high enough to turn on M6. M7 is thoroughly turned off, and the special structure does not affect the clamp circuit. M0 can be normally turned on during the ESD procedure.

It should be mentioned that "M6_G" keeps a certain potential even when V_{gate} gradually falls to 0. Because of the very small leakage current, the charges on "M6_G" are finally leaked over a long time period. This makes sure that the special structure does not affect the clamp circuit in the whole ESD event. Figure 7(a) shows the waveforms of V_{gate} and "M6_G" under an ESD event. We can see that "M6_G" keeps a high potential for a long time and falls very slowly. Actually, it takes about 5 ms to fall to 0. It makes sure that M6 is fully turned on and V_{gate} does not be pulled down by M7.

However, a false triggering pulse has a much weaker impact on V_{gate} than the ESD event does. As D1 cannot be conducted, V_{gate} cannot charge "M6_G" to the high potential. As shown in Fig. 7(b), under a 100 ns/1.8 V power up event, "M6_G" is initially pulled up to about 0.2 V due to the coupling effect, which is similar with the coupling of V_{gate}. So, M6 is turned off, and M7 is turned on by M8. V_{gate} is quickly pulled down to V_{SS} by M7 after a very small peak. This process occurs in a very short time and M0 is not turned on. "M6_G" still falls very slowly.

If the clamp circuit is triggered by any factor under the normal operating conditions, V_{gate} will be finally pulled down to V_{SS} by M7. As mentioned earlier, M5 cannot thoroughly pull V_{gate} down to V_{SS}, but it can pull V_{gate} down to a low voltage, and "M6_G" decreases. M6 is gradually turned off, and M7 is gradually turned on. Finally M7 pulls V_{gate} down to V_{SS}. Figure 7(c) shows the waveform of V_{gate} under this condition. We can see that V_{gate} initially rises to 1.8 V (V_{DD}), but it is gradually pulled down by M4 and M5. Finally it is thoroughly pulled down to 0 after 2.14 μs by M7. Compared with previous circuits, this turn-off time is very short, and much energy is saved.

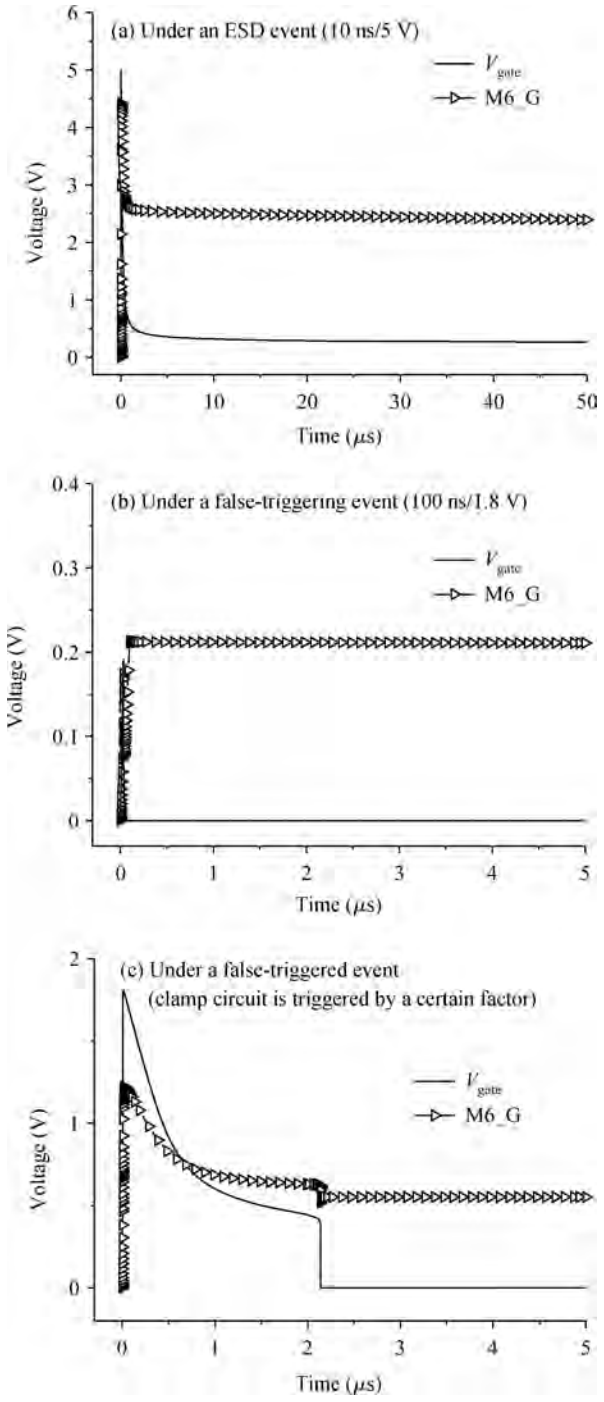

Fig. 7. Waveforms of V_{gate} and M6_G under different events.

3.5. Optimization of the novel ESD power clamp circuit

It is necessary to optimize the design in order to obtain the best performance with the lowest cost. The W/L ratio of M3 should be designed to be large to a certain extent so that V_{gate} can be fully pulled up when the ESD event comes. The W/L ratios of M4 and M5 should be small enough to obtain a long delay time. Furthermore, the W/L ratio of M8 should be small, then the gate voltage of M7 will rise slowly, and M7 cannot be turned on during the ESD process.

The W/L ratio of M0 is another crucial parameter in the clamp circuit, which is directly proportional to the discharge ability. Small W/L saves more of the layout area and more energy, whereas large W/L is better for the discharge performance. There is a trade-off between the two factors, and the two factors should be balanced carefully. In this paper, we choose the W/L of M0 to satisfy 2 kV HBM.

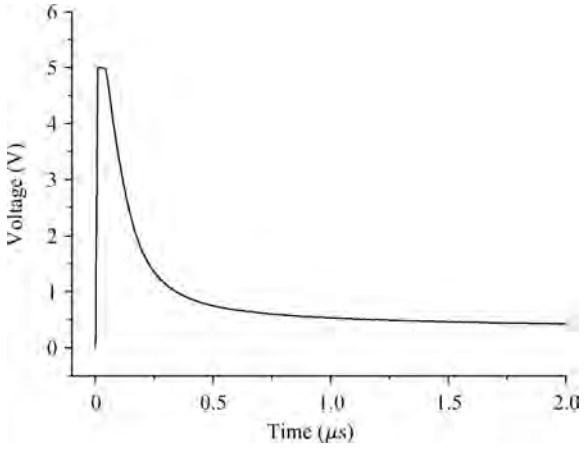

Fig. 8. Waveform of V_{gate} under the ESD event.

For a 2 kV ESD stress, $V_{esd} = 2$ kV, R_{esd} (1.5 kΩ) is the equivalent resistance of a human body. Assuming the fully conducting resistance of M0 ($V_{gs} = V_{ds} = V_{DD}$) is R_{dson}, one can obtain

$$V_{DD} = \frac{R_{dson}}{R_{esd} + R_{dson}} V_{esd} = \frac{R_{dson}}{1500 + R_{dson}} \times 2000. \quad (1)$$

The gate-oxide breakdown voltage of transistors in 0.18 μm CMOS technology under a 100 ns voltage pulse is around 8 V[14]. We design the upper limitation of V_{DD} as 6 V to allow enough of a margin. Equation (1) can be rewritten as follows:

$$6 \geqslant \frac{R_{dson}}{R_{esd} + R_{dson}} V_{esd} = \frac{R_{dson}}{1500 + R_{dson}} \times 2000. \quad (2)$$

By solving Eq. (2), one can obtain:

$$R_{dson} \leqslant 4.5\,\Omega. \quad (3)$$

So, the final W/L ratio of M0 can be easily determined. Here the width of M0 is 400 μm.

4. Characteristic simulation

The novel clamp circuit is simulated based on a 1.8 V 0.18 μm CMOS process. The RC time constant is set to 10 ns, $R = 10$ kΩ, $C = 1$ pF, and the width of M0 is set to 400 μm.

4.1. Voltage characteristic

A power-up event of VDD rising from 0 to 5 V within10 ns (10 ns/5 V) is adopted to simulate an ESD event, the waveform of V_{gate} is shown in Fig. 8. Since the threshold voltage of 0.18-μm CMOS MOSFET is about 0.5 V, the gate voltage of clamp MOSFET keeps "on" for 1.2 μs, which is long enough to discharge the ESD energy.

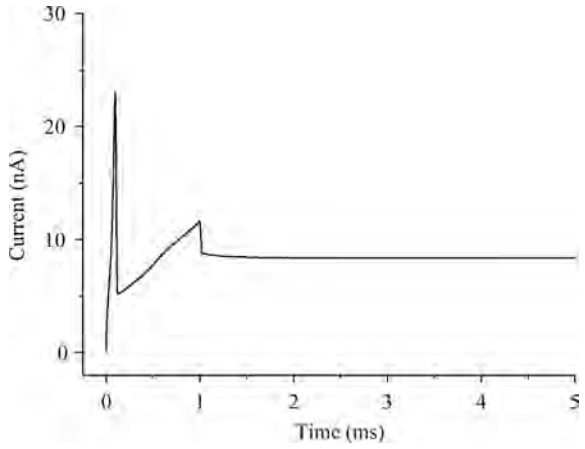

Fig. 9. Waveform of leakage current under the normal operating conditions.

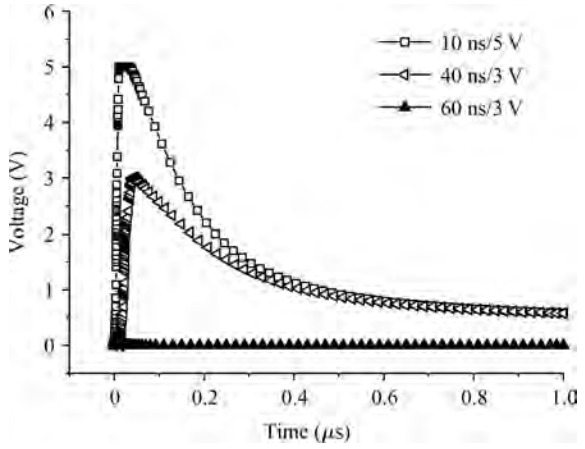

Fig. 10. Waveforms of V_{gate} under different conditions (10 ns/5 V, 40 ns/3 V and 60 ns/3 V).

4.2. Current characteristic

Figure 9 shows the leakage current under a normal power-up event, V_{DD} rises from 0 to 1.8 V in 1 ms. The peak leakage current is 24 nA, and leak current keeps at 8.4 nA after the power-up pulse. The clamp MOSFET is thoroughly turned off under normal operating conditions, and the 8.4 nA current is mainly the turn-off leakage current of the clamp MOSFET.

4.3. Immunity to false triggering

In order to explain the excellent immunity to false triggering in some special applications, the simulation conditions are set to 10 ns/5 V, 40 ns/3 V and 60 ns/3 V respectively. Figure 10 shows the waveforms of V_{gate} under the three conditions. The result shows that the clamp circuit is not triggered when the rise time is longer than 60 ns and the power voltage is lower than 3 V. Hence, the novel clamp circuit can avoid the false triggering more effectively.

Here a 40 ns/ 3 V power up event is considered as a low-level ESD event, so the clamp circuit is designed to be triggered under this condition. The sensitiveness of the detect element to fast power-up events can be adjusted by changing the W/L ratios of transistors such as M1 and M2.

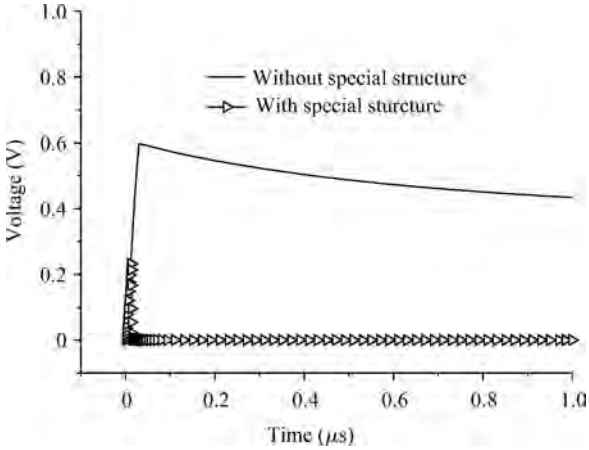

Fig. 11. Waveforms of V_{gate} with and without the special structure under a 30 ns/1.8 V event.

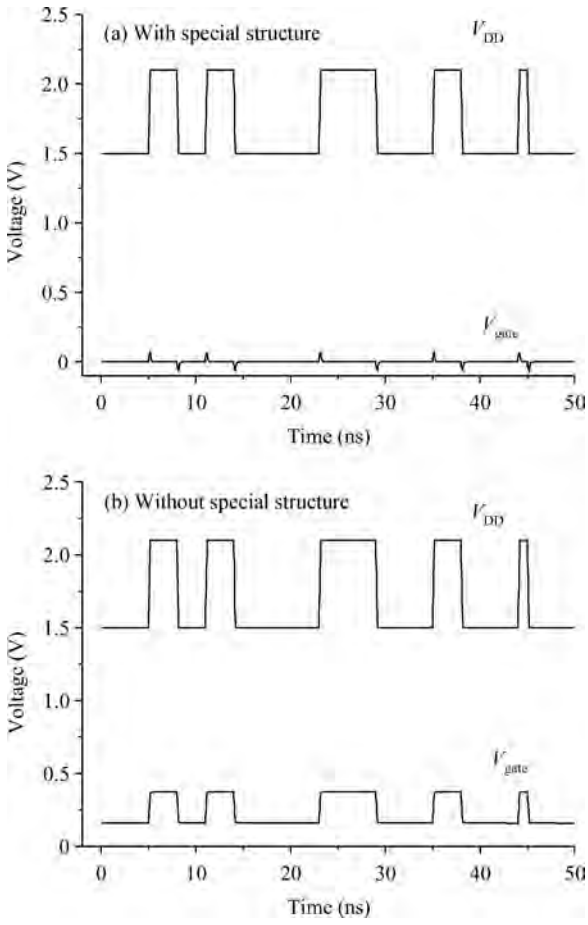

Fig. 12. Waveforms of V_{gate} under the noise characteristics test.

It is necessary to compare the circuits with and without the special structure. Figure 11 shows the simulation result of V_{gate} under a 30 ns/1.8 V power up event. With the special structure, V_{gate} rises to about 0.22 V and then immediately goes back to 0. However, without the special structure, V_{gate} rises to about 0.6 V firstly and then starts to slowly fall. Therefore, the special structure can effectively avoid "sub_mistriggering".

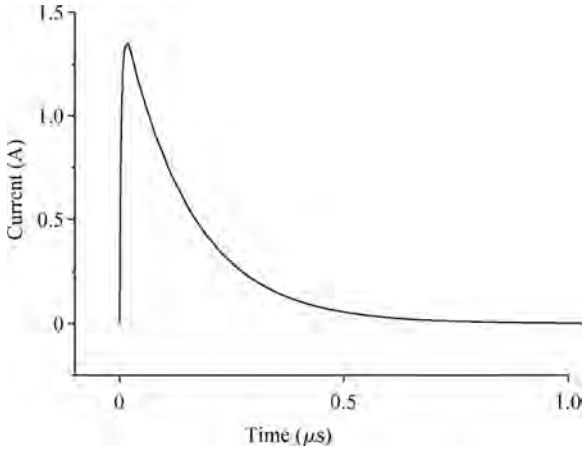

Fig. 13. Waveform of current used to simulate a 2 kV HBM ESD test.

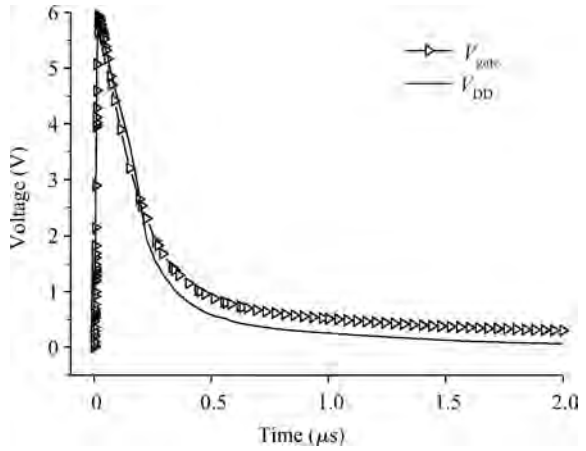

Fig. 14. Waveforms of V_{DD} and V_{gate} under a 2 kV HBM ESD test.

4.4. Noise characteristics

The power supply noise is often seen in a circuit with high switching rates, and it always causes energy consumption and can even trigger the clamp circuit. A pseudorandom pulse is applied as the worst case scenario of power supply noise. The applied noise has a rate of 500 Mb/s and an amplitude of 0.6 V[6]. The noise characteristic of V_{gate} is shown in Fig. 12(a). It can be seen that the maximal voltage of V_{gate} is only about 60 mV, and the peak width is very narrow. So, the proposed clamp circuit rejects power supply noise effectively.

The noise characteristic without the special structure is shown in Fig. 12(b). We can see that V_{gate} varies at about 220 mV, so the special structure can avoid power supply noise effectively. Furthermore, V_{gate} is not thoroughly pulled down to V_{SS}, and M0 may leak energy. As mentioned earlier, this is caused by M5. So the special structure can also guarantee that M0 is thoroughly turned off.

4.5. Circuit-level ESD test

A circuit-level ESD test is necessary for the clamp circuit. According to the US MIL-STD-883 (method 3015.7), the HBM waveform has a rise time of less than 10 ns and a delay time of 120–180 ns. For a 2 kV ESD test, the peak current is 1.33 A ± 10%. The transient current waveform used in the simulation is shown in Fig. 13.

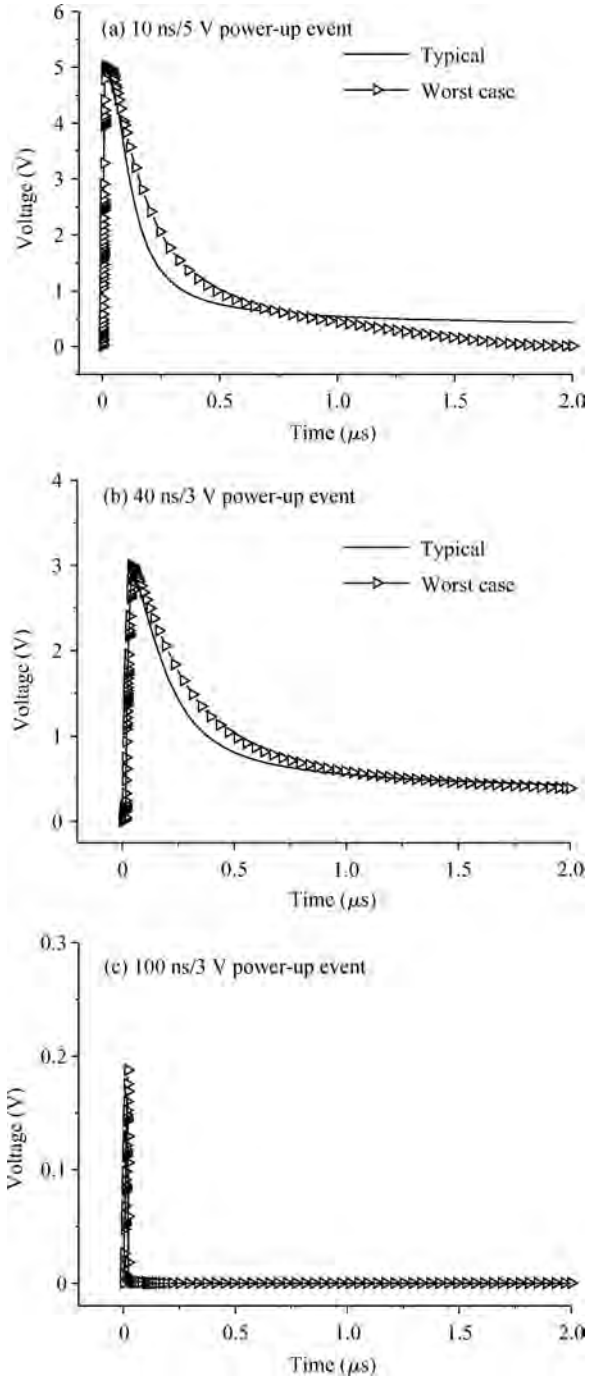

Fig. 15. Comparison of V_{gate} under typical and the worst case.

Figure 14 shows the waveforms of V_{DD} and V_{gate} in a circuit-level ESD test. The maximal voltage of V_{DD} and V_{gate} are about 6 V, and V_{DD} falls to 1.8 V (normal operating voltage) in 0.25 μs. Therefore, the clamp circuit can successfully discharge the ESD energy.

4.6. Process and temperature variations

It is necessary to consider the impact of process and temperature variations (PTV) on the operation of the proposed power clamp. The delay time under very fast power up conditions is simulated for the worst case process variations. The

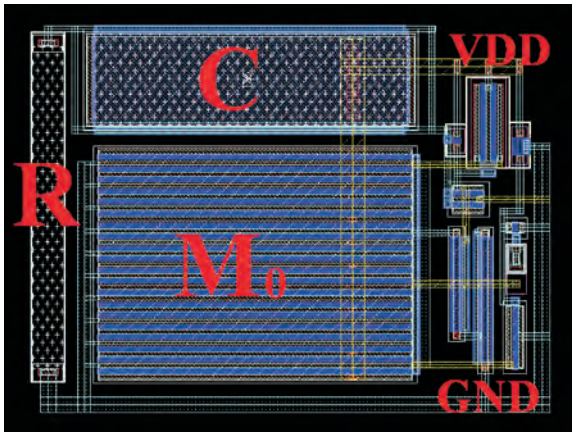

Fig. 16. Layout of the novel clamp circuit.

simulation results are presented in Fig. 15. Here the worst case means the operating condition is 125 ℃ and FF process corner. We can see that under the worst case, 10 ns/5 V and 40 ns/3 V power-up events can trigger the clamp MOSFET, while a 100 ns/3 V power-up event cannot trigger the clamp MOSFET. It illustrates that the proposed circuit passes the PTV test.

4.7. Layout

In the classic clamp circuit, the large capacitor and resistor consume much of the layout area. However, in the novel circuit, the RC time constant is sharply reduced, so it saves some of the layout area. In order to make sure of the reliability of the proposed clamp circuit, the layout is designed strictly according to the ESD layout design rules. Figure 16 shows the layout of the novel clamp circuit. The area of the novel clamp circuit is $33 \times 25\ \mu m^2$.

5. Conclusion

In this paper, a novel ESD power clamp circuit for a 0.18 μm CMOS process is proposed. The clamp circuit adopts a special structure. It maintains a 1.2 μs delay time and a 2.14 μs turn-off time, reduces about 70% RC time constant, and avoids a fast false triggering event such as a 30 ns/1.8 V power-up. Besides, with the consideration of the gate reliability, a voltage margin is considered in the design, where the maximal voltages of the transistor electrodes are 6 V under the 2 kV HBM ESD event.

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