High efficiency class-I audio power amplifier using a single adaptive supply*

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Abstract: A high efficiency class-I linear audio power amplifier (PA) with an adaptive supply is presented. Its efficiency is improved by a dynamic supply to reduce the power transistors' voltage drop. A gain compression technique is adopted to make the amplifier accommodate a single positive supply. Circuit complicity and chip area are reduced because no charge pump is necessary for the negative supply. A common shared mode voltage and a symmetric layout pattern are used to minimize the non-linearity. A peak efficiency of 80% is reached at peak output power. The measured THD+N before and after the supply switching point are 0.01% and 0.05%, respectively. The maximum output power is 410 mW for an 8 Ω speaker load. Unlike switching amplifiers, the class-I amplifier operates as a linear amplifier and hence has a low EMI. The advantage of a high efficiency and low EMI makes the class-I amplifier suitable for portable and RF sensitive applications.

Key words: class-I; power amplifier; gain compression; adaptive supply; power efficiency
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1. Introduction

Audio amplifiers can be categorized into two classes: linear amplifiers and switching amplifiers. Of linear amplifiers such as class-A, B and AB, class-AB has the best linearity, but suffers from bad efficiency. Theoretically, the maximum efficiency of class-A and AB is 50% and 78%, respectively. A switching amplifier such as class-D has a typical efficiency above 80%, but linearity is only moderate and the off-chip inductor and capacitor increases both system cost and board space. A filter-less class-D has been proposed to save the inductor in the output filter, but the load speaker must be the inductive type and be placed closely to the amplifier's output[1]. Recently, class-D has been very popular due to its high efficiency, but it has a serious EMI problem. A class-D will introduce both conducted noise and radiated noise, which will limit their application in a radiation sensitive environment. Although the spread spectrum technique is reported in Refs. [2, 3] to reduce EMI, there is some degradation of linearity due to the clock modulation. To achieve a compromise between efficiency and linearity, a dual supply class-G and class-H were presented in Refs. [4, 5]. Both of them alternate the voltage supply between a pair of positive and negative voltages that has two adaptive levels according to the output signal amplitude. However, there are also two drawbacks in class-G/H. Firstly, the efficiency is improved only if a low voltage supply is used. The efficiency will fall back to a class-AB efficiency when the amplifier is powered with a high supply voltage. Secondly, the generation of a pair of positive and negative supplies increases the circuit complexity and chip area. For example, a buck converter and two charge pumps have to be embedded[4]. To overcome the two drawbacks of the conventional class-G/H, a class-I and a multilevel class-G have been presented in Refs. [6, 7]. They are single supply rail amplifiers and use a continuous supply or a multi-level supply to improve efficiency. However they suffer from THD+N deterioration after supply switching. This paper presents a novel design to reduce the THD+N deterioration.

The class-I amplifier can maintain a higher efficiency than class-AB in the whole power range. The extra cost is only a buck convertor on the chip, and a much smaller external LC filter than those in class-D. The higher efficiency in the class-I amplifier is due to its adaptive positive supply, which is generated by an on-chip buck converter. A switching point is chosen as a separation point of small and large signal amplitude. Before the switching point, a fixed low voltage supply will be applied to the main amplifier. After the switching point, the supply will vary continuously to track the output amplitude. The aim is to keep the transistors' voltage drop small in any output amplitude. Thus, the efficiency is always better than that of a class-AB. A typical waveform of a class-I and class-G with dual supplies is shown in Fig. 1. The class-I is actually a kind of envelop tracking amplifier, to which has been introduced a RF power amplifier and an ADSL line driver as in Refs. [8, 9].

To achieve a single supply operation, a gain compression technique was adopted. The power efficiency of the charge pumps is lower than that of the inductor based switching converters, so removal of the negative supply can avoid using the charge pump and help to improve the power efficiency. Another benefit is that this design can be implemented in a standard CMOS process which is preferred in the SOC design. If a negative supply is adopted, a triple well process is necessary and increases the system cost[6]. The proposed class-I amplifier is suitable for portable applications where high power efficiency, high linearity, small board size and low system costs are desired.

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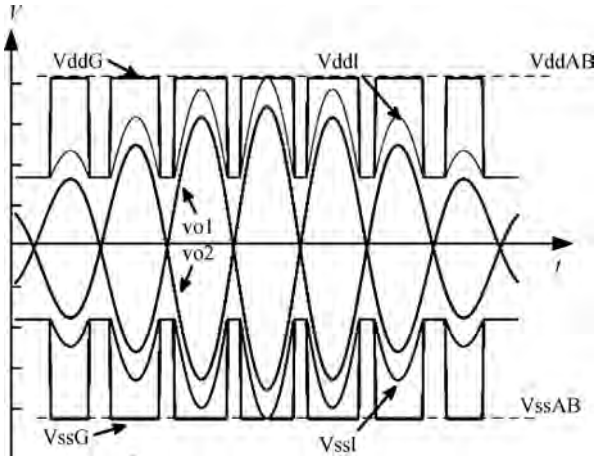

Fig. 1. Supply waveform of class-I, G and AB.

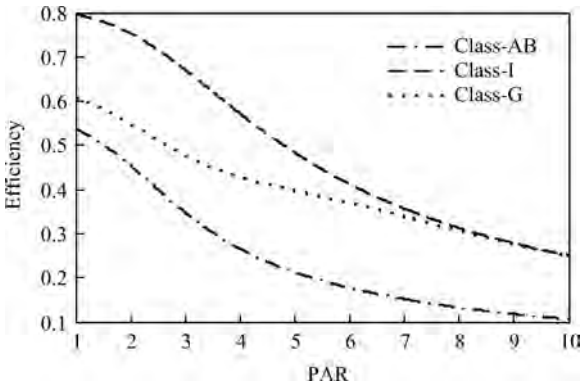

Fig. 2. Average efficiency of class-I, G and AB versus PAR.

2. Efficiency comparison

Efficiency analysis of the power amplifier for a sine type signal has been done by Refs. [6, 7, 10]. This paper presents an analysis of efficiency versus a general audio signal. In general, amplitude of audio signal (such as speech, music) approximately follows the distribution of the Gauss probability[10]. The probability density function (PDF) of a Gauss distributed voltage signal can be expressed in Eq. (1).

$$\mathrm{pdf}(V) = \frac{1}{\sqrt{2\pi}\sigma}\exp\left(-\frac{V^2}{2\sigma^2}\right), \quad V \in (-V_\mathrm{p}, +V_\mathrm{p}), \quad (1)$$

where the standard deviation σ stands for the root mean square (RMS) voltage, and V_p is the peak voltage amplitude. V_p and σ can be related by PAR which is defined as the peak voltage to RMS average voltage ratio i.e. PAR $= V_\mathrm{p}/\sigma$. The average power can be calculated as:

$$P_\mathrm{av} = \int_{-V_\mathrm{p}}^{+V_\mathrm{p}} P_\mathrm{inst}(V)\mathrm{pdf}(V)\mathrm{d}V, \quad (2)$$

where $P_\mathrm{inst}(V)$ is the instantaneous power with amplitude V and P_av is the average power of signals with a PDF of pdf(V). From Eqs. (1) and (2), the average efficiency for a given PDF can be calculated as Eq. (3).

$$\eta_\mathrm{avg} = \frac{P_\mathrm{av\text{-}out}}{P_\mathrm{av\text{-}in}}, \quad (3)$$

where $P_\mathrm{av\text{-}out}$ and $P_\mathrm{av\text{-}in}$ are the average output and input power, respectively. The average efficiency of PA can be calculated according to signal and supply voltage expression. In class-I, the generated supply voltage can be written as in Eq. (4),

$$V_\mathrm{sup} = \begin{cases} V_\mathrm{low}, & 0 < V < V_\mathrm{low} - V_\mathrm{hr}, \\ V + V_\mathrm{hr}, & V_\mathrm{low} - V_\mathrm{hr} < V < V_\mathrm{p}, \end{cases} \quad (4)$$

where V_low is the minimum supply voltage and V_hr is the voltage headroom from supply to output voltage. By combining Eqs. (1)–(4), the average efficiency of class-I can be calculated as in Eq. (5). The efficiency expression of class-G and class-AB is shown in Eqs. (6) and (7).

$$\eta_\mathrm{av\_I} = 2\int_0^{V_\mathrm{p}} \frac{V^2}{R_\mathrm{L}}\mathrm{d}V \times \left[2\int_0^{V_\mathrm{low}-V_\mathrm{hr}} V_\mathrm{low}\frac{V}{R_\mathrm{L}}\mathrm{pdf}(V)\mathrm{d}V + 2\int_{V_\mathrm{low}-V_\mathrm{hr}}^{V_\mathrm{p}} (V + V_\mathrm{hr})\frac{V}{R_\mathrm{L}}\mathrm{pdf}(V)\mathrm{d}V\right]^{-1}, \quad (5)$$

$$\eta_\mathrm{av\_G} = 2\int_0^{V_\mathrm{p}} \frac{V^2}{R_\mathrm{L}}\mathrm{d}V \times \left[2\int_0^{V_\mathrm{low}-V_\mathrm{hr}} V_\mathrm{low}\frac{V}{R_\mathrm{L}}\mathrm{pdf}(V)\mathrm{d}V + 2\int_{V_\mathrm{low}-V_\mathrm{hr}}^{V_\mathrm{p}} \frac{V_\mathrm{high}V}{R_\mathrm{L}}\mathrm{pdf}(V)\mathrm{d}V\right]^{-1}, \quad (6)$$

$$\eta_\mathrm{av\_AB} = 2\int_0^{V_\mathrm{p}} \frac{V^2}{R_\mathrm{L}}\mathrm{d}V \times \left[2\int_0^{V_\mathrm{p}} V_\mathrm{sup}\frac{V}{R_\mathrm{L}}\mathrm{pdf}(V)\mathrm{d}V\right]^{-1}. \quad (7)$$

Using Eqs. (5)–(7), an efficiency comparison of class-I, G and AB versus PAR is shown in Fig. 2. The parameters are chosen as: $V_\mathrm{p} = 2.8$ V, $V_\mathrm{low} = 1.4$ V, $V_\mathrm{high} = 3.2$ V, $V_\mathrm{hr} = 0.4$ V, $R_\mathrm{L} = 8\ \Omega$, and class-G's switching point is the same as that of class-I. The efficiency of Class-I is the highest among the three types. Class-G has a moderate efficiency, and class-AB has the worst efficiency as expected. When PAR is close to 10, the efficiency curves of class-G and class-I overlap, because most of the signal amplitude is below the switching point in this case, and they had the same supply voltage. For a common audio signal, PAR ranges from 3 to 10. Class-I shows its superior average efficiency performance compared to class-AB.

3. Implementation

3.1. System overview

The class-I consists of a level detector and process (LDP) block, a DC/DC converter, and a bridge tied load (BTL) output PA, as shown in Fig. 3. LDP detects the amplitude of the input, pre-amplifies signals before BTL and generates the reference input V_ref for the DC/DC converter. The DC/DC converter's regulated output V_sup is used to power the BTL PA, which drivers the external speaker.

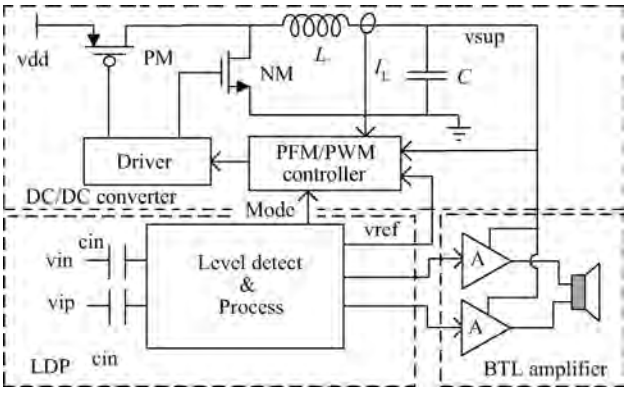

Fig. 3. Architecture of class-I.

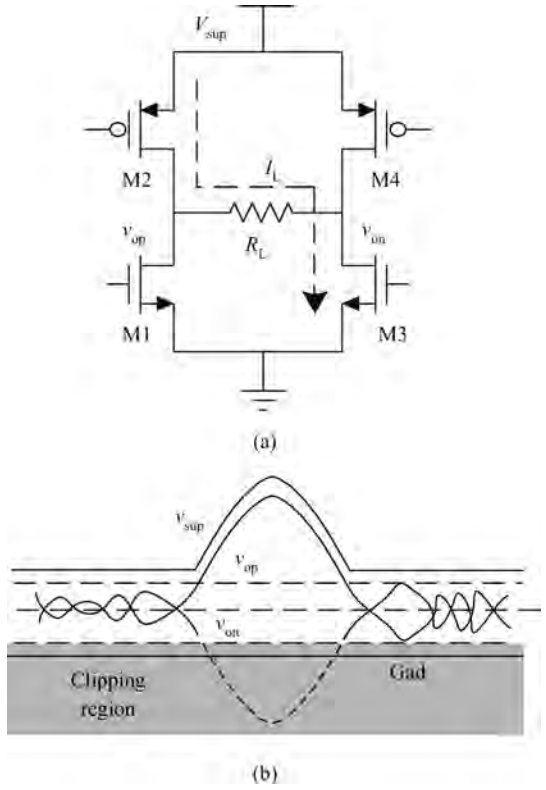

Fig. 4. Output stage with single supply voltage. (a) Schematic. (b) Clipping of large signal at the ground.

3.2. Gain compression and LDP

In a single rail power supply, gain compression is used to extend the output voltage range. A BTL output stage is shown in Fig. 4. To improve efficiency, the power transistor's voltage drop must be kept small. If the load current flows in the same direction as in Fig. 4(a), for high efficiency, the output voltage V_{op} and V_{on} will be close to V_{sup} and ground, respectively. When the signal amplitude increases and V_{sup} starts to track V_{op}, V_{on} will be limited by GND and cannot extend to the negative supply. This clipping as shown in Fig. 4(b) will cause serious distortion. To avoid clipping, the gain compression technique fixes the low end output voltage, while extending the high end voltage by a doubled gain. Therefore, the differential gain is the same as that with dual supply. The function

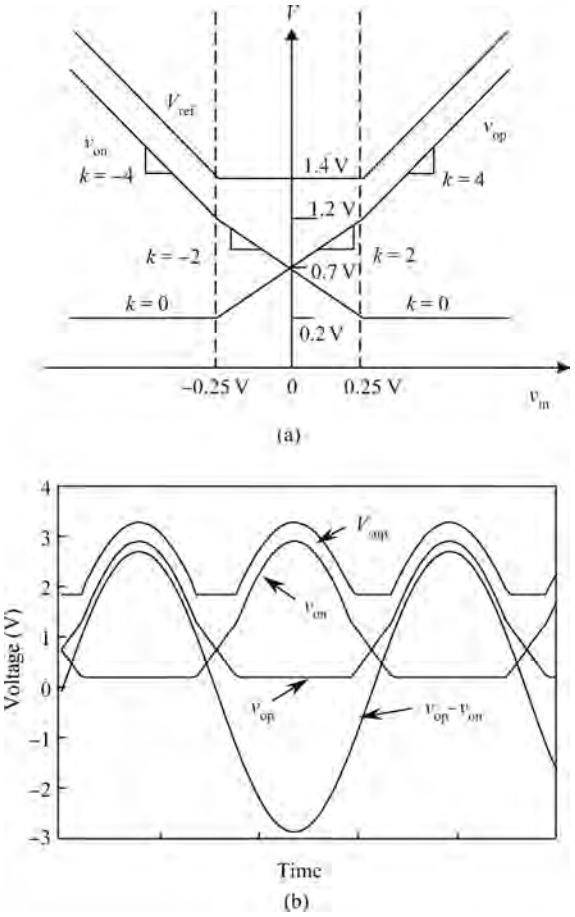

Fig. 5. Gain compression. (a) DC transfer curve. (b) Transient waveform.

of gain compression is shown in Fig. 5(a). In this design, the class-I amplifier has a fixed gain of four. For a differential input voltage within ±0.25 V, the gain from input to V_{op} and V_{on} are +2 and –2, respectively. For differential input voltage larger than 0.25 V, the gain from input to V_{op} and V_{on} are four and zero. Although the single end gain varies with output amplitude, the differential gain is independent of output amplitude. Figure 5(b) shows a transient sinusoid output waveform.

The implementation of gain compression is shown in Fig. 6. The audio signal is pre-amplified by a full differential amplifier OP1 with a gain of four. The audio amplitude level is derived by two comparators, CMP1 and CMP2. The comparator outputs s1–s4 control the signal connected to V_n and V_p. A resistor chain formed by R_1–R_4 divides the voltage from V_{n2} to V_{p2}. R_1–R_4 also function as the common mode (CM) feedback resistor of OP1. When using gain compression, there are two points which may bring non-linearity. The first is the common-mode voltage of V_{cm} and OP1. A common mode sharing structure here feeds OP1's CM output V_{cm} to BTL's CM input. This structure avoids the non-linearity introduced through CM variation in Refs. [6, 7]. The second is the mismatch of resistors R_1–R_4. The gain from input to BTL's input is $(V_p–V_n)/V_{in}$ and it should be kept constant. The signal pair feed to V_n and V_p is (V_{n2}, V_{cm}) or (V_{n1}, V_{p1}) or (V_{cm}, V_{p2}) according to the signal amplitude. To keep a constant gain and guarantee the linearity, R_1–R_4 should be designed to satisfy

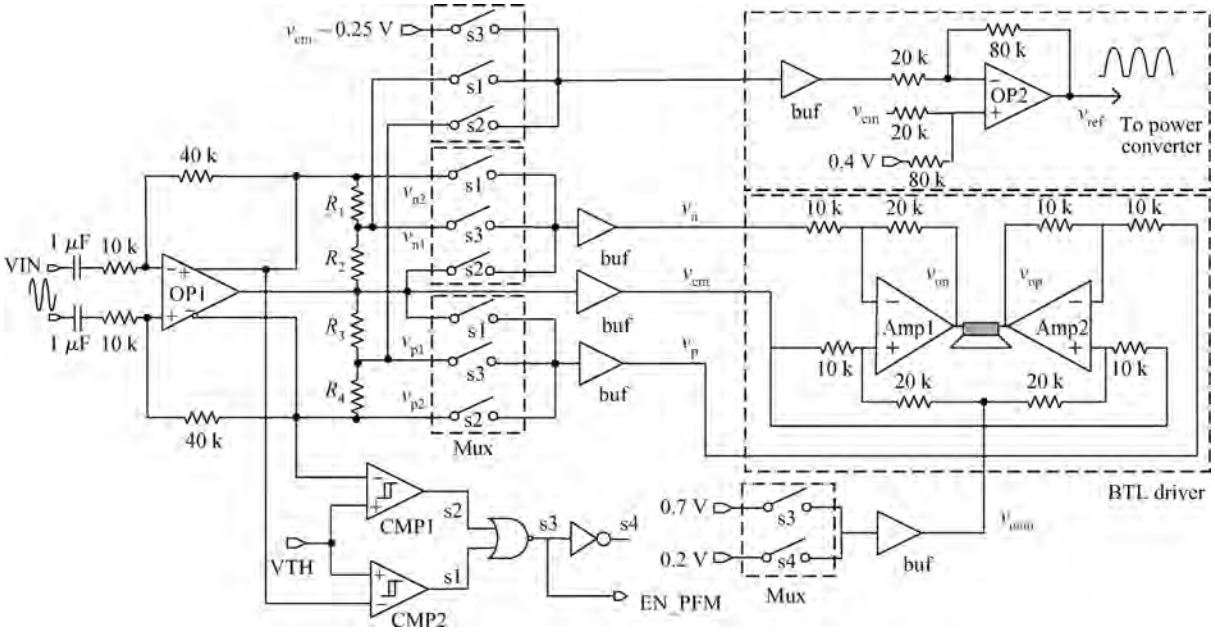

Fig. 6. Schematic of LDP.

$R_1 + R_2 = R_2 + R_3 = R_3 + R_4$, which is equivalent to $R_1 = R_3$ and $R_2 = R_4$. Note that V_{ref} is generated according to V_{n1} and V_{p1}, so R_2 should equal to R_3, otherwise the peak voltage of V_{ref} will be different due to the different amplitude of V_{n1} and V_{p1}. The four resistors should be designed with the same value. Special attentions are paid to the match of R_1 with R_3 and R_2 with R_4 during layout design, because the mismatch of R_2 and R_3 only has a small effect on the amplitude of V_{ref} which has no effects on THD+N.

To verity the effect of mismatch introduced non-linearity, a simulation of THD for a 300 mV input amplitude versus mismatch is performed and the result is shown in Fig. 7. It is shown that a 0.5% mismatch will degrade the THD to about –60 dB. In order to achieve good linearity, a mismatch of less than 0.2% is preferred. The well matched layout pattern of the four resistors is shown in Fig. 8. Each resistor is divided into 16 segments. R_1 and R_3 share the same central line as well as R_2 and R_4. The length of wire connections in each resistor pair is kept the same to minimize parasitic introduced mismatch.

In the gain compression technique, the common mode output voltage of BTL driver, V_{ocm}, is changed according to signal amplitude. The output amplifiers Amp1 and Amp2 in BTL are the inverting type. Outputs of BTL can be expressed as $V_{on} = V_{ocm} - 2(V_n - V_{cm})$ and $V_{op} = V_{ocm} - 2(V_p - V_{cm})$. With small output amplitude, V_{on} and V_{op} are symmetrical differential signal. To maximize output voltage swing, V_{ocm} is set at 0.7 V which is half of the 1.4 V supply voltage. With large output amplitude, one of V_{on} and V_{op} has no gain and equals to their common mode voltage V_{ocm}. V_{ocm} is also the voltage drop of the conducted NMOS transistor as in Fig. 4(a). A 0.2 V V_{ocm} is chosen in this case, which is a tradeoff between the power dissipation and the saturation drain-source voltage of the NMOS transistors.

The reference voltage for the dynamic supply is OP2's output voltage in Fig. 6. OP2 is an inverting amplifier with a gain of four. When V_{ref} has to track the higher voltage of output, the lower voltage of v_{n1} and v_{p1} is selected to the input of OP2, and the gain from V_{in} to V_{ref} is the same as that to V_{on} or to V_{op}. The headroom between V_{ref} and the output amplitude is controlled by common mode output of OP2, which is 0.4 V in this design.

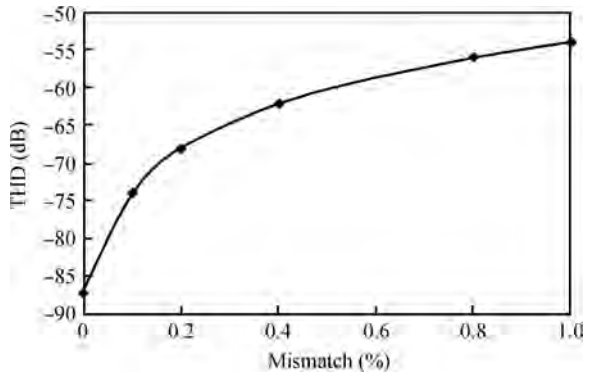

Fig. 7. Simulated THD versus mismatch of resistors with 1.2 V output.

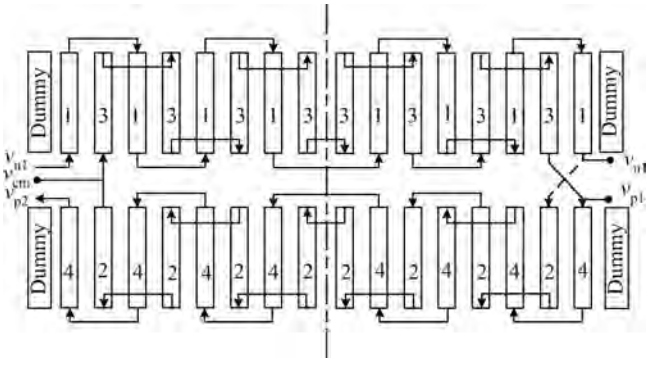

Fig. 8. Layout of matched resistors R_1–R_4.

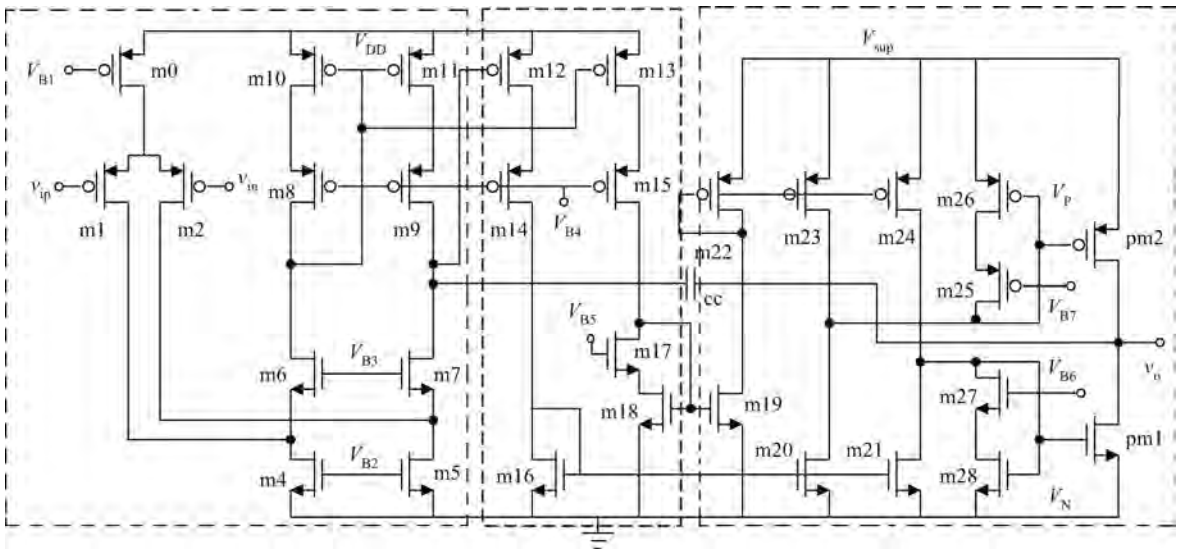

Fig. 9. Schematic of the classAB amplifier.

3.3. PSRR and a class-AB amplifier

In this design, the PA's supply is on-chip generated and a voltage ripple is inevitable in the switching converter. The designed converter has a 20 mV ripple in PWM mode and a 60 mV ripple in PFM mode. High PSRR is critical to suppress the effects from the supply ripple. A three stage amplifier, as shown in Fig. 9, is used as the PA. It uses separated supplies for the high gain stage and the output stage. A detailed analysis of this amplifier can be found in Ref. [11]. As the third stage of the amplifier is supplied by an adaptive supply, the ripple voltage is larger than the global supply V_{dd}. A high PSRR of V_{sup} is necessary to avoid the supply noise coupled to the output. A high PSRR of V_{sup} is guaranteed from two aspects. Firstly, the BTL output driver is to some degree a differential structure and the noise from V_{sup} is a common mode noise at the two outputs. Second, V_{sup} is only applied to the output stage of the amplifier. Assuming that the signal gain is A and the supply noise gain is A_n, then A, A_n and PSRR can be expressed as Eqs. (8)–(10).

$$A = g_{m1}g_{m9}r_{o9}r_{o1}\frac{g_{m12}}{g_{m16}}\frac{g_{m20}}{g_{m26}}g_{mpm2}(r_{opm1}/\!/r_{opm2}), \quad (8)$$

$$A_n = g_{mpm2}(r_{opm1}/\!/r_{opm2}), \quad (9)$$

$$\mathrm{PSRR} = \frac{A}{A_n} \approx g_{m1}g_{m9}r_{o9}r_{o1}\frac{g_{m12}}{g_{m16}}\frac{g_{m20}}{g_{m26}}, \quad (10)$$

where g_m is the trans-conductance and r_o is small signal resistance. It is shown that PSRR is approximately equals the voltage gain of the first two stages. The gain of the amplifier is mainly contributed by the first stage. Its PSRR is high enough for noise suppression. Simulation results shows a minimum of 109 dB PSRR for V_{sup} in the 20–20 kHz audio band.

3.4. Dynamic power supply

A dynamic power supply is generated by a DC/DC converter. Its reference and mode control signal are generated in LDP as in Fig. 6. Unlike the traditional DC/DC converter, in this application, the regulated output is not a constant DC voltage but varies with the audio signal, and the output power will change in a wide dynamic range. Thus the converter needs a fast loop response to its varying reference, and it should be highly efficient in both light and heavy load conditions. A PFM/PWM dual mode buck converter as shown in Fig. 10 is adopted in this design. To achieve fast response and avoid a supply introduced audio distortion, the bandwidth of the control loop is set at 250 kHz, which is ten times higher than the audio band. The convertor works in PFM mode at light load and PWM mode at heavy load to improve overall power efficiency in all load conditions. To reduce the external devices' size, a high clock frequency is desired. High switching frequency, however, may lead to excessive switching losses and will degrade the converter's efficiency. As a compromise the clock frequency in the PWM mode is 2 MHz. The external devices were chosen as $L = 2.2\ \mu$H and $C = 2\ \mu$F. The inductor used in this converter is much smaller than that used in the class-D amplifier where a typical inductance is 15–33 μH. The PWM control loop is an average current mode control. Current sense is implemented using a G_m–C method. The PFM con-

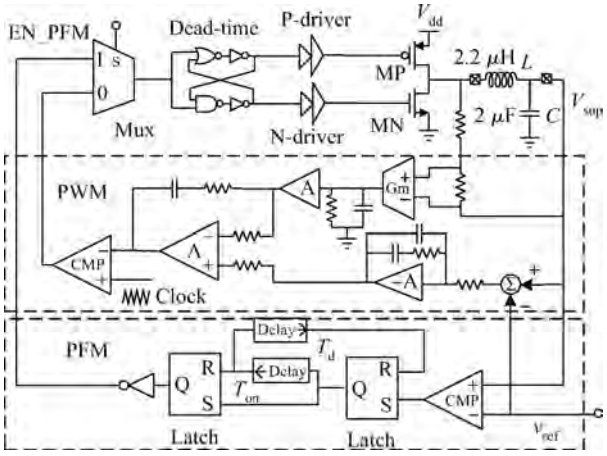

Fig. 10. Block diagram of the DC/DC converter.

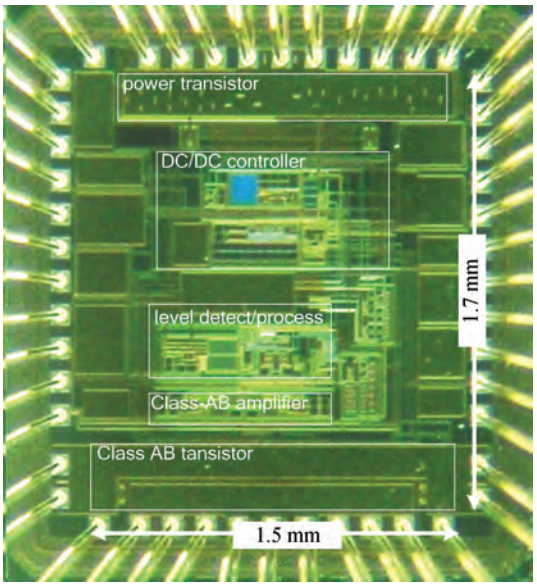

Fig. 11. Die micrograph.

troller is a constant on time controller which can help to keep the switching frequency so it does not interfere with the audio band in light load conditions.

4. Experimental results

The prototype was fabricated in an SMIC 0.18-μm 3.3 V CMOS process. Figure 11 is the die micrograph of the chip. The core size is 1.7×1.5 mm^2.

The measured THD+N results versus output power and frequency are shown in Figs. 12(a) and 12(b). The THD+N increased from 0.01% to 0.05% after the switching point. The maximum output power, defined as the output power at 1% THD+N, is 410 mV.

The first seven harmonics spectrum before and after the switching point are shown in Figs. 13(a) and 13(b). In Fig. 13(a), the amplitudes of second and third order harmonic are very close. The distortion is mainly caused by odd harmonics before the switching point. In Fig. 13(b), a distinct increase of an even harmonics amplitude is observed and is the main source of the distortion. The even harmonics are not effectively suppressed, because the waveforms of V_{on} and V_{op} are not symmetric and the BTL output is not a true differential structure after the switching point. The asymmetry of the system and the mismatch of resistors cause a deterioration of THD+N. .

Figure 14 shows the efficiency comparison of measured class-I and theoretical class-AB. Efficiency is measured by applying a sinusoid input with different amplitudes. It shows an obvious efficiency improvement from class-AB to class-I. Figure 14 also shows a theoretical output power probability of an audio signal, which follows a Gauss distribution with a 2.5 V peak amplitude and 15 dB PAR. A 65% efficiency is obtained when the probability density is higher than 10%. The quiescent power measured is 9.9 mW. The performance summary and comparison are summarized in Table 1. According to Ref. [12], the FOM of the power amplifier is defined as the ratio of peak power delivered to the load of the quiescent power.

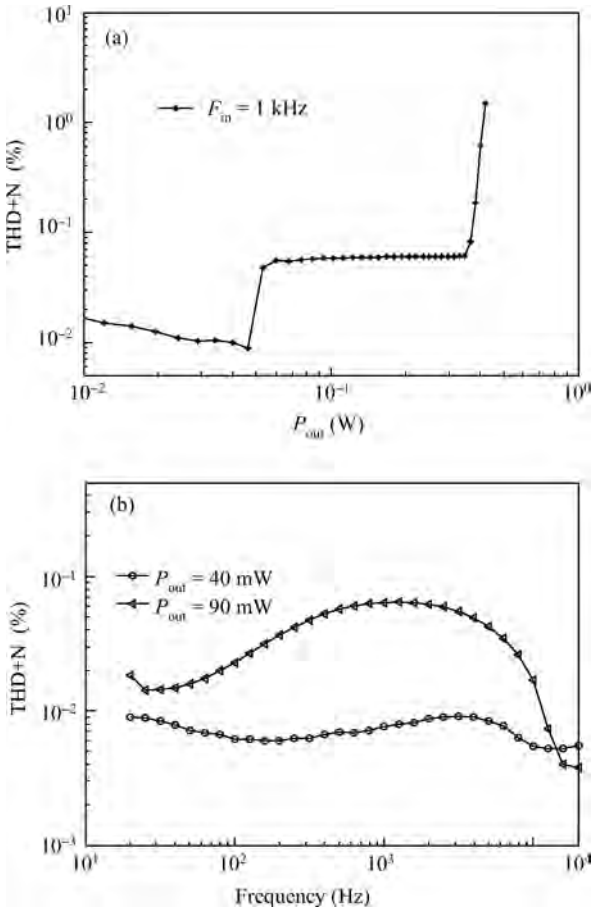

Fig. 12. Measured THD+N versus (a) output power and (b) frequency.

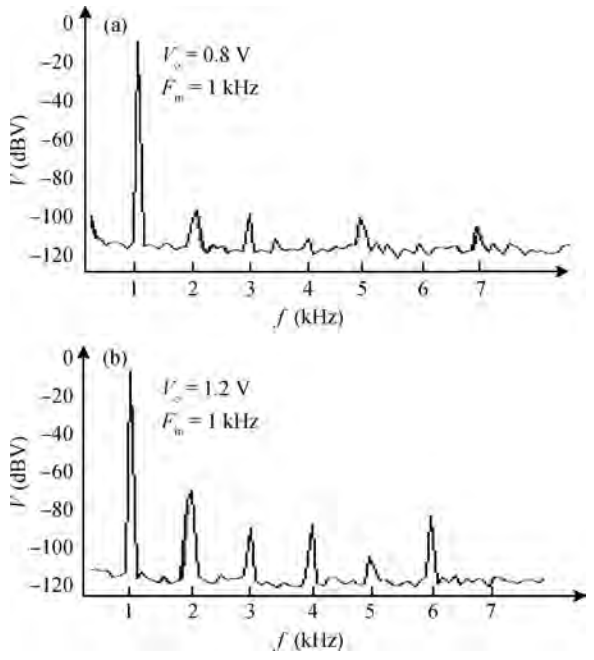

Fig. 13. Output spectrum at (a) 0.8 V output and (b) 1.2 V output.

5. Conclusion

A high efficiency, class-I linear audio amplifier is presented. High efficiency is achieved by adopting an adaptive

Table 1. Measurement summary and performance comparison.

Parameter	This work Class-I	ISSCC2010 Class-G[4]	MAX97200 Class-H[5]	ISSCC2008 Class-AB[12]
Technology	180 nm CMOS	65 nm CMOS	Bi-CMOS	130 nm CMOS
Quiescent power (mW)	9.9	0.41	2	1.2
Max P_{out}[1] (mW)	410	90	90	40
Peak efficiency (%)	80	70	67	Unavailable
Maximum efficiency at 15 dB PAR input[2] (%)	65	60	60 (Estimated)	Unavailable
THD+N (dB)	–80	–80	–87	–84
FOM[3]	41.4	219.5	22.5	33.3

1: Output power at 1% THD+N. 2: Output amplitude probability > 10%. 3: FOM = (Peak output power)/(Quiescent power).

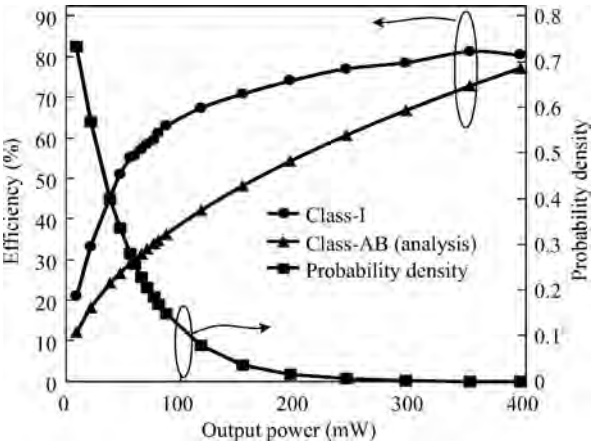

Fig. 14. Efficiency comparison of measured class-I and class-AB.

supply which effectively reduces power dissipation on power transistors. This design reveals a new method to improve power efficiency without using a switching amplifier. With proposed common mode sharing in gain compression, the presented design shows an improvement in THD+N after the switching point than previous designs. The presented design is compatible with standard CMOS processes which makes it suitable for SOC integration.

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