A Novel Radiation Tolerant SOI Isolation Structure

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Abstract : A novel radiation tolerant SOI isolation structure ,consisting of thin SiO_2/ polysilicon / field SiO_2 multilayers ,is proposed. A device with this structure does not show obvious changes in subthreshold characteristics and leakage current ,indicating a superior radiation tolerance to traditional LOCOS.

Key words : isolation structure ; radiation tolerance ; SOI
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1 Introduction

Silicon-on-insulator (SOI) devices are attractive elements for high-performance ,radiation hardened ,and CMOS circuits. While device isolation in SOI CMOS provides complete immunity to latch-up ,SOI structures are also less susceptible to transient radiation and single-event upset due to the reduced semiconductor charge collection volume of the thin silicon layers[1,2]. Although interactions between devices on separate islands are readily eliminated with SOI technology ,potential parasitics exist within an island. Device conduction can occur via three paths : (1) the conventional top channel at the gate-oxide/ Si interface ; (2) the back channel at the Si/ buried oxide (BOX) interface ; and (3) the edge-channel along the sidewalls of the island.

All of these three regions are subject to total dose radiation effect. Techniques exist for hardening the top and back channels , leaving sidewall effect as the critical SOI total dose radiation hardening issue. Total dose radiation effects on the top channel can be controlled by bulk gate oxide radiation hardening techniques[3] , and back channel leakage in nMOSFET can be suppressed by applying a negative substrate bias that reduces the radiation induced positive charge build-up at the BOX/ Si interface. A deep B implantation can also be used to raise the back channel threshold voltage[4,5]. However ,there still remains edge-channel conduction ,the most difficult leakage to suppress.

In this paper , a new isolation technology , which can suppress edge-channel conduction , is proposed ,and its effectiveness is verified.

2 Experiment

2.1 Isolation structure

Figure 1 shows the schematic cross-section of the isolation structure. This structure consists of thin SiO_2/ polysilicon/ field SiO_2 multilayers. The polysilicon layer at the sidewall of the body region is connected to the substrate. When the CMOS/ SOI device is irradiated , electrons induced by the positive charge trapped in the field SiO_2 layer appear only in the sidewall polysilicon layer and the substrate near the Si/ SiO_2 interface , because the polysilicon layer is connected to the substrate. The polysilicon layer works so as to shield the body region from the radiation-induced positive charge

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trapped in the field SiO_2 layer. On the other hand, the positive charge trapped in the thin sidewall SiO_2 layer adjacent to the body region can induce electrons at the sidewall surface of the body region. However, since the concentration of these electrons can be decreased beyond the channel impurity concentration by reduction of the thickness of the sidewall SiO_2 layer, a depletion or an inversion region cannot be formed. That is to say, edge-channel conduction can be suppressed.

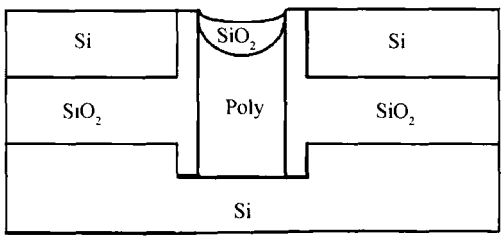

Fig. 1 Schematic cross-section of the isolation structure

2.2 Process

20μm/1.2μm PD SOI nMOSFETs are fabricated on SIMOX wafers with a buried oxide thickness of 370nm and a top silicon thickness of 197nm. The CMOS/SOI fabrication process with this structure starts with the growth of a thermal pad oxide, followed by the deposition of a silicon nitride layer. A pattern is applied and the trench is etched though the nitride, oxide, silicon film, and BOX in turn and approximately 250nm into the substrate. Next, an oxidation is performed at 850 ℃ to obtain a 50nm SiO_2. Then, SiO_2 is etched back and the substrate at the bottom of the trench is exposed. The trench is filled with a 1000nm deposited polysilicon film and the polysilicon is etched back to the top of the nitride using reactive ion etch (RIE). The processes of filling and etching are repeated one more time to planarize the surface. After the diffusion of phosphor, a field oxidation is performed at 910 ℃ to avoid a short. Next, the nitride is removed, followed by well implants, gate oxidation, and gate electrode formation.

The gate oxide thickness of all devices is 20nm. After the pattern of the n^+ doped polysilicon LDD structure is formed using phosphorus implantation with a dose of $2.5\times10^{13}\,cm^{-2}$ and energy of 30keV, the oxide spacers are formed, followed by source/drain doping (As, 80keV, $4\times10^{15}\,cm^{-2}$). 20nm Ti is deposited to form Titanium silicide contacts on the source/drain and polysilicon regions.

Figure 2 shows the cross-section SEM of the structure after trench-etching, twice deposition and etching of polysilicon and field oxidation. 20μm/1.2μm nMOSFETs with LOCOS isolation are also fabricated to compare radiation tolerance.

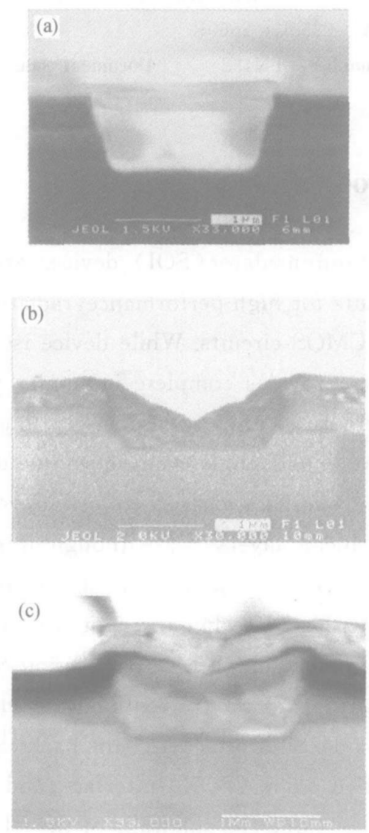

Fig. 2 Cross-section SEM of the structure (a) After trench-etching; (b) Twice deposition and etching of polysilicon; (c) Field oxidation

2.3 Measurements and radiation characterization

The characteristics of the nMOSFETs are measured with a HP 4145A parameter analyzer. Radiation experiments are performed using Co^{60} Gamma rays with a dose rate of 230rad(Si)/s. The source, back gate and body tie are grounded and the

front gate and drain are biased at 3V during the radiation. All the measurements are finished within 1h after the radiation.

3 Results and discussion

Figure 3 shows the subthreshold characteristics of the closed-gate device which eliminates the edge-channel. After a 10^6 rad(Si) radiation, the subthreshold characteristics show less change and no obvious leakage current, indicating a radiation tolerance of the front and back gates exceeding 10^6 rad (Si). Figure 4 shows the subthreshold characteristics of the LOCOS isolated device. The device does not show obvious leakage current before radiation. However, after a total dose radiation of 3×10^5 rad (Si), the leakage current exceedes 1nA due to the conduction of the edge-channel. Conversely, the subthreshold characteristics of the device with the novel isolation structure does not change much, and the leakage current is still very small after a total dose radiation of 3×10^5 rad(Si), as shown in Fig. 5. Thus, the radiation tolerance of the novel isolation structure is superior to that of the traditional LOCOS.

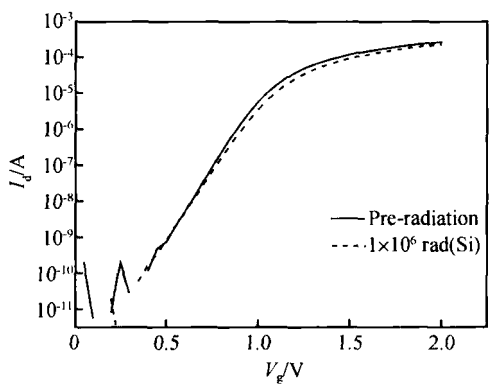

Fig. 3　Subthreshold characteristics of closed-gate device

4 Conclusion

A novel radiation tolerant SOI isolation structure which consists of thin SiO_2/polysilicon/field SiO_2 multilayers is presented. The subthreshold characteristics do not change much and the leakage current does not increase obviously after a total dose radiation of 3×10^5 rad(Si), compared with the device isolated by LOCOS.

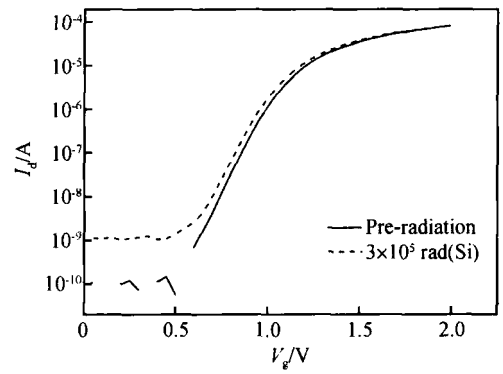

Fig. 4　Subthreshold characteristics of LOCOS isolated device

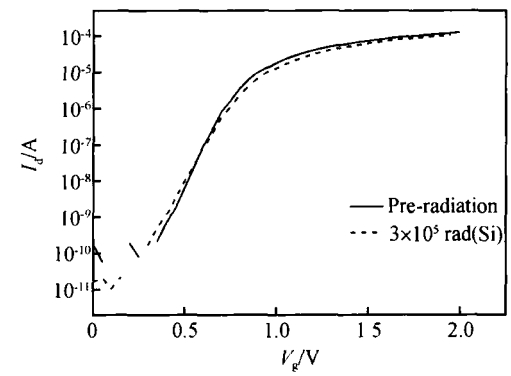

Fig. 5　Subthreshold characteristics of device with the novel isolation structure

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一种新型抗辐照 SOI 隔离结构

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摘要: 制备了一种新型抗辐照 SOI 隔离结构,它包含了薄 SiO_2/多晶硅/SiO_2 多层膜. 利用这种结构制备的 SOI 器件在经受 3×10^5 rad(Si)的辐照后亚阈值特性未发生明显变化,漏电流也无增加,说明其抗辐照性能优于传统的 LOCOS 隔离结构.

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