Low Phase Noise Quadrature Oscillators Using New Injection Locked Technique *

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Abstract: A low phase noise quadrature oscillator using the new injection locked technique is proposed. The incident signal is directly injected into the common-source connection of the sub-harmonic oscillator. In principle, the phase noise performance of the quadrature output is better than the sub-harmonic oscillator itself. The quadrature oscillator is implemented in a 0.25μm CMOS process. Measurements show the proposed oscillator could achieve a phase noise of -130dBc/Hz at 1MHz offset from 1.13GHz carrier while only drawing an 8.0mA current from the 2.5V power supply.

Key words: oscillator; RF; CMOS; phase noise
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1 Introduction

Among many techniques proposed to generate the quadrature carrier signals, the LC coupled quadrature oscillator has a lower phase noise performance and is widely used in RF transceivers. The quadrature signals are generated by inducing some type of coupling between two sub-harmonic oscillators[1~5]. Although many coupled methods are proposed, these methods all worsen phase noise performance. The phase noise of the quadrature signals is worse than the sub-harmonic oscillators themselves.

In this paper, a new method is proposed to generate low phase noise quadrature carrier signals. The method utilizes the new implementation of the injection locked technique. In principle, the phase noise performance of the quadrature output is better than the sub-harmonic oscillators themselves. A quadrature oscillator using the proposed injection locked technique is presented to evaluate the new implementation potentialities.

2 New implementation of injection-locked technique

In Refs. [6~8], the super-harmonic injection locked oscillators as low power frequency dividers are proposed. Figure 1 shows the original schematic of the differential injection-locked frequency divider. It is essentially a LC oscillator (we refer to as "sub-harmonic oscillator"), except that the incident signal is injected into the gate of M3, which delivers the incident signal to the common source connection (the node "S") of M1 and M2. The node S, even in the absence of the incident signal, oscillates at twice the frequency of the output signals, and is an appropriate injection node for a divide-by-two operation. After the lock, the output frequency will be one half the incident signal frequency, and the frequency divider operation is implemented.

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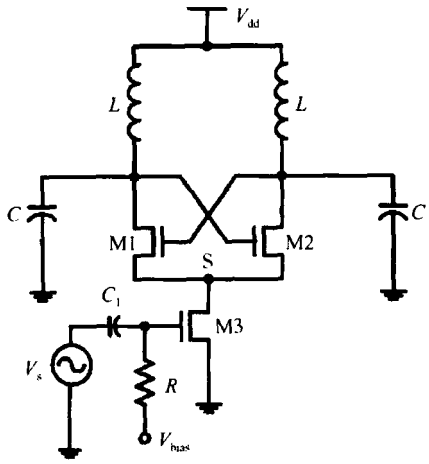

Fig. 1 Original schematic of the differential injection-locked frequency divider

However ,the phase noise of the divider output is dependent on the noise performance of the incident signal. It would be worsened by excess noise from the sub-harmonic oscillator[6~8]. Since the incident signal is usually generated by a high frequency oscillator (we refer to as "main oscillator") which oscillates at twice the frequency of the divider outputs ,its phase noise is poor ,and this results in poor phase noise performance for the divider outputs. If the divider outputs are the desired carrier signals ,the high phase noise would significantly worsen the system performance.

In this paper ,we propose a new implementation of the injection locked technique. As shown in Fig. 2 ,the divider is changed to a top-biased LC oscillator ,and M3 is its tail current source. The incident signal is directly injected into the common source connection (the node "S") of M1 and M2 , and a narrowband noise filtering network (the inductor L_1 and the parasitic capacitance at the node S) is added to the same node S. The noise filtering network resonates at twice the frequency of the divider output and provides a high impedance only in the narrow band of the second harmonic frequencies that stops the cross-coupled pair (M1 and M2) in triode from loading the resonator (L and C). This could suppress the troublesome noise frequencies in the incident signal ,making it appear noiseless to the sub-harmonic oscillator. So in principle the incident noise has no effect on the phase noise of the divider outputs. Also as Ref. [9] shown ,the noise filtering network with the large capacitance C_2 could improve the phase noise performance of the sub-harmonic oscillator itself by almost 8dB as it suppresses the troublesome noise frequencies in the current source M3.

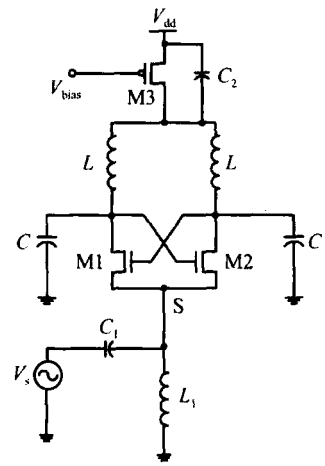

Fig. 2 Schematic of the proposed differential injection-locked frequency divider

In summary ,the proposed implementation of the injection locked technique could greatly improve the phase noise performance of the divider outputs. If the divider outputs are the desired carrier signals ,the lower phase noise would greatly improve the system performance. The cost of the proposed implementation is an extra noise filtering network (mainly an inductor L_1) and the large capacitance C_2. However , if the incident signal is from a LC oscillator (the main oscillator) ,which is most often the case ,the LC tank in the main oscillator can be used as the noise filtering network at the same time. This is due to the fact that the LC tank in the main oscillator also resonates at the twice the frequency of the divider outputs. Thus , the proposed implementation induces no extra cost except for the capacitance C_2. This will be described in detail in the following section.

3 Low phase noise quadrature oscillator

If a pair of differential incident signals is injected into two same sub-harmonic oscillators, four quadrature outputs could be generated at the sub-harmonic oscillator outputs. The differential incident signals are generated by an ordinary LC oscillator (we refer to as "main oscillator") which oscillates at twice the frequency of the quadrature outputs. The idea to generate quadrature carrier signals has been proposed in Ref. [10].

Using the proposed implementation of the injection locked technique and aforementioned method, we proposed a novel low phase noise quadrature oscillator, whose schematic is shown in Fig. 3.

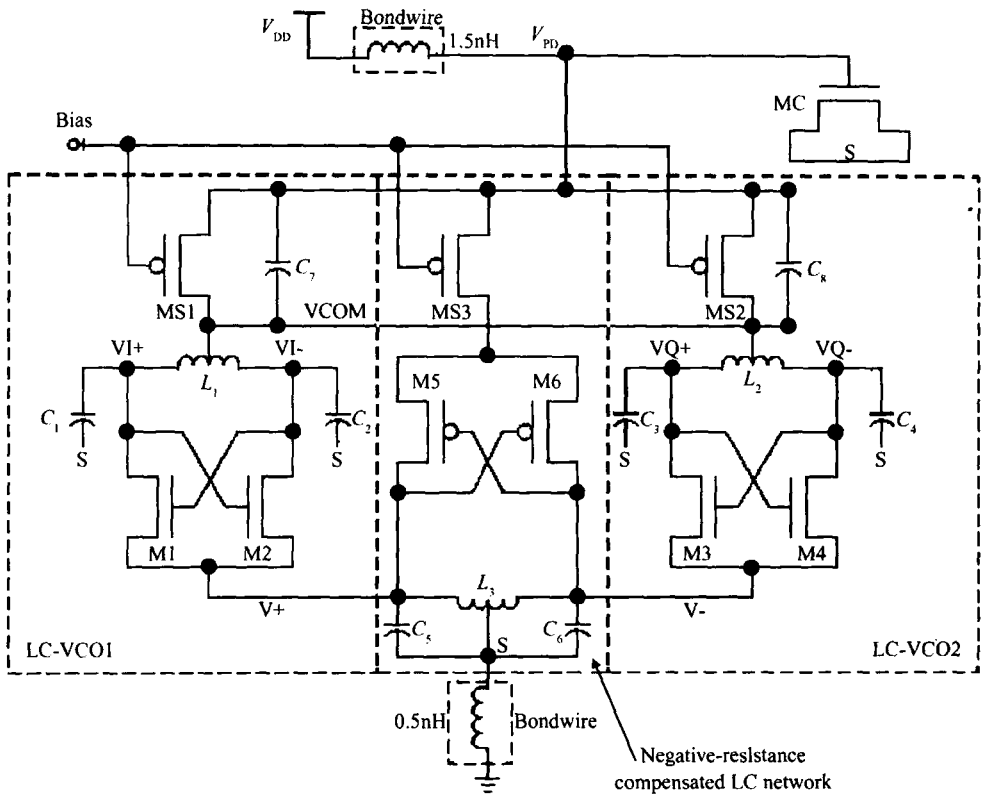

Fig. 3　Schematic of the proposed quadrature oscillator (output buffers are not shown)

MS3, M5, M6, L_3 and C_5, C_6 are the main oscillators which oscillate at twice the frequency of the quadrature outputs. L_3, C_5, and C_6 comprise the LC tank of the main oscillator. L_3 is a symmetrical spiral inductor with center-tap to keep the symmetry of the circuit, and resonates with the capacitance C_5/ C_6 and the parasitic capacitance at twice the frequency of the quadrature outputs. The cross-coupled pair M5 and M6 compensates the LC tank loss, and MS3 is the tail current source of the main oscillator.

The main oscillator generates the differential incident signals which directly inject into the common source connections (the node "V + " and "V - ") of two sub-harmonic oscillators (LV-CVO1 and LC-VCO2). The quadrature oscillating signals could be generated at the LV-CVO1 and LC-VCO2 outputs (the nodes "VI + ","VI - ", "VQ + "and "VQ - "). The sub-harmonic oscillators LC-VCO1 and LC-VCO2 are identical and consist of the cross-coupled pair (M1/ M2, M3/ M4) to compensate the LC tank loss, the on-chip symmet-

rical spiral inductors with center-tap (L_1, L_2), the on-chip MIM capacitor (C_1/C_2, C_3/C_4), the tail current sources (MS1, MS2), and the tail current source filtering capacitance (C_7, C_8).

One half of the inductor L_3, the capacitance C_5 (C_6), and the parasitic capacitance at the node V+ (V-) are simultaneously used as the noise filtering network for the sub-harmonic oscillator LC-VCO1 (LC-VCO2). This greatly improves the phase noise performance of the quadrature outputs as discussed in section 2.

Since only the quadrature outputs at the nodes VI+, VI-, VQ+ and VQ- are the desired signals and the noise performance of the main oscillator has no effect on the phase noise of the quadrature outputs (at least in principle). The main oscillator needs only to keeping oscillating and design optimization of the main oscillator is placed on the power consumption. The current consumed by the main oscillator can be designed to minimal specifications under the power consumption optimization. Furthermore, the sub-harmonic oscillators LC-VCO1 and LC-VCO2 are driven by the differential injected signals, so the oscillating startup safety consideration could be alleviated. The safety margin factor for the trans-conductance of the cross-coupled pairs (M1/M2, M3/M4) could also be reduced from three to a little greater than one. This would further lower the phase noise of the quadrature outputs or lower the power consumption.

The large capacitance C_7 and C_8 provide a low impedance for the high frequency noise and combine with the noise filtering networks to suppress the troublesome noise frequencies in the current sources (MS1 and MS2) making MS1 and MS2 noiseless to the sub-harmonic oscillators. If the capacitance of C_7 and C_8 is large enough, the node "VCOM" is nearly a common-mode node (virtual ground). So the center-taps of L_1 and L_2 could be connected to this same node "VCOM".

The dummy transistor MC provides a filtered capacitance (about 10pF) to reduce the ripple of the supply bus V_{PD}.

Four output buffers are added to drive the off-chip 50Ω loads. They are the ordinary common-source amplifiers and not shown in Fig. 4.

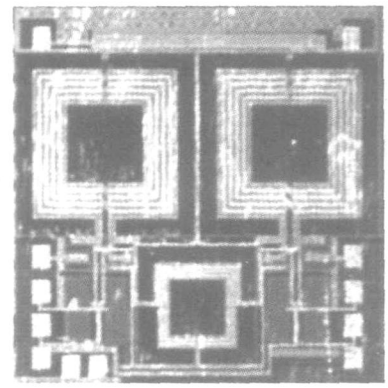

Fig. 4 Microphotograph of the proposed oscillator

4 Results

The proposed circuit has been implemented in 0.25μm CMOS process. Figure 4 shows the microphotograph of the proposed oscillator, and the die area is 1.2mm×1.0mm, most of which is occupied by three on-chip inductors. Two same symmetrical inductors with center-taps, L_1 and L_2, are laid out in metals 4 and 5 except that the cross-sections are laid out in metals 2 and 3. The symmetrical inductor L_3 is laid out in metals 3, 4, and 5 except that the cross-sections are laid out in metals 1 and 2. The inductors L_1, L_2 have an inductance of 17.6nH and a quality factor of 7.9, and the inductor L_3 has an inductance of 6.3nH and a quality factor of 10.6.

Figure 5 shows the measured output spectrum of the quadrature oscillator. The oscillating frequency is about 1.13GHz and the output power is about 5.3dBm. The simulated oscillating frequency is 1.2GHz and the difference may be due to the inaccurate inductor model.

Figure 6 shows the measured phase noise performance of the quadrature oscillator. The phase noise is -130dBc/Hz at 1MHz offset from 1.13GHz carrier, which is 6dB higher than the simulated results. The difference may be due to inaccurate inductor model and the device noise models.

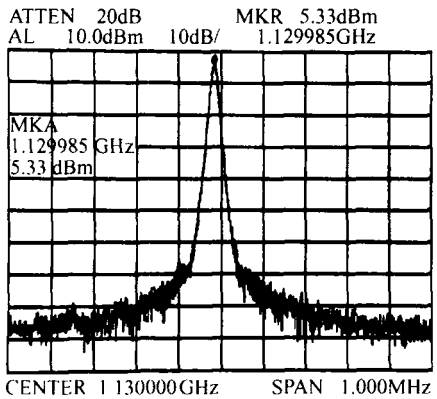

Fig. 5　Measured output spectrum of the quadrature oscillator

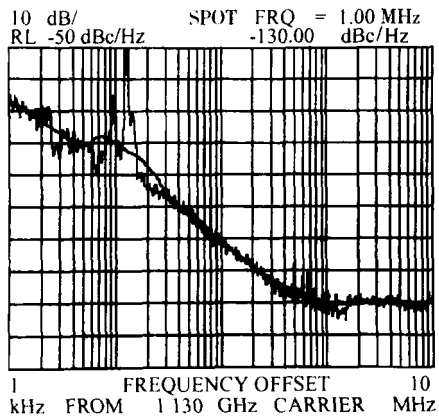

Fig. 6　Measured phase noise performance of the quadrature oscillator

The oscillator core draws 8. 0mA current from the 2. 5V power supply, so the FoM (figure of merit) of the proposed oscillator is

$$\mathrm{FoM} = 10\lg\left(\left(\frac{\omega}{\Delta\omega}\right)^2 \times \frac{1}{\Gamma(\Delta\omega)\ P}\right) \approx 209$$

where P is the power consumption. This FoM is comparable to the quadrature oscillators in Refs. [1, 3～5, 11, 12].

The phase accuracy of the quadrature oscillator is another important performance parameter. However, there are no effective methods to measure the phase error since the present oscillograph can not measure the phase error between two GHz signals. Although the indirect methods to measure the phase error between the quadrature signals exist, the results are not meaningful[5]. Since mixers were not integrated into the same chip, the indirect method could not be used.

5　Conclusion

In this paper, a low phase noise quadrature oscillator using the new injection locked technique is proposed. The new injection locked technique could improve the phase noise performance of the quadrature oscillator. The quadrature oscillator is implemented in 0. 25μm CMOS process. Measurements show the proposed oscillator could achieve comparable performance against prior technique.

References

[1] ElSayed A M, Elmasry M I. Low-phase-noise LC quadrature VCO using coupled tank resonators in a ring structure. IEEE J Solid-State Circuits, 2001, 36: 701

[2] Chi Baoyong, Shi Bingxue. Integrated 2. 4GHz CMOS quadrature VCO with symmetrical spiral inductors and differential varactors. IEEE RFIC Symposium, 2002: 451

[3] Van der Tang J, Van de Ven P, Kasperkovitz D, et al. Analysis and design of an optimally coupled 5-GHz quadrature LC oscillator. IEEE J Solid-State Circuits, 2002, 37: 657

[4] Vancorenland P, Steyaert M S J. A 1. 57GHz fully integrated very low-phase-noise quadrature VCO. IEEE J Solid-State Circuits, 2002, 37: 653

[5] Gierkink S L J, Levantino S, Frye R C, et al. A low-phase-noise 5-GHz CMOS quadrature VCO using superharmonic coupling. IEEE J Solid-State Circuits, 2003, 38(7): 1148

[6] Rategh H R, Lee T H. Super-harmonic injection locked oscillators as low power frequency dividers. Symp VLSI Circuits Dig, 1998: 132

[7] Rategh H R, Lee T H. Super-harmonic injection-locked frequency dividers. IEEE J Solid-State Circuits, 1999, 34(6): 813

[8] Rategh H R, Samavati H, Lee T H. A CMOS frequency synthesizer with an injection-locked frequency divider for a 5-GHz wireless LAN receiver. IEEE J Solid-State Circuits, 2000, 35(5): 780

[9] Hegazi E, Sjöland H, Abidi A A. A filtering technique to lower LC oscillator phase noise. IEEE J Solid-State Circuits, 2001, 36(12): 1921

[10] Chi Baoyong, Shi Bingxue. Low-power CMOS VCO with dual-band local oscillating signal outputs for 5/2. 5-GHz WLAN transceivers. Tsinghua Science and Technology, 2003, 8(2): 121

[11] Tiebout M. Low-power low-phase-noise differentially tuned quadrature VCO design in standard CMOS. IEEE J Solid-

State Circuits ,2001 ,36 :1018

[12] Andreani P. A low-phase-noise low-phase-error 1.8 GHz quadrature CMOS VCO. IEEE Int Solid-State Circuits Conf Dig Tech Papers ,San Francisco ,CA ,2002 :290

使用新注入锁定技术的低相位噪声正交振荡器 *

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摘要: 提出了一种利用新注入锁定技术的低相位噪声正交振荡器,激励信号直接注入子谐波振荡器的共源连接点.原理上,正交振荡器的相位噪声性能会比子谐波振荡器的相位噪声性能好.该正交振荡器已经采用 0.25μm CMOS 工艺实现,测试结果表明该正交振荡器的振荡频率约为 1.13 GHz,在偏离振荡频率 1M Hz 处的相位噪声约为 - 130dBc/ Hz.该振荡器采用 2.5V 电源电压,消耗的电流约为 8.0mA.

关键词: 振荡器; 射频; CMOS; 相位噪声

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