Analytical Modeling of Threshold Voltage for Double-Gate MOSFET Fully Comprising Quantum Mechanical Effects *

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Abstract: The analytical solutions to 1D Schrödinger equation (in depth direction) in double-gate (DG) MOSFETs are derived to calculate electron density and threshold voltage. The non-uniform potential in the channel is concerned with an arbitrary depth so that the analytical solutions agree well with numerical ones. Then, an implicit expression for electron density and a closed form of threshold voltage are presented fully comprising quantum mechanical (QM) effects. This model predicts an increased electron density with an increasing channel depth in subthreshold region or mild inversion region. However, it becomes independent on channel depth in strong inversion region, which is in accordance with numerical analysis. It is also concluded that the QM model, which barely considers a box-like potential in the channel, slightly over-predicts threshold voltage and underestimates electron density, and the error increases with an increasing channel depth or a decreasing gate-oxide thickness.

Key words: DG MOSFET; 1D analytical QM solution; non-uniform potential in channel-depth direction; electron density; threshold voltage; channel depth

PACC: 7340Q; 6185; 0300

CLC number: TN304.02 **Document code:** A **Article ID:** 0253-4177(2005)03-0429-07

1 Introduction

DG-MOSFET has been considered one of the most promising candidates for the channel length beyond 65nm regime[1~5] in place of current MOSFET due to the electrostatic concern (i.e., off-state leakage current). Compact analytical modeling is thus desirable in anticipation of technology maturity. Extensive works have been done on this field[6~12]. However, they all focus on electrostatic analysis, thus ignoring quantum mechanical (QM) effects that are indispensable in the range of deca-nano scale. In Ref. [13], QM effects do be considered but a box-like potential in the channel is assumed, which is insufficient for the channel depth larger than 10nm according to the comparison with numerical simulation.

In this work, the analytical solutions to the eigen-energy levels are derived with the consideration of non-uniform potential in the channel. Then, an implicit expression for electron density and a closed form of threshold voltage for DG-MOSFETs are presented fully comprising QM effects. The analytical values of eigen-energy levels, electron densities, and threshold voltages with arbitrary device parameters agree well with the numerical results.

2 Analytical eigen-energies with non-uniform potential

The structure of the DG-MOSFET is depicted

* Project supported by National High Technology R&D Program of China (No. 2003AA1Z1370)

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Received 7 September 2004, revised manuscript received 12 November 2004

in Fig. 1. In our notation, the channel depth is d and the gate-oxide (both front and back) is t_{ox}. As far as electron surface density or threshold voltage is concerned, especially with the consideration of QM effects, one may focus on 1D analysis along the depth direction, i. e. z-direction in Fig. 1 (the effects along the channel is not the keystone this paper addresses, and there has been active work on Refs. [11, 12]). To calculate electron surface density, the eigen-energy levels in the potential well along z-direction need to be obtained. According to numerical simulations, they shift with different depths. In Fig. 2, two diagrams are plotted qualitatively to show different situations of energy levels in the potential well with different depths. As it is seen in the figure, the energy levels are above the electric potential energy in the well when the channel is narrow. However, they go beneath the central point of the electric potential energy with an increasing depth. Our task is to analytically calculate these energy levels with an arbitrary depth.

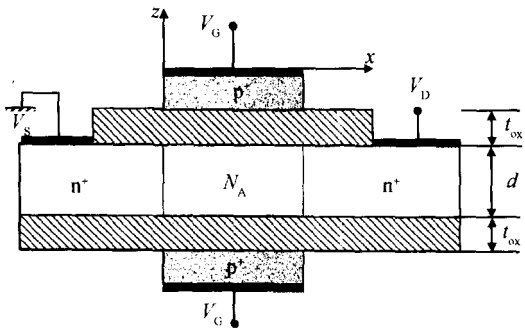

Fig. 1 DG-MOSFET cross-section with p^+ poly-silicon double-gate and n^+ drain/source regions The channel depth is d and the gate-oxide (both front and back) is t_{ox}. z is the direction along depth while x is the direction along channel.

If the assumption of a box-like potential in the channel (ignoring the non-uniform potential) and infinitely high potential barriers at the silicon/oxide interfaces along the z-direction is made, the following analytical solutions to energy levels, $E_{n,k}$, are derived

$$E_{n,k\text{-squ}} = E_{c0} + \frac{n^2\pi^2\hbar^2}{2m^*_{z,k}d^2} \qquad (1)$$

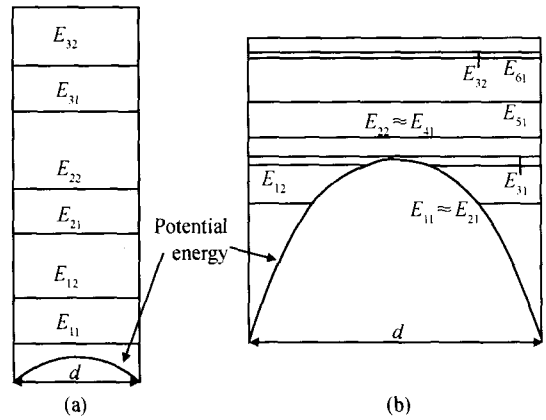

Fig. 2 Qualitative diagrams of energy levels in the potential well along the depth direction A narrower depth is assumed on the left while a wider depth is on the right.

where n is the quantum number, k refers to different valleys of the silicon conduction band, ‘squ’ indicates the energy levels are for square potential well, E_{c0} is the value of the central point of potential well, and $m^*_{z,k}$ is the effective mass along z-direction of valley k with $m^*_{z,1} = m_l^* = 0.916m_0$ and $m^*_{z,2} = m_t^* = 0.19m_0$ (the subscript 1 referring to unprimed valley and 2 referring to primed valley for a silicon crystal with 〈100〉 orientation, m_l^* the longitudinal mass, m_t^* the transverse mass, and m_0 the free electron mass). This formula, however, is not sufficiently correct with a wide channel or a high gate bias because under these situations the non-uniformity of the electric potential along the depth cannot be neglected. Therefore, to make it more practical, the first-order correction to the energy levels using the time-independent perturbation theory is applied with a perturbation potential energy $\delta H = q^2\rho z^2/2\varepsilon_{Si}$ where ε_{Si} is silicon permittivity and $\rho = -(N_e + N_a - N_d)/d$ is the average space charge density within the potential well with N_e the electron density per unit area, N_a the acceptor density per unit area and N_d the donor density per unit area. Thus, we find first-order corrections[13]

$$\delta E_{n\text{-squ}} = \frac{q^2\rho d^2}{24\varepsilon_{Si}}\left(1 - \frac{6}{(n\pi)^2}\right) \qquad (2)$$

In Fig. 3, different energy levels ($n = 1, 2$) of different valleys ($k = 1, 2$) are depicted against different

channel depth and in Fig. 4 they are depicted against different average space charge density (this is equal to be under different gate bias). Squared symbols represent the analytical solutions using Eq. (1) plus Eq. (2) while round symbols stand for numerical results. As one can clearly see from the figures, if the channel is narrow (approximately narrower than 15nm) or the space charge density is low (approximately lower than $10^{18}\mathrm{cm}^{-3}$), the analytical solutions with the assumption of a square potential well plus the first-order perturbation correction agree well with the numerical ones. However, if the channel is wider or the space charge density is higher, the errors between these two become intolerant. The reason for this is that the potential energy in the channel can no longer be regarded as perturbation. Therefore, other analytical mean needs to be found for these cases.

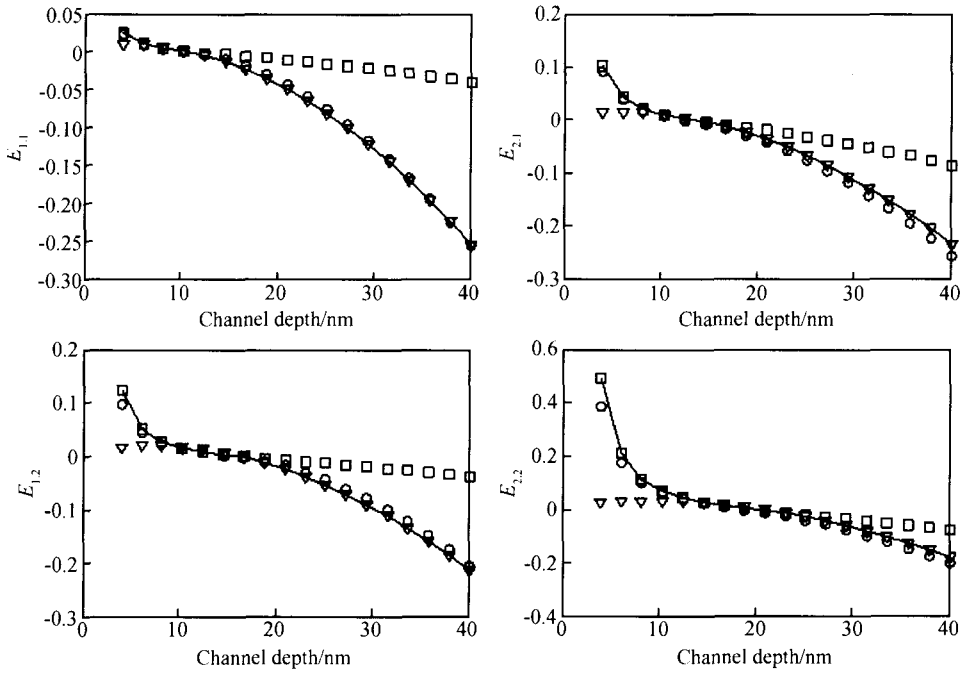

Fig. 3　Energy levels $E_{n,k}$ versus channel depth ($\rho = 10^{18}\mathrm{cm}^{-3}$)　Rounds represent numerical results, solid lines represent analytical results E_{n,k_ana}, squares represent analytical results E_{n,k_squ} with first-order perturbation, and triangles represent analytical results E_{n,k_tri}.

Note that DG-MOSFET tends to be two back-against-back independent MOSFETs if channel becomes wider or space charge density gets higher. Consequently, the potential in the channel tends to be split into two independent parabola-like deep potential wells as in the MOS structure. In earlier works, the approximate solutions to energy levels for MOS structure using triangle potential well are proved to be reasonable both in subthreshold region[14] and in strong inversion region[15]. Hence, we investigate the applicability of these approximate solutions for DG-MOSFET. The expressions are listed below.

$$E_{n,k\_\mathrm{tri}} = E_{c0} + \left(\frac{\hbar^2}{2m^*_{z,k}}\right)^{1/3} \times \left[\frac{3}{2}\pi qF_s\left(n+\frac{3}{4}\right)\right]^{2/3} + \frac{q^2\rho(d/2)^2}{2\varepsilon_{Si}} \quad (3)$$

where 'tri' denotes that the energy levels are for triangle potential well and $F_s = q(\eta N_e + N_a - N_d)/\varepsilon_{Si}$ is the surface electric field. Here, η, an empirical parameter, differs for different device structures as discussed in Ref. [15] and for our case $\eta = 0.25$. In Figs. 3 and 4, the triangle symbols represent E_{n,k_tri}. As it is seen in the figures, the analytical solutions with the triangle well tally with numerical ones with wide channel or high space charge density. Furthermore, if E_{n,k_squ} are away a-

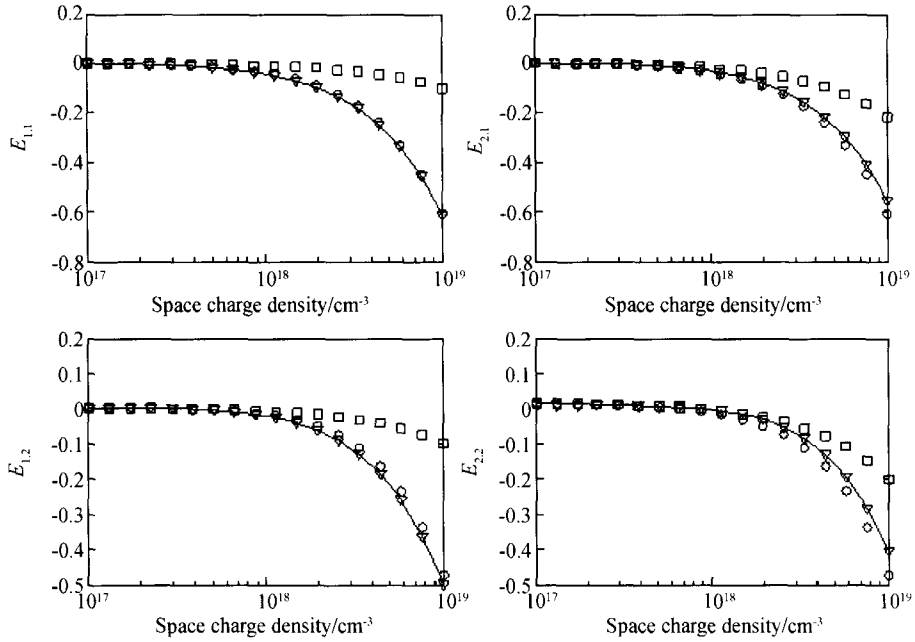

Fig. 4 Energy levels $E_{n,k}$ versus average space charge density (d = 20nm) Rounds represent numerical results, solid lines represent analytical results E_{n,k_ana}, squares represent analytical results E_{n,k_squ} with first-order perturbation, and triangles represent analytical results E_{n,k_tri}.

bove zero, they accord with numerical ones since this corresponds to the case of narrower depth or lower space charge density and if E_{n,k_squ} are away below zero, E_{n,k_tri} accord with numerical ones since this corresponds to the case of wider depth or higher space charge density. To include all cases, the strategy in Fig. 5 is used to obtain the final analytical solutions E_{n,k_ana} for an arbitrary depth. The solid lines both in Figs. 3 and 4 stand for E_{n,k_ana}, which are in accordance with numerical results with an arbitrary depth or space charge density (meaning the analytical solutions are effective under all gate bias).

If $E_{n,k\_squ} < E_{n,k\_tri}$
then $E_{n,k\_ana} = E_{n,k\_squ}$
Else if $E_{n,k\_squ} > 0$
then $E_{n,k\_ana} = E_{n,k\_squ}$
Else
then $E_{n,k\_ana} = E_{n,k\_tri}$

Fig. 5 Strategy for obtaining analytical energy levels from the combination of E_{n,k_squ} and E_{n,k_tri}

3 Electron density and threshold voltage

Due to the confinement of electron motion normal to the interface, the conduction band within the transistor channel is split into several subbands, each of which is associated with the corresponding energy eigenvalue. Hence, the electron surface density may be expressed as

$$N_e = \sum_{n=1}^{N_t}\sum_{k=1}^{N_m} g_k N_k \lg\{1+\exp[(E_{n,k} - E_{c0})/k_B T] \times \exp[q(\phi_c - \phi_{Fn})/k_B T]\} \quad (6)$$

where $N_k = (m_{dk}^* k_B T)/(\pi\hbar^2)$ is the density of states in the subband at energy $E_{n,k}$, m_{dk}^* is the density of states effective mass ($m_{d1}^* = m_t^*$, $m_{d2}^* = (m_l^* m_t^*)^{1/2}$), $N_t = 10$ is the number of subbands, $N_m = 2$ is the number of different sets of valleys, $g_1 = 2$, $g_2 = 4$ is the degeneracy of the valleys of set, $\phi_c = -E_{c0}/q$, $\phi_{Fn} = -E_{Fn}/q$ with E_{Fn} the quasi-Fermi level, k_B is the Boltzmann constant, and T is the temperature. On the other hand, according to 1D electrostatic analysis, the electron density may be al-

so expressed as[13]

$$N_e = 2C_g(V'_G - \phi_c)/q \qquad (7)$$

where $C_g = C_{ox}C_d/(C_{ox} + C_d)$ represents the gate capacitance per unit area with $C_{ox} = \varepsilon_{ox}/t_{ox}$ the oxide capacitance per unit area and $C_d = 4\varepsilon_{Si}/d$ is the depletion capacitance per unit area. $V'_G = V_G - (\phi_M - \chi + V_A - V_D)$ is the effective gate voltage with V_G the gate bias, ϕ_M the work function of the gate material, χ the electron affinity of the semiconductor, $V_A = qN_a/2C_g$ and $V_D = qN_d/2C_g$. Equating Eq. (6) and Eq. (7), the implicit analytical form of electron density is obtained with a given gate bias[13]. Different from Ref. [13], the analytical solutions to $E_{n,k}$ introduced in this paper, i. e. E_{n,k_ana}, are substituted into Eq. (6). In Fig. 6, the analytical electron surface densities are depicted against gate voltage with different channel depths, agreeing well with the numerical simulation results (executed using Schred 2. 0[16], a 1D Schrödinger-Poisson-equation self-consistent solver). According to our model's prediction, an increase of the gate voltage results in a weaker influence of the channel depth on the electron density. The electron density increases with an increasing channel depth in subthreshold region or mild inversion region while it becomes independent on channel depth in strong inversion region. This results from a decrease of the average distance of electrons from the surfaces with an increase of the surface potential, similarly as in the conventional bulk MOS transistor[17]. The QM model, which merely considers a box-like potential in the channel (strategy used in Ref. [13]), underestimates electron density and the trend that it decreases with an increasing channel depth is inappropriate according to numerical results. In Fig. 7, the electron densities are depicted against gate voltage with different gate-oxide thickness. From the figure, our model tallies well with numerical results while the box-like potential well assumption vastly underestimate values and the error becomes larger with a decreasing gate-oxide thickness.

Finally, a closed form of the threshold voltage is about to be presented. From Eq. (6), the semi-

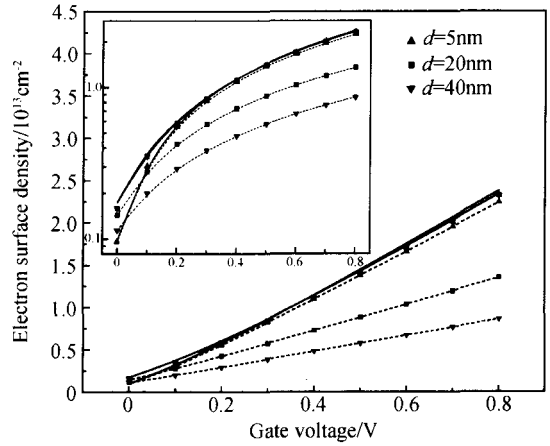

Fig. 6　Electron surface density versus gate voltage with different channel depths both on linear scale (right) and logarithmic scale (left)　t_{ox} = 1nm　Symbols stand for numerical results, solid lines stand for analytical results fully comprising QM effects, and dashed lines with symbols represent analytical results with the box-like-potential assumption.

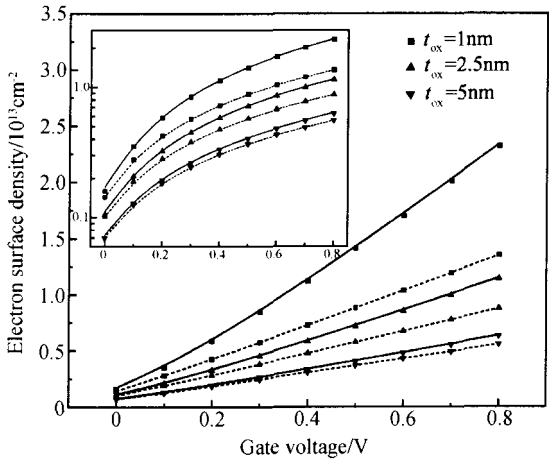

Fig. 7　Electron surface density versus gate voltage with different gate-oxide thickness both on linear scale (right) and logarithmic scale (left)　d = 20nm　Symbols stand for numerical results, solid lines stand for analytical results fully comprising QM effects, and dashed lines with symbols represent analytical results with the box-like-potential assumption.

conductor capacitance C_s may be derived as (using Boltzmann statistics)[13]

$$C_s = q\frac{dN_e}{d\phi_c} = \frac{q^2 N'_c}{k_B T}\exp[q(\phi_c - \phi_{Fn})/k_B T] \qquad (8)$$

where $N'_c = \sum_n^{N_t}\sum_k^{N_m} g_k N_k \exp[(E_{n,k\_ana} - E_{c0})/k_B T]$

is the effective density of states. Then, we define the device threshold as the gate voltage at which C_s equals $2C_g$ (more specifically, see Ref. [13]). Therefore, the threshold voltage V_{th} is finally obtained as

$$V_{th} = \phi_M - \chi + V_A - V_D + \frac{k_B T}{q} \lg\left[\frac{2 C_g k_B T}{q^2 N_c'(V_{th0})}\right] \tag{9}$$

Here $N_c'(V_{th0})$ indicates the energy levels, which is used to calculate N_c' and obtained under the gate voltage of V_{th0} (V_{th0} is derived from the similar form of Eq. (9), but uses energy levels with box-like potential well, thus independent of gate voltage, to calculate N_c'). In Fig. 8, V_{th} is plotted against channel depth with different gate-oxide thickness. It is concluded from the figure that the threshold voltage decreases with an increasing channel depth or gate-oxide thickness. The model merely with the box-like-potential slightly overestimates the values of the threshold voltage.

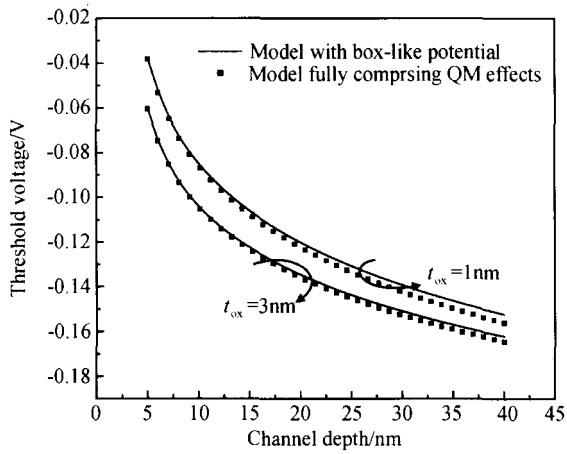

Fig. 8 Threshold voltage versus channel depth with different gate-oxide thickness

4 Conclusion

Analytical modeling for deca-nano scaled DG-MOSFETs is desirable for circuit designers. Electrons in the channel are severely confined along the channel depth under such small scale so that the QM effects must be modeled. Previous works either ignore QM effects or make too coarse assumptions of the quantum potential well.

In this paper, the non-uniform potential in the channel is considered. A closed form of energies levels for an arbitrary depth and space charge density is presented. Then, an implicit form of the electron density and a closed form of the threshold voltage are proposed, which utilize the analytical solutions to energy levels.

According to the model's prediction, the following conclusion may be made: an increased electron density with an increasing channel depth in subthreshold region or mild inversion region. However, it becomes independent on channel depth in strong inversion region. It is also concluded that the QM model, which barely considers a box-like potential in the channel, slightly over-predicts threshold voltage and underestimates electron density and the error increases with an increasing channel depth or a decreasing gate-oxide thickness. This indicates that the full comprising of QM effects is indispensable for practical DG-MOSFETs (with channel depth of deca-nano scale).

References

[1] http://public.itrs.net

[2] Suzuki K, Tanaka T, Tasaka Y, et al. Scaling theory for double-gate SOI MOSFETs. IEEE Trans Electron Devices, 1993, 40: 2326

[3] Frank D J, Taur Y, Wong H. Generalized scale length for two-dimensional effects in MOSFETs. IEEE Electron Device Lett, 1998, 19: 385

[4] Frank D J, Laux S E, Fischetti M V. Monto Carlo simulation of a 30nm dual-gate MOSFET: how short can Si go. Digest of IEDM, 1992: 553

[5] Balestra F. Comments, with reply, on double-gate operation and volume inversion in n-channel SOI MOSFET's. IEEE Electron Device Lett, 1992, 13: 658

[6] Suzuki K, Tanaka T, Tosaka Y, et al. Analytical surface potential expression for thin-film double-gate SOI MOSFET's. Solid-State Electron, 1994, 37: 327

[7] Suzuki K, Sugii T. Analytical models for n^+-p^+ double-gate SOI MOSFET's. IEEE Trans Electron Devices, 1995, 42: 1940

[8] Suzuki K, Tosaka Y, Sugii T. Analytical threshold voltage model for short channel n^+-p^+ double-gate SOI MOSFET's. IEEE Trans Electron Devices, 1996, 43: 732

[9] Pei Gen, Ni Weiping, Kammula A, et al. A physical compact model of DG MOSFET for mixed-signal circuit applications-Part Ⅰ: model description. IEEE Trans Electron Devices, 2003, 50(10): 2135

[10] Pei Gen, Kan E. A physical compact model of DG MOSFET for mixed-signal circuit applications-Part Ⅱ: parameter extraction. IEEE Trans Electron Devices, 2003, 50(10): 2144

[11] Chen Qiang, Harrell E, Meindl J. A physical short-channel threshold voltage model for undoped symmetric double-gate MOSFETs. IEEE Trans Electron Devices, 2003, 50(7): 1631

[12] Liang Xiaoping, Taur Yuan. A 2-D analytical solution for SCEs in DG MOSFETs. IEEE Trans Electron Devices, 2004, 51(9): 1385

[13] Baccarani G, Reggiani S. A compact double-gate MOSFET model comprising quantum-mechanical and nonstatic effects. IEEE Trans Electron Devices, 1999, 46(8): 1656

[14] Ma Yutao, Li Zhijian, Liu Litian. Quantum mechanical effects correction to MOS threshold voltage comprising multi-subband structure. Chinese Journal of Semiconductors, 1999, 20(3): 219(in Chinese) [马玉涛, 李志坚, 刘理天. 包含多子带结构的 MOS 器件开启电压量子力学效应修正模型. 半导体学报, 1999, 20(3): 219]

[15] Ma Yutao, Liu Litian, Yu Zhiping, et al. Validity and applicability of triangular potential well approximation in modeling of MOS structure inversion and accumulation layer. IEEE Trans Electron Devices, 2000, 47(9): 1764

[17] http://www.nanohub.purdue.edu/NanoHub/

[18] Majkusiak B, Janik T, Walczak J. Semiconductor thickness effects in the double-gate SOI MOSFET. IEEE Trans Electron Devices, 1998, 45(5): 1127

考虑量子效应的双栅 MOSFET 的阈电压解析建模 *

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摘要: 推导了双栅 MOSFET 器件在深度方向上薛定谔方程的解析解以求得电子密度和阈电压. 该解析解考虑了任意深度情况下沟道中深度方向上电势的不均匀分布,结果与数值模拟吻合. 给出了电子密度的隐式表达式和阈电压的显式表达式,它们都充分考虑了量子力学效应. 模型显示,在亚阈值区或者弱反型区,电子密度随深度增加而增加;然而,在强反型区,它与深度无关,这与数值模拟的结果吻合. 结果进一步显示,只考虑方形势阱的量子力学结果,略高估计了阈电压,且低估了电子密度. 误差随着深度的增加或者栅氧厚度的减少而增加.

关键词: 双栅 MOSFET; 一维解析量子求解; 沟道深度方向的非均匀电势; 电子密度; 阈电压; 沟道深度

PACC: 7340Q; 6185; 0300

中图分类号: TN304.02　　**文献标识码**: A　　**文章编号**: 0253-4177(2005)03-0429-07

*国家高技术研究发展计划资助项目(批准号:2003AA1Z1370)

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2004-09-07 收到,2004-11-12 定稿