A Novel Local-Dielectric-Thickening Technique for Performance Improvements of Spiral Inductors on Si Substrates *

Yang Rong , Li Junfeng , Zhao Yuyin , Chai Shumin , Han Zhengsheng , and Qian He

(*Institute of Microelectronics , Chinese Academy of Sciences , Beijing* 100029 , *China*)

Abstract : A novel local-dielectric-thickening technique is presented for performance improvements of Si-based spiral inductors. This technique employs the processes of deposition ,photolithography ,and wet-etching ,to locally thicken the oxide layer under the inductor ,which can decrease the substrate loss and improve the inductor performance. Both the structures and processes are compact ,economical ,and compatible with CMOS processing. Several square spiral inductors with different inductances are fabricated ,and the quality factors and the self-resonant frequencies both increase clearly with this proposed technique :for the 10nH ,5nH ,and 2nH inductors ,the peak quality factors are effectively improved by 46. 7 % ,49. 7 % ,and 68. 6 % ,respectively ;however ,the improvement percents of the self-resonant frequencies are more significant ,which are 92. 1 % ,91. 0 % ,and no less than 68. 1 % respectively.

Key words : silicon ; inductor ; structure ; process ; quality factor ; self-resonant frequency
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1 Introduction

In recent years ,the high performance integrated inductor on lossy Si-substrates , has become a very challenging issue in the booming RF CMOS technology[1~3] . Unlike the RF performance of MOSFET improving with scaling-down ,the quality-factors of inductors ,i. e. *Q* 's ,are always limited by the degradation resulting from energy dissipation in the semiconducting substrates[4] . In order to improve *Q*-factors ,many methods were proposed to reduce the substrate loss : the patterned ground shields[4] improved *Q* 's effectively , but decreased self-resonant frequencies (f_{sr} 's) due to their additional parasitic capacitance ;the MEMS engineering in substrates[5] could indeed raise *Q* 's tremendously ,however ,there were many issues such as compatibility ,cost , reliability , etc ;as for the substrate p-n junction isolation against the eddy current under the inductor[6] ,ion implantors with high-energy and large-beam-current are indispensable , and the diffusion time is almost unacceptable.

In this paper ,a novel compact local-dielectric-thickening technique has been developed to improve *Q* 's and to avoid the issues in the above-mentioned methods. This technique locally thickens the oxide thickness under the inductor using the processes of deposition ,photolithography ,and wet-etching ,which is a very effective technique with acceptable process cost and time. Both the quality-factors and the self-resonant frequencies can be improved significantly with this technique.

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Yang Rong male ,was born in 1976 ,PhD candidate. He is currently studying RF CMOS technology.
Li Junfeng male ,was born in 1973 ,associate professor. He is currently studying VLSI technology.
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2 Structures and fabrication

Spiral inductors are the most feasible and widely used integrated inductors because of their compatibility with IC processing. The spiral inductor is usually composed of the top metal spiral and the center-tap underpass using a lower metal layer, whose layout is shown in Fig. 1. The layout parameters are the number of turns (n), the line width (w), the line spacing (s), the outer dimension (od) and the inner dimension (id), which plus process parameters determine the electrical behavior of the inductor. In low frequencies, when the substrate effects and the metal eddy current can be neglected, the inductance (L) of a square spiral inductor can be regarded as the function of the layout parameters, formulated as[7]

$$L = 2.34\mu_0 \frac{n^2 \frac{\text{od} + \text{id}}{2}}{1 + 2.75 \frac{\text{od} - \text{id}}{\text{od} + \text{id}}} \quad (1)$$

where μ_0 is the vacuum permeability.

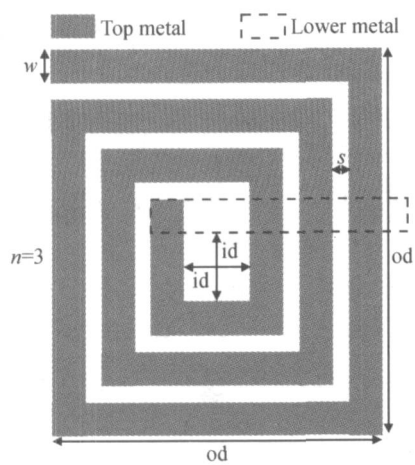

Fig. 1 Layout of a 3 turn square spiral inductor

However, a real spiral inductor on Si substrates does not only provide inductance, whose parasitic capacitance and resistance must be taken into account. Hence a compact physical model of the spiral inductor[1] can be depicted as Fig. 2, where L is for the inductance that we expect, R_s for the series resistance of metal line, C_p for the shunt capacitance between the main spiral and the center-tap, C_{ox} for the capacitance between the spiral and the substrate, and C_{Si}, R_{Si} for the substrate parasitic capacitance, resistance, respectively.

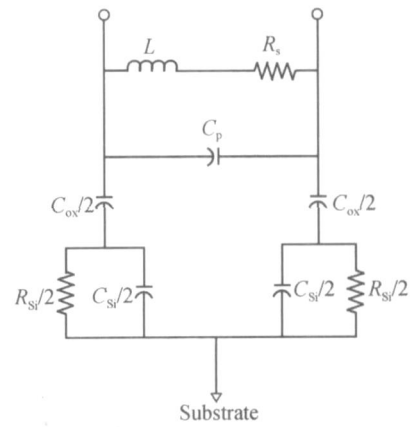

Fig. 2 Model for a spiral inductor on silicon[1]

Additional to the inductance, two key performance parameters of the inductor are the quality factor (Q) and the self-resonant frequency (f_{sr}), which represent how close the inductor approximates an ideal one and in what frequency range it can work as an inductive component, respectively. Q is defined as

$$Q = 2\pi \frac{\text{energy stored}}{\text{energy loss in one oscillation cycle}} \quad (2)$$

With the frequency rising, Q degrades because the energy dissipation in the semiconducting substrate increases. Then f_{sr} can be defined as the frequency when Q (or L) drops to zero. Thus, reducing the energy loss in the substrate will be an effective way to improve Q and f_{sr}. It is clear that one could serve the purpose by thickening the oxide thickness (t_{ox}). Theoretically, the thicker the oxide is, the more favorable it is for the on-chip inductor; however, an excessively thick oxide layer is unacceptable when considering active devices and interconnection structures: for LOCOS (local oxidation of silicon) or STI (shallow trench isolation), the thick oxide results in excess strain or loss in active areas; for PMD (pre-metallization-dielectric), it brings about difficulties in the contact hole etching and the electrode formation; for ILD (interlayer dielectric), it is unfavorable for vias and metal-insu-

lator-metal (MIM) capacitors. Fortunately, the dilemma can be avoided by the local thickening of the dielectric under the inductor, with an additional photolithography mask. Such an idea originally came from Ref. [8]: etching-back in the Si substrate under the inductor and local-dielectric-thickening with thermal oxidation using similar LOCOS fundamentals, which proved effective in *Q*-improvement, but these complicated steps did expend too much process time and cost.

This paper has developed an improved technique for local-dielectric-thickening, whose schematic structures are shown in Fig. 3. The processes for this technique are very compact and compatible with CMOS processing: after the LOCOS (or STI) processing, a CVD (chemical vapor deposition) SiO_2 layer was deposited, whose thickness was optional from 1μm to 3μm; then the CVD SiO_2 layer outside the local thickening area shown in Fig. 3 was selectively removed by BOE (buffered oxide etching) solution, with the local thickening area covered by photoresist; finally the photoresist was removed and the local-thickening region for the inductor was accomplished. It should be stated that wet-etching is more preferable and the additional dimension (*a*) is indispensable when etching the CVD SiO_2. Wet-etching results in a sloping sidewall instead of a steep one, which is favorable for interconnection. When the lateral etching is taken into account, the masked region (the local thickening area) must be larger than the spiral area (the inductor area), and it is proposed that *a* should be no less than 5μm. Since the metal line connected to the inductor is usually wide (typically $w > 10\mu m$), such a height of the CVD SiO_2 mesa (1～3μm) would not be a risk in metallization processing. When compared with the method proposed in Ref. [8], this technique could save many process steps, therefore it has many advantages in process cost, time, and reliability. What's more, this local-dielectric-thickening technique is also feasible for polygonal or circle spiral inductors, although it was originally developed for a square one.

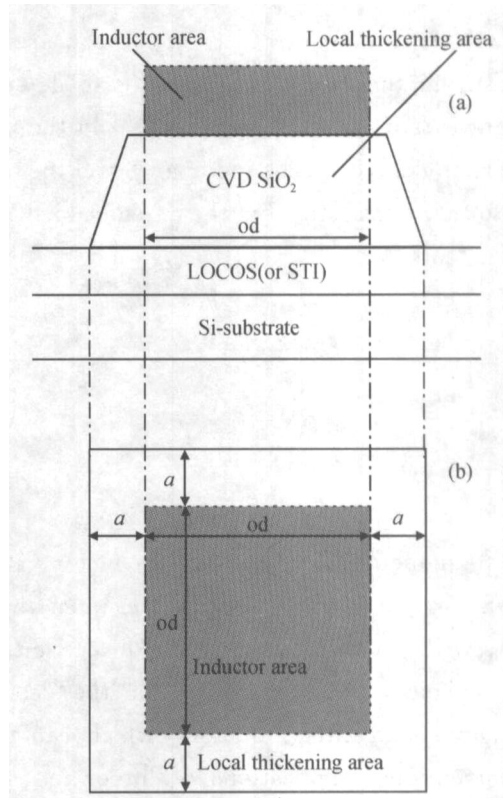

Fig. 3　Schematic structures for local-dielectric-thickening under inductors　(a) Cross section; (b) Top view

Following these process steps, several square spiral inductors were fabricated in the same Si substrate featuring p (100) and 20Ω·cm, and some control inductors without local-dielectric-thickening were also fabricated. A two-layer-aluminum technology was employed with LOCOS isolation. The thicknesses of LOCOS, PMD, metal-1, ILD, metal-2 are 0.5μm, 0.7μm, 0.6μm, 1μm, 2μm, respectively. The layout parameters are determined according to Formula (1) to attain a certain inductance value.

3　Results and discussion

RF *S*-parameters (from 100MHz to 20GHz) were measured with a HP8510C vector network analyzer and a Cascade Microtech Summit 9000 probe station with ground-signal-ground (GSG) pattern probes. An open pad structure, identical to the one that the inductor is connected to, including all the metal paths that are needed to reach the spiral, is placed near the device under test (DUT) in

the layout. The *Y*-parameters (converted from the measured *S*-parameters) of the open pad are subtracted from those of DUT in order to de-embed the parasitics inserted by the probes and the pads, in a certain degree[3]. The inductance and the quality factor are extracted from the de-embedded *Y*-parameters as follows[9],

$$L = \frac{\mathrm{Im}(\frac{1}{y_{11}})}{2\pi f} \tag{3}$$

$$Q = \frac{\mathrm{Im}(\frac{1}{y_{11}})}{\mathrm{Re}(\frac{1}{y_{11}})} \tag{4}$$

The inductance and the quality factor varying with the frequency are compared between the inductors with and without the local-dielectric-thickening technique (See Fig. 4). For the designed 10nH, 5nH, and 2nH inductors, which can cover the conventional applications of integrated spiral inductors, the performance improvements resulting from the local-dielectric-thickening technique are all significant: all the peak Q's increase and occur at higher frequencies, which means the inductors can operate at higher frequencies for a given Q; the L-f curves become flatter, and the measured L's are also closer to the designed ones according to Formula (1), which is favorable for circuit design and may be explained from the fact that the substrate effects on the inductance are slighter with thicker oxide; it is also favorable that f_{sr} (where L drops to zero) increases clearly for each inductor, which means that the range of operation frequency is extended to higher frequency bands. All these quality factors and self-resonant frequencies of the inductors with and without the local-dielectric-thickening technique are compared in Table 1, and the efficiencies of this technique are evaluated by calculating improvement percents. For the 10nH, 5nH, and 2nH inductors, Q_{max} improvements are 46.7%, 49.7%, and 68.6% respectively, which seems that the Q-improvement degrades with the inductance rising. More significant and steady f_{sr} improvements can also be observed for all these inductors in the same table. Therefore, one could draw a conclusion that for the most widely used nH-level integrated spiral inductors, both Q- and f_{sr}- improvements resulting from the proposed local-dielectric-thickening technique are considerable. However, in this study, the oxide under the inductors only be thickened by 1.5μm; it seems possible that more significant performance improvements can be expected with a thicker oxide.

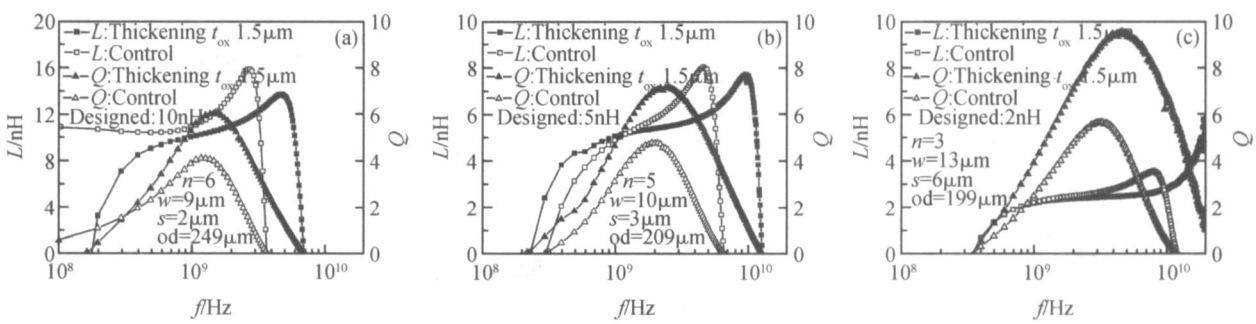

Fig. 4 Inductance and quality-factor varying with frequency of 10nH (a), 5nH (b), and 2nH (c) inductors

Table 1 Comparison of the quality factors and the self-resonant frequencies between the inductors with and without the local-dielectric-thickening technique

	2nH inductor		5nH inductor		10nH inductor	
	Q_{max}	f_{sr}/ GHz	Q_{max}	f_{sr}/ GHz	Q_{max}	f_{sr}/ GHz
With this proposed technique	9.54	> 20 *	7.17	12.8	6.06	7.30
Without this proposed technique	5.66	11.9	4.79	6.7	4.13	3.80
Improvement	68.6%	> 68.1%	49.7%	91.0%	46.7%	92.1%

*Beyond the measurement range 1～20GHz

4 Summary

A novel compact local-dielectric-thickening technique has been proposed to improve the performance of spiral inductors on Si substrates in this paper. The structures and processes for this technique are also described in detail. Several square inductors are fabricated using this technique and show significant improvements in both the quality factors and the self-resonant frequencies. Such a technique is promising in performance improvements for Si-based spiral inductors.

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References

[1] Thomas L H. The design of CMOS radio-frequency integrated circuits. Cambridge :Cambridge University Press ,1998

[2] Burghartz J N ,Rejaei B. On the design of RF spiral inductors on silicon. IEEE Trans Electron Devices ,2003 ,50(3) :718

[3] Koutsoyannopoulos Y ,Papananos Y. Systematic analysis and modeling of integrated inductors and transformers in RF IC design. IEEE Trans Circuits Syst Ⅱ:2000 ,47(8) :699

[4] Yue C P ,Wong S S. On-chip spiral inductors with patterned ground shields for Si-based RF ICs. IEEE J Solid-State Circuits ,1998 ,33(5) :743

[5] Long Haibo ,Zhang Yaojiang ,Feng Zhenghe. Enhancement of quality factor in RF-MEMS spiral inductors by etching out substrate. 3rd International Conference on Microwave and Millimeter Wave Technology ,2002 :1166

[6] Liu Chang ,Chen Xueliang ,Yan Jinlong. Novel substrate pn junction isolation for RF integrated inductors on silicon. Chinese Journal of Semiconductors ,2001 ,22(12) :1486

[7] Mohan S S ,Del Mar Hershenson M ,Boyd S P ,et al. Simple accurate expressions for planar spiral inductances. IEEE J Solid-State Circuits ,1999 ,34(10) :1419

[8] Tan Y ,Kumar M ,Cai Jun ,et al. A SOI LDMOS technology compatible with CMOS ,BJT ,and passive components for fully-integrated RF power amplifiers. IEEE Trans Electron Devices ,2001 ,48(10) :2428

[9] Yin Wenyan ,Pan Shujun ,Li Lewei ,et al. Experimental characterization of on-chip inductor and capacitor interconnect : part Ⅰ. series case. IEEE Trans Magn ,2003 ,39(6) :3497

一种用以改善硅衬底螺旋电感性能的局域介质增厚新技术*

杨　荣　李俊峰　赵玉印　柴淑敏　韩郑生　钱　鹤

(中国科学院微电子研究所，北京　100029)

摘要：提出了一种用于提高硅基螺旋电感性能的局部介质增厚技术.这种技术通过淀积、光刻和湿法腐蚀工艺,局部增加电感下方的氧化层厚度,以降低衬底损耗和提高电感性能.所采用的结构及工艺简单、成本低廉,与 CMOS 工艺兼容良好.用这种技术制作的几种不同电感量的方形螺旋电感、品质因数和自谐振频率均显著提高.10nH,5nH 和 2nH 的电感,品质因数的峰值分别提高了 46.7%,49.7%和 68.6%;而自谐振频率的改善更明显,分别达到了 92.1%,91.0%及不低于 68.1%.

关键词：硅；电感；结构；工艺；品质因数；自谐振频率

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杨　荣　男,1976 年出生,博士研究生,目前从事 RF CMOS 技术的研究.

李俊峰　男,1973 年出生,副研究员,博士研究生,目前从事超大规模集成电路技术研究.

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