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# A Novel Matched Filter Structure with Neuron MOS Devices*

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**Abstract**: Based on the principle of the neuron MOS device, a novel matched filter structure which is easily realized by neuron MOS is presented and the details of circuit performance is analyzed. Compared to the conventional structure, the number of circuit elements is decreased greatly for the same function. The test chip is fabricated in 0.35μm process, and the measured result shows that the system structure is feasible and effective.

**Key words**: neuron MOS; matched filter; threshold
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## 1 Introduction

In 1991, Shibata and Ohmi presented a new device structure called neuron MOS (abbreviated by neu-MOS or νMOS)[1]. In the last 10 years, the device has shown great potential functions in many circuit applications such as multi-logic circuit, VLSI and so on[2~4]. In this paper, a new application of this device in matched filter is presented. The circuit structure of a novel matched filter is presented, and the detailed circuit performance is analyzed. It can be seen that the structure introduced in this paper is easily realized by neuron MOS, and the number of devices is decreased greatly compared with the conventional structure. The circuit is simulated by HSPICE, and a test chip was fabricated with 0.35μm IC process, the test result is given also. This matched filter can be used in many fields such as CDMA communication system, image manipulation and so on.

## 2 Conception of neuron MOS

The symbol of neuron-MOS is shown in Fig. 1. The structure of the device is different from the normal MOSFET. It has multiple input gates coupled to the floating gate through capacitor. The potential of the floating gate $\phi_f$ is decided by

$$\phi_f = \frac{C_1V_1 + C_2V_2 + \cdots\cdots + C_nV_n}{C_{TOT}} \quad (1)$$

where

$$C_{TOT} = \sum_{i=0}^{n} C_i$$

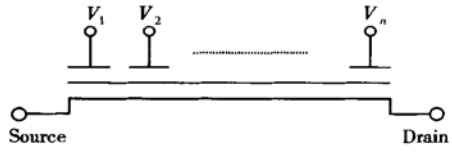


Fig. 1　Symbol of νMOS

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The total capacitor includes the capacitor $C_0$ which is the capacitor between the substrate and the floating gate. When the $\phi_f$ is less than the threshold of the transistor as seen from the floating gate ($V_{TH}^*$), the transistor will be off; on the contrary, if $\phi_f$ is over $V_{TH}^*$, the device will be turned on.

That is to say the condition of the transistor being turned on is

$$\frac{C_1V_1 + C_2V_2 + \cdots\cdots + C_nV_n}{C_{TOT}} > V_{TH}^* \qquad (2)$$

From Eq. (2), we know that whether the transistor turns on or not is decided by the weighted sum of the voltage applied in the multiple input gates. It is worth to note that the operation of the weighted sum calculation in the device does not produce the power loss. The power loss only occurs during the procedure of the recharge and discharge through the capacitors, which make the circuit composed of this device has the characteristics of low power loss. In addition, although there are many capacitors in the input terminals, they will not affect the operation speed of the device because they are serial to the capacitor $C_0$.

## 3 Conventional digital matched filter structure

The structure of conventional digital matched filter (DMF) is shown in Fig. 2[5]. The frame S is the sliding register, and the DMF is illustrated in the big dashed frame. Generally, before the sampling data input to the DMF, it is necessary to quantitate the data. The data in the registers slide to the right one when a sampling data inputs, then multiply to the fixed PN code, finally the sum of the results is executed. The absolute value of the sum shows the matched degree of the input signal to the PN code. If the absolute value is above a certain value, it is considered that the input signal and the PN code matched well. So, after this, a threshold adjudgement circuit should be designed to output a high or low voltage level as shown in the Figure.

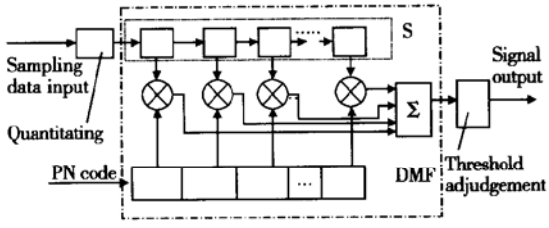


Fig. 2 Structure of conventional digital matched filter

## 4 Novel circuit structure of matched filter based on neuron MOS

Using neuron MOS to realize matched filter, the structure of the matched filter has some difference from the conventional DMF. First, because the $\nu$MOS can treat the analog data directly, the sampling data need not to be quantitated instead of being input to the matched filter directly, that is to say A/D converter can be omitted. Secondly, the multiply circuit is replaced by the difference absolute value circuit. To change this, the difference of the two structures is the different adjudgement standard. The sum of the difference absolute values shows the matched degree of the input data to the PN code. If the sum is less than a certain value, it can be considered that the input data and the PN code matched well. In this structure, the sum circuit and the adjudgement circuit are realized by a $\nu$MOS inverter. In addition, in this structure, the sliding registers of sampling data are replaced by the shift register of PN code which is more simplified than the former. The circuit structure is shown

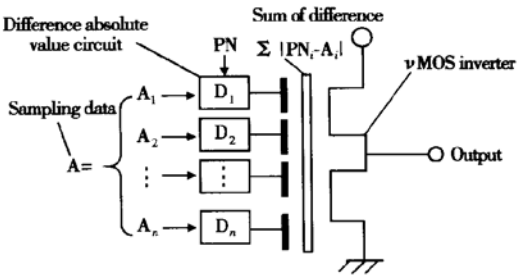


Fig. 3 Circuit structure of $\nu$MOS matched filter

in Fig. 3.

# 5 Analysis of the detailed circuit performance

## 5.1 Difference absolute value circuit

The difference absolute value circuit can be easily realized by *v*MOS as shown in Fig. 4[4]. In addition to the assistant switches, the circuit is mainly composed of two *v*MOS source followers.

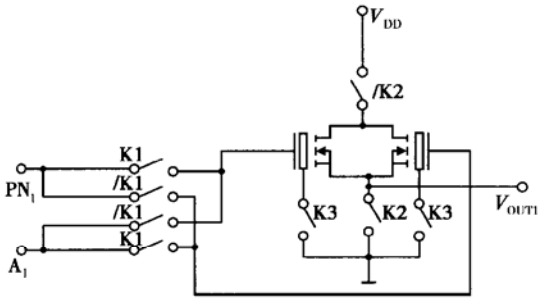


Fig. 4　Difference absolute value circuit

To simplify the analysis, we assume that the thresholds of the *v*MOS seen from the floating gate are zero. Controling the state of switches, K1~ K3 can make the circuit operate at the four phases in turn: reset phase, prepare phase, exchange phase, source follow phase as shown in Figs. 5(a), (b), (c), and (d). At the reset phase, turn on the switches K1 and K3, the potential of the floating gate would be reset to zero. Then turn the switch K3 off to let the circuit enter prepare phase. This time the potential of the floating gate would be still zero. And then turn off the switch K1 to exchange the input signals $PN_1$ and $A_1$, the circuit will enter the exchange phase. This time the potential of the floating gate would be $A_1 - PN_1$ (the left one) or $PN_1 - A_1$ (the right one). Finally turn the switch K2 on, one of the source followers that the potential of the floating gate is over zero will be activated, the circuit enter the source follow phase, and the output will follow the greater value of the differences ($|A_1 - PN_1|$).

Compared with the conventional multiple circuit, the number of devices is decreased greatly. Figure 6 is the simulation result of this circuit by HSPICE. Here we simulate two periods (each period is 2$\mu$s), during which the input $PN_1$ is applied to high voltage level (5V). At the first period, the other input $A_1$ is applied to 2V. So at the source follow phase, the output of this period should be the difference absolut value of the two inputs that is 3V. At the second period, $A_1$ is apllied to 0V, as a result, at the source follow phase, the output should be 5V. From the figure, it can be seen that the result is complied with the analysis. That is to say, using the difference absolute value circuit, the difference absolute value of each sampling data $A_i$ and PN code $PN_i$ can be carried out.

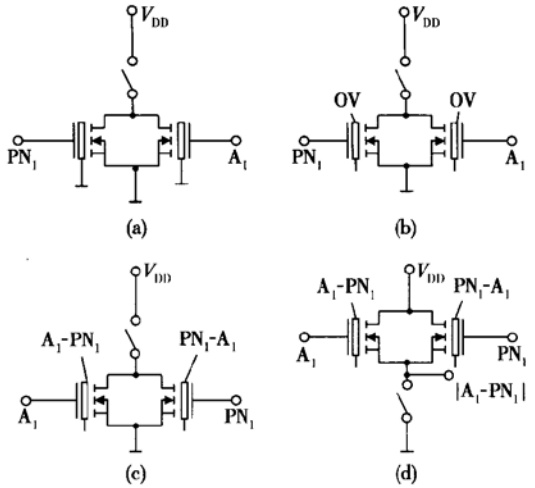


Fig. 5　Analysis of difference absolute value circuit (a) Reset phase; (b) Prepare phase; (c) Exchange phase; (d) Source follow phase

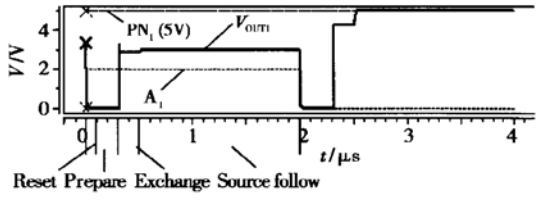


Fig. 6　Simulation result of difference absolute value circuit

## 5.2 Sum and adjudgement circuit

If the sampling data and the PN code matched well, the sum of all difference absolute value circuit

cells should be less than a certain value $V^*$, so the following circuit should output a high voltage level when

$$\sum |PN_i - A_i| = \sum V_{OUTi} \leqslant V^*$$

This function called sum and adjudgement function can be realized by a νMOS inverter as shown in Fig. 7. Take the capacitors as the relationship of $C_1 = C_2 = C_3 = \cdots = C_n$, and $C_0 \ll (C_1 + C_2 + C_3 + \cdots + C_n)$, then the potential of the floating gate $\phi_f$ would be

$$\phi_f = \frac{C_1V_{OUT1} + C_2V_{OUT2} + \cdots + C_nV_{OUTn} + C_{n+1}V_{adj}}{C_{TOT}}$$

$$\approx \frac{1}{n+1}\sum (V_{OUT1} + V_{OUT2} + \cdots + V_{OUTn} + V_{adj})$$

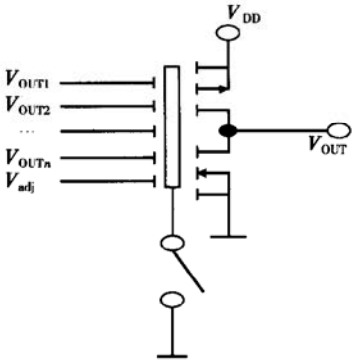


Fig. 7 νMOS inverter

If it is less than the threshold of the inverter $V^*_{INV}$, the inverter will output a high voltage level. On the contrary, if it is over $V^*_{INV}$, the output will be at low voltage level. That is to say when

$$\sum (V_{OUT1} + V_{OUT2} + \cdots + V_{OUTn}) \leqslant (n+1)V^*_{INV} - V_{adj}$$

the output will be at high voltage level. Here adding the terminal $V_{adj}$ is used to adjust the threshold value of the adjudgement circuit.

## 6 Experiment result

We fabricated a test chip for four sampling data. Figures 8(a) and (b) is the photograph of the difference absolute value circuit and νMOS inverter. Figure 8(c) is the test result of the difference absolute value circuit. Here one of the input signals $PN_1$ is applied to 1V. The other input $A_1$ is applied to 1, 2, 3, 0.5, and 0V as shown in the figure. The time when the switch /K2 is at the high level is the phase of source follow. Each difference absolute value of the two input voltages is 0, 1, 2, 0.5, and 1V, so at each source follow phase the output $V_{OUT1}$

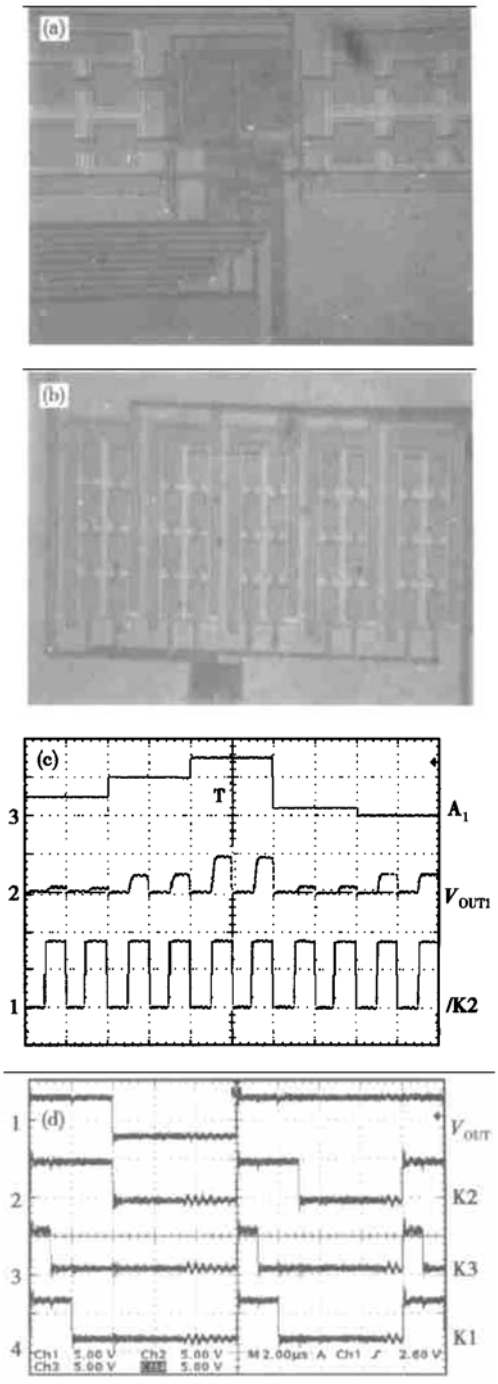


Fig. 8 Photographs of test chip and test result (a) Difference absolute value circuit; (b) νMOS inverter; (c) Test result of difference circuit; (d) Test result of the test chip

should be 0, 1, 2, 0.5, and 1V. From the results, we can know that the outputs are mostly conformed with the simulation results. Figure 8(d) is the test result of the test chip. We tested two groups data. For the first group the four sampling data are 0, 4.5, 4.5, and 4.5V. The PN codes are 1(5V), -1(0V), 1(5V), and 1(5V). For the second group the four sampling data are 4.5, 0, 4.5, and 4.5V. The PN codes are the same as the first group. It can be seen that for the first group, the PN code does not match the sampling data well, but for the second group, the two signals match well. So the output should be at low voltage level at the source follow phase for the first group and high voltage level for the second group. Here the time when the switch K2 is at the low voltage level is the phase of source follow. From the figure, it can be seen that the result is complied with the analysis.

## 7 Conclusion

A novel matched filter structure based on neuron MOS is presented. Compared with the conventional digital matched filter (DMF), the structure is much more simplified and the number of devices is decreased greatly. The experiment result of the test chip shows that the circuit structure is properly.

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# 用神经元 MOS 结构实现的一种新型匹配滤波器*


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**摘要**: 在神经元 MOS 基本工作原理的基础上, 提出了一种新型的匹配滤波器结构, 并对具体电路进行了分析. 与传统的匹配滤波器相比, 具有结构简单的优点, 大大减少了器件数目. 最后给出了测试芯片的结果, 验证了电路的可行性.



**关键词**: 神经元 MOS; 匹配滤波器; 阈值

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