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A 71mW 8b 125MSample/s A/D Converter*

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Abstract: A 1.8V 8b 125Msample/s pipelined A/D converter is presented. Power efficiency is optimized by size scaling down scheme using low power single stage cascode amplifier with a gain boosted structure. Global clock tree and local generators are employed to avoid loss and overlap of clock period. The ADC achieves a signal-to-noise-and-distortion ratio (SNDR) of 49.5dB(7.9ENOB) for an input of 62MHz at full speed of 125MHz, consuming only 71mW. It is implemented in 0.18μm CMOS technology with a core area of 0.45mm^2.

Key words: analog-to-digital converter; pipeline; low power; low voltage
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1 Introduction

Super performance digital communication and waveform acquisition or instrumentation require analog-to-digital converters (ADCs) with resolution of at least 7 bits and sampling rates higher than 50Msample/s. For an embedded SOC application, 8b 125Msample/s ADC is a challenge for its low voltage and low power requirement. Now, with deep sub-micron CMOS transistors, supply voltage of digital circuit is reduced from 5.0V to 3.3V and even to 1.8V with CMOS process improvement. Single supply voltage is aimed at both digital and analog for convenient use. However, low supply voltage presents a major challenge to analog circuit design due to mostly reduced dynamic range.

Power efficiency is also very critical for high speed ADC design, especially embedded in a SOC. Pipelined structure is a popular choice due to its good balance between the power and the speed. Those high speed 8 bits ADCs reported in Ref. [1 ~ 3] in pipeline structure combined with other technology, whose power dissipation is still considerable large, all over 150mW even near 400mW. The subject of this work is to develop a very low power and high speed A/D converter, operating at 1.8V supply voltage.

2 ADC architecture

In general, a multistage pipeline ADC consists of cascaded stages. Each stage contains a t-bit sub A/D converter (subADC) and a residue circuit with gain of 2^t. All stages process different input (from the output of the previous stage) simultaneously. The sum of the resolutions of all the stages is usually made greater than the output resolution to introduce redundancy. The use of redundancy and digital correction will overcome the effects of

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comparator and OTA offsets on the ADC linearity[4]. The output of each stage consists of two parts, a low-resolution digital output and the amplified analog residue. With the digital error correction, as long as the analog residue is accurate, errors in the digital outputs can be sensed and corrected. As a result, the main accuracy limitation is the linearity of the residue circuit.

It has been proved that increasing stage resolution improves the linearity[5]. However, the power dissipation and the die area will increase at the same time. Stage resolution should be designed from a linearity standpoint. As for an 8-bit ADC, 1.5-bit per stage pipelined architecture will satisfy the linearity requirement with acceptable power dissipation. This ADC architecture is shown in Fig. 1. The analog input is sampled by a unity gain sample hold (S/H) stage, followed by interstages with gain of two amplification and residual summation. The sample and hold stage is added in front of the ADC as the first stage for better dynamic linearity for high frequency input signals. Two comparators are used in each stage to quantize the analog residue into a 1.5-bit digital word, while a 2-bit flash A/D conversion is implemented with three ones in the last stage because it can not be corrected. The 1.5-bit output from the front 6 stages feeds into an error correction circuit after aligned, which generates the final digital output by correcting with the last two bits.

Switched-capacitor circuits are used to implement gain-of-two amplification and residual summation. The diagram of the gain stage circuit is shown in Fig. 2. Two phased nonoverlapping clocks

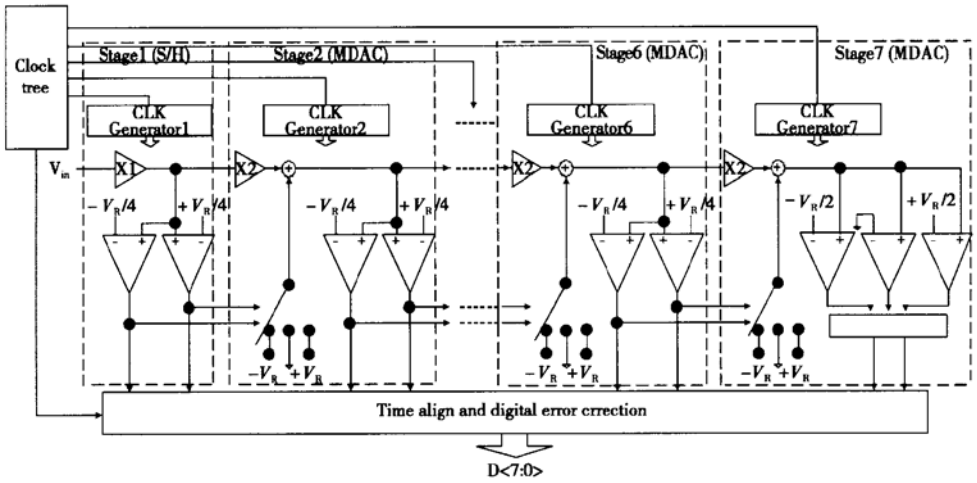

Fig. 1　Pipeline ADC architecture

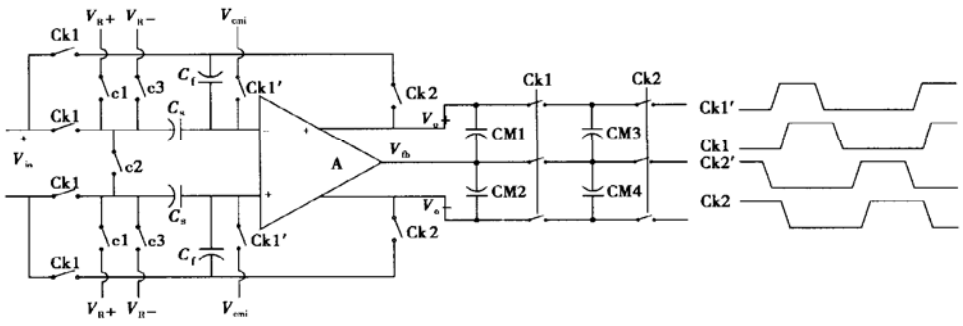

Fig. 2　Gain-of-two amplification and RSTG

Ck1′ and Ck2′ with their delayed phase Ck1 and Ck2 are generated to control the operation of charge transfer and conservation. It is a fully differential bottom-plate sampling and flip-around structure. During Ck1′ and Ck1, the operational amplifier is reset and the bottom plates of capacitors C_s and C_f are tied to V_{in}. During Ck2′ and Ck2, the bottom of C_f is connected to the output of the operational amplifier, while the bottom plate of C_s is connected to $+V_R$, $-V_R$ or shorted to differential zero, depending on the control clocks c1, c2, and c3 encoded with the comparator outputs from the previous stage. Assuming the linear gain of the operational amplifier is A, the gain stage transfer function is derived from Eq. (1), according to the charge conservation at the input of the operational amplifier. If $A \to \infty$ and $C_s = C_f$, the equation can be simplified to ideal gain-of-two and residual function.

Ck1′ turns off before Ck1, so the charge conserved at the input node of operational amplifier does not change when Ck1 turns off. Then the charge injection dependent on input signal is eliminated and linearity is improved. The sample and hold structure is similar to interstages based on charge transfer and conservation. Ck2′ is used to control switches in adjacent stages.

$$V_o = \begin{cases} V_{in} \times \dfrac{C_s + C_f}{C_s/A + (1 + 1/A) C_f} - V_R \times \dfrac{C_s}{C_s/A + (1 + 1/A) C_f} & \text{if} \quad V_{in} > +\dfrac{V_R}{4} \\ V_{in} \times \dfrac{C_s + C_f}{C_s/A + (1 + 1/A) C_f} & \text{if} \quad -\dfrac{V_R}{4} < V_{in} < +\dfrac{V_R}{4} \\ V_{in} \times \dfrac{C_s + C_f}{C_s/A + (1 + 1/A) C_f} + V_R \times \dfrac{C_s}{C_s/A + (1 + 1/A) C_f} & \text{if} \quad V_{in} > -\dfrac{V_R}{4} \end{cases} \Rightarrow \begin{cases} 2V_{in} - V_R \\ 2V_{in} \\ 2V_{in} + V_R \end{cases} \quad (1)$$

As shown in Fig. 2 a dynamic common-mode feedback (CMFB) circuit[6] composed of the switched-capacitor circuits is used for power consideration and convenience of arbitrary CMFB voltage.

3 Circuit description

3.1 High-swing regulated folded cascode amplifier

Operational amplifier with high gain and output swing can be easily realized by two stages. However, power dissipation is very large in order to achieve so high speed. Therefore, single stage folded cascode amplifier is adopted. The circuit is shown in Fig. 3. High DC gain is achieved by regulating amplifiers. Furthermore, only a V_{dsat} is required over these transistors so that output swing is increased compared with gain-boosting structure with just two transistors in Refs. [6, 7].

A pMOS input pair is used for a low input common voltage, which is different from the output common to achieve a high dynamic range in low voltage environment. The input of the regulating amplifiers is at transistor sources[8], which can operate with very low bias currents and can be constructed with very small size transistors to minimize the decrease of GBW. The amplifier uses a SC common-mode feedback (CMFB) circuit which is easily implemented in SC system with high dynamic range. According to simulation, the cascode amplifier of the first stage achieves 81dB DC gain and

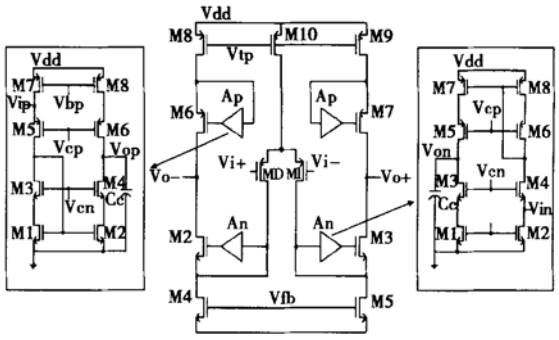

Fig. 3 Cascode amplifier with gain boosted

1.2V differential output swing with 800MHz UGBW loaded by 1pF capacitor.

In order to reduce the power dissipation, size of following operational amplifiers is reduced due to the scaling down accuracy requirement of cascade stages. The power dissipation is reduced significantly after size scaled down. The power dissipation of operational amplifier in S/H is 10mW and 8mW is consumed for the first gain stage one with 20% saved.

3.2 Switches: NMOS, CMOS, bootstrap MOS switch

On-resistance of MOS switch is a significant limitation on the tracking speed and the settling time. Moreover, distortion will be produced by nonlinearity of on-resistance when tracking continuous signals, especially the S/H stage. Three types of switch are used to optimize the total performance, NMOS, CMOS, and bootstrapped MOS switch. Switches connected with input common mode voltage are NMOS switches, whose another node is connected with the input node of the amplifier due to the low input common mode voltage. All the other switches except the two sampling ones are all CMOS switches, whose distortion is not the dominant consideration.

Bootstrap circuit[9] shown in Fig. 4 is used to obtain high linear sampling switches. The circuit produces a constant voltage near the supply voltage

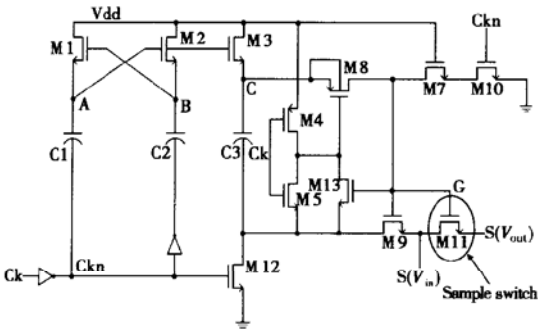

Fig. 4　Boostrapped MOS switch

between the gate and source of the sampling NMOS. Due to a constant V_{gs}, the on-resistance of the switch is almost constant, which significantly reduces the distortion. Furthermore, constant V_{gs} of sampling switch enables a common mode rejection. As will be seen in section 4, SNDR changes very slightly when the common mode level wanders.

3.3 Differential comparator

The sub-ADC in each pipeline stage consists of two fully differential comparators shown in Fig. 5[9]. In the 1.5-bit-per stage architecture, the sub-ADC thresholds are $+V_R/4$ and $-V_R/4$, where the ADC input range is $-V_R$ to $+V_R$ differential. The switched-capacitor comparator operates on nonoverlapping two-phase clocks Ck1 and Ck2. The differential network samples V_R during Ck1 onto capacitor C, while the input at capacitor $3C$ is shorted giving differential zero. During Ck2, the input signal V_{in} is applied at the inputs of both capacitors causing a differential voltage proportional to $V_{in}-V_R/4$ to appear at the input of the comparator preamp. At the end of Ck2, the regenerative flip-flop is latched to make the comparison and produce digital levels at the output V_o.

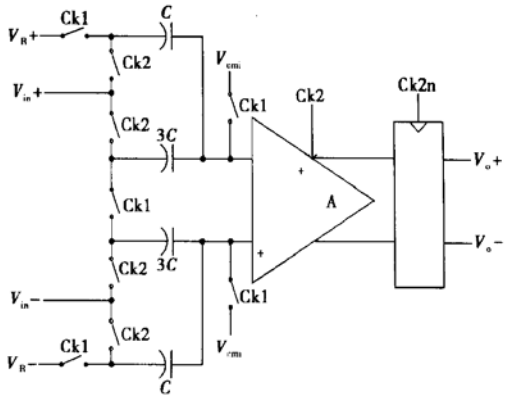

Fig. 5　Switched-capacitor comparator

Due to the digital correction, a comparator error of $V_R/4$ (150mV) can be tolerated. With such a large allowable offset, a fully dynamic comparator is often used in order to reduce static power consumption[9]. At this low voltage, however, there are significant meta-stability problems with a fully dynamic comparator. Therefore, a preamp with static current is used before regenerating.

3.4 Distributed clock and master-slave current bias scheme

Operating at such high frequency, a clock skew might be so large that timing will be difficult to control and overlap might occur. Therefore, a global clock tree is employed with local clock generator for each stage to avoid loss and overlap of clock period due to delay skews.

Disturbance between stages caused by switching is serious, so slave bias generator for each stage is employed driven by a common master bias current.

4 Simulated results

A summary of the ADC overall performance given in Tabel 1 and Fig. 6 is the FFT analysis of simulated results. The chip is implemented in 0.18μm CMOS process. The layout of the ADC core is shown in Fig. 7. Compared with those high speed 8-bit ADCs reported from Refs. [1~3], power dissipation of the converter in this design is very low with good dynamic performance. Only 1.5dB of SNDR varies shown in Table 1 when the common mode voltage of input signal changes from ground to supply voltage.

Table 1 Performance summary

Resolution	8bit
Conversion rate	125MHz
Process	0.18μm 1p6M mixed signal CMOS
Power supply	1.8V
Total power	71mW@1.8V
SNDR (f_{in}= 62MHz f_{clk}= 125MHz)	49.2dB@0V(common) 49.5dB@0.6V(common) 48.0dB@1.8V(common)
SFDR	59dB
Die area	0.45mm^2

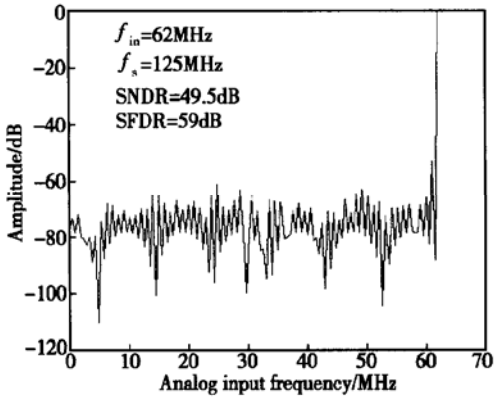

Fig. 6 Spectrum analysis

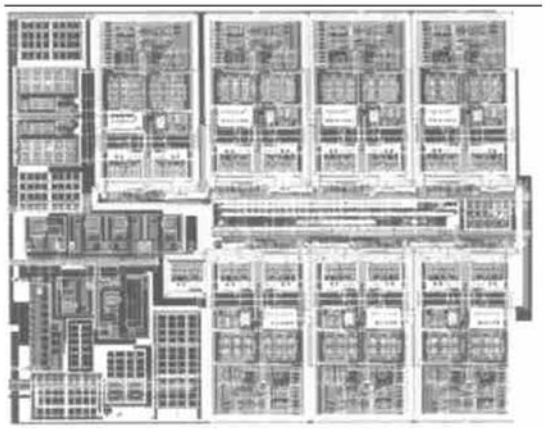

Fig. 7 ADC core layout

5 Conclusion

Low power is achieved by using the low power operational amplifier with power optimized by size scaling down scheme. Special consideration on low voltage environment is discussed such as high swing regulation amplifiers and low distortion switches. The design achieves 7.9 ENOB for 62MHz input at full sampling rate of 125MHz with a strong rejection to DC wandering of input signal, consuming only 71mW with a core area of 0.45mm^2 operating at 1.8V power supply.

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References

[1] Jun Ming, Lewis S H. An 8-bit 80-Msample/s pipelined ana-

log-to-digital converter with background calibration. IEEE J Solid-State Circuits, 2001, 36(10): 1489

[2] Choe M J, Song B S, Bacrania K. An 8-b 100-Msample/s CMOS pipelined folding ADC. IEEE J Solid-State Circuits, 2001, 36(2): 184

[3] Wang Yunti, Razavi B. An 8-bit 150-MHz CMOS A/D converter. IEEE J Solid-State Circuits, 2000, 35(3): 308

[4] Lewis S H, Gray P R. A pipelined 5-Msample/s 9-bit analog-to-digital converter. IEEE J Solid-State Circuits, 1987, 22(12): 954

[5] Lewis S H. Optimizing the stage resolution in pipelined, multistage, analog-to-digital converters for video-rate applications. IEEE Trans Circuits Syst Ⅱ, 1992, 39(8): 516

[6] Marques A, Peluso V, Steyaert M, et al. A 15-b resolution 2-MHz Nyquist rate ADC in a 1-μm CMOS technology. IEEE J Solid-State Circuits, 1998, 33(7): 1065

[7] Flandre D, Viviani A, Eggermont J, et al. Design methodology for CMOS gain-boosted folded-cascode OTA with application to SOI technology. Proc ESSCIRC'96, 1996, (9): 320

[8] Gatti U, Maloberti F, Torelli G. A novel CMOS linear transconductance cell for continuous-time filters. Proc ISCAS, 1990, 2(5): 1173

[9] Abo A M, Gray P R. A 1.5-V 10-bit 14.3-MS/s CMOS pipeline analog-to-digital converter. IEEE J Solid-State Circuits, 1999, 34(5): 599

一个 71mW 8 位 125MHz A/D 转换器*

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摘要: 介绍了工作在 1.8V 的 8 位 125MHz 流水线 A/D 转换器. 采用了低功耗的增益自举单级折叠级联运放, 器件尺寸逐级减小进一步优化功耗. 为消除不匹配造成的相位遗漏与重叠, 每级均有独立的双相不交叠时钟发生电路, 并由一全局的时钟树驱动. 输入频率为 62MHz 的信号, 以 125MHz 时钟采样, 可获得 49.5dB(7.9 位有效精度) 的信号与噪声及谐波失真比(SNDR), 功耗仅为 71mW. 电路用 0.18μm CMOS 工艺实现, 面积为 0.45mm^2.

关键词: 模数转换器; 流水线; 低功耗; 低电压

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