Electrical Performance of Static Induction Transistor with Mixed I–V Characteristics

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Abstract: The mixed non-saturating I–V characteristics of static induction transistor (SIT) are investigated. The optimum matching relations among the structural, material, and technological parameters are also presented. The technological experiments demonstrate that the channel parameters play a critical role in determining whether it is a mixed, triode-like or pentode-like I–V characteristics. The general control principles, methods, and criterions of fabrication parameters as well as the effect of control factor are analytically discussed. The results are useful for design and fabrication of SIT, especially for SIT with mixed I–V characteristics.

Key words: static induction transistor; pinch-off; mixed characteristics; saturation
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1 Introduction

It is well known that electrical performances of static induction transistor (SIT) are strikingly influenced by small dimension effects. Its I–V characteristics and electrical performance parameters are intimately dependent on structural, material, and technological parameters. The relationships between the electrical performances of SIT and its structural, material as well as technological parameters are not only very intricate but also impacted each other. Technological practices could not get right guide as the theory on this subject is imperfect. The successful probabilities of SIT fabrication are not high because the electrical parameters are modulated by experience to certain extent. The technology regularities are submerged or disturbed by numerous and disorderly phenomena. There-

fore, it is necessary to be able to control electrical performances of SIT accurately according to the practical requirements rather than rely on a haphazard "trial and error" approach. So far, neither domestic nor international achievements in scientific research for technology control of electrical performances of SIT have been reported.

SIT is a structurally sensitive high frequency high power device[1~10]. Its electrical performances are determined by following factors: structural parameters (length l_c, thickness d_c and width w_c of the channel along with the ratio of l_c/d_c), material parameters (doping concentration N_D in channel region and the thickness of epitaxial layer T) and technological parameters mainly including the depth of source X_{js}, diffusion depth of gate region X_{jg}, doping concentrations N_{DS}, N_{AG} of source and gate regions as well as transverse diffusion factor Y. Among these parameters there must be a certain

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optimum matching relationship for the SIT with excellent performances. The main aim of this paper is to find out the relationship. The I-V characteristics is always the fundamental electrical performance of all the various type static induction transistors directly reflecting the quality of device. The I-V characteristics of normally-on SIT with vertical multi-channel is obviously dependent on channel parameters l_c/d_c, l_c, doping concentration N_D in the channel. The non-saturating I-V characteristics of the SIT result from short and narrow channel. With the variations of channel parameters, the I-V characteristics of SIT transfer from pentode-like to triode-like characteristics or conversely. This corresponds to that the pinch-off point approaches the source region and the carrier injection mode tends to space charge limit effect. The I-V characteristics of SIT displays many features in the transformation such as standard saturating pentode-like characteristics, quasi-saturating inclining triode-like, mixed characteristics of pentode- and triode-like, triode-like, and triode-like with a certain shift along voltage axis.

When used in low resistance load directly driven circuits, it is generally believed that the SIT with mixed I-V characteristics is more suitable than with pure triode-like as a result of the reduction of dead region but maintaining the merits of triode-like such as low output impedance, low distortion, and convenience for low resistance load directly driving.

2 Control of fabrication parameters of SIT

The control of I-V characteristics is essentially the modulation for parameters of the channel. For high performance SIT, it is a key step to design and fabricate a structurally reasonable channel region. This is not only a theoretical but also a practical question. In accordance with our experience, some discussions are proposed as follows.

2. 1 Thickness d_c of channel

Firstly, the control for transverse dimension of the channel i. e. thickness d_c is discussed. According to our experience, a parameter β is defined as:

$$\beta \equiv d_c/a_0 = 2(a/a_0) \qquad (1)$$

where a is a half of thickness of channel, a_0 is depletion layer width of gate-channel p^+-n^- junction at $V_G = 0$. Here, this junction is approximately considered as single-side abrupt p-n junction. a_0 is a function of doping concentration N_D of substrate, to be expressed as:

$$a_0 \approx \left[\frac{2k\epsilon_0}{qN_D} \Phi_B \right]^{1/2} \qquad (2)$$

where q is the electron charge (1.6×10^{-19}C), k is dielectric constant of silicon (11.8), ϵ_0 is the dielectric constant of vacuum (8.86×10^{-14}F/cm), Φ_B is built-in potential of p^+-n^- junction about 0.76V in our structure. According to Eq. (1), thickness of channel can be expressed as

$$d_c = \beta a_0 \qquad (3)$$

β is referred to as pinch-off factor of channel. For the given channel length, the value of β indicates the pinch-off degree of channel corresponding to different I-V characteristics of SIT, as schematically illustrated in Fig. 1. The smaller value of β means deeper degree of pinch-off and higher potential barrier for majority carriers. It can be clearly seen from Fig. 1 the influence of β on the I-V characteristics is remarkable. In order to arrive excellent I-V characteristics it is necessary to choose appropriate β value. As a result of the pinch-off factor $\beta \geq 4$, the channel thickness $d_c \geq 4a_0$, the channel is not pinched off at $V_G = 0$, the I-V characteristics of SIT is similar to a resistance as shown in Fig. 1(a). When $\beta = 2.5$, $d_c \approx 2.5a_0$, although the channel is inclined towards pinch-off, the channel is still in normally-on state at $V_G = 0$ as demonstrated in Fig. 1(b). As the channel is pinched off only at low negative biased voltage for example $-0.5 \sim -1$V as prescribed, the SIT exhibits typical mixed I-V characteristics from triode-like to pentode-like. When β is decreased to 1.4, $d_c = 1.4a_0$, the

channel is already pinched off but with less degree at $V_G = 0$, and SIT presents representative triode-like I–V characteristics as shown in Fig. 1(c). As the β is further reduced to 0.8, $d_c = 0.80a_0$, the channel is deeply pinched off at $V_G = 0$, and at this time SIT is in normally-off state with following two features as demonstrated in Fig. 1(d): (1) the characteristic curves shift along V_D axis with cer-

tain voltage; (2) as for the small current region, the I–V characteristics is practically identical with that of bipolar static induction transistor (BSIT). According to the practical technological experience, $\beta \approx 2.5$ is chose for normally-on SIT; $\beta \approx 0.7 \sim 1.0$ for normally-off BSIT and SITH (static induction thyristor).
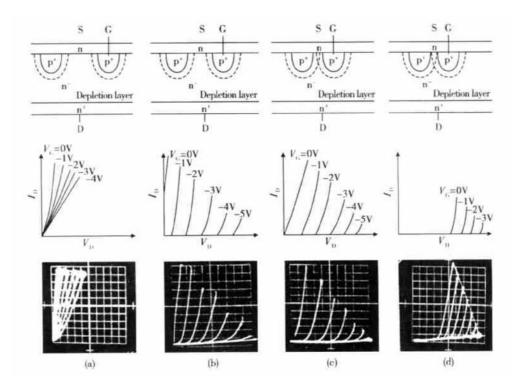

Fig. 1 I–V characteristics with different β (a) $\beta = 4.0$; (b) $\beta = 2.5$; (c) $\beta = 1.4$; (d) $\beta = 0.8$

2.2 Length l_c of channel

When the gate region is formed by boron diffusion the lateral stretch X_{jl}, vertical depth X_j of a p^+-n^- structure have an important role in modulating the thickness d_c, length l_c of channel simultaneously. In other words, l_c, d_c as well as l_c/d_c are changed at the same time and influenced each other as illustrated in Fig. 2. It can be seen from Fig. 2

$$l_c \approx X_j - X_{js} \qquad (4)$$

Because the depth of gate region X_j is usually much larger than that of n^+ source region, the length l_c of channel can be approximately expressed as:

$$l_c \approx X_j \qquad (5)$$

Since the lateral depth X_{jl} varies near linearly with the vertical depth X_j of gate-channel p^+-n^- junction at the diffusion temperature range $1100 \sim 1250\,°C$, l_c could be shown as:

$$X_{jl} \approx Y X_j \qquad (6)$$

where Y is a coefficient between $0.52 \sim 0.7$ defined as: $Y \equiv X_{jl}/X_j$. The pitch (gate to gate spacing) is designed as

$$d \approx d_c + 2X_{jl} \qquad (7)$$

Therefore, the length l_c and pitch d can be respectively expressed as:

$$d \approx 3a_0 + 1.4l_c \qquad (8)$$

$$l_c \approx X_j \approx \frac{d - \beta a_0}{1.4} \qquad (9)$$

The important significance of the expressions (8)

or (9) is that it quantitatively describes the relationship among the structural, material, and technological parameters. Since β is an adjustable factor, the optimum matching among fabricating parameters can be so easily arrived by artificially modulating the value of β, that the satisfactory I–V characteristics and high performance of SIT can be achieved. β has effect of controlling factor in this sense.
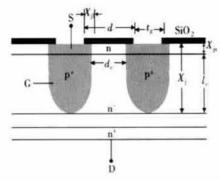

Fig. 2　Geometrical structure of unit in SIT

3　Adjustment for mixed I–V characteristics

The dimensions of channel necessary for mixed I–V characteristics are listed in Table 1. In order to achieve the mixed I–V characteristics, the channel should not be pinched off by $V_G = 0$ and ought to be pinched off by low negative biased gate voltage $V_{G,off}(-1V$ should be chosen according to

fabrication experience). The width of gate-channel depletion layer is a_0 at $V_G = 0$ and a_p at $V_{G,off} = -1V$. As a result of the relation:

$$3a_p \approx 2a_0 \qquad (10)$$

the mixed I–V characteristics is determined by following expressions:

$$a_0 < d_c = \beta a_0 \leqslant 2a_p \approx 3a_0 \qquad (11)$$
$$2 < \beta \leqslant 3 \qquad (12)$$

If a unit of length $3a_0$ is used, it is found that the ratio $l_c/3a_0$ has effects on I–V characteristics as follows:

(1) When the ratio $l_c/3a_0$ is varied between 0.3 and 0.5, the SIT presents non-saturating I–V characteristics.

(2) As the value of $l_c/3a_0$ approaches 0.7, the SIT exhibits transition I–V characteristics from mixed to less saturating mode. The typical value of $l_c/3a_0$ is 0.45 for the mixed I–V characteristics, corresponding to length of channel: $l_c \leqslant 1.35a_0$.

(3) As the value of $l_c/3a_0$ larger than 0.6, the SIT shows less saturating pentode-like I–V characteristics.

(4) When the value of $l_c/3a_0$ is close to 1, the SIT displays complete saturating pentode-like I–V characteristics.

(5) For the long length of channel l_c, the I–V characteristics of the SIT is analogous to that of JEET with a long channel; the modulating effect of potential barrier on current will disappears.

Table 1　Necessary channel dimensions for mixed I–V characteristics

$N_D/10^{14}\mathrm{cm}^{-3}$	$a_0/\mu m$	$3a_0/\mu m$	$D_c = \beta a_0/\mu m$	β	$l_c/\mu m$	l_c/d_c	$l_c/3a_0$	I–V characteristics type
2.0	2.2	6.6	15.1	6.88	3.0	0.20	0.45	Resistance
2.0	2.2	6.6	5.0	2.27	2.0	0.40	0.30	Triode-like
10.0	1.0	3.0	2.5	2.47	1.0	0.40	0.33	Triode-like
10.0	1.0	3.0	2.4	2.40	1.0	0.42	0.33	Triode-like
2.0	2.2	6.6	6.0	2.73	2.8	0.47	0.42	Mixed
2.0	2.2	6.6	6.0	2.73	3.0	0.50	0.45	Mixed
2.0	2.2	6.6	5.4	2.45	2.8	0.52	0.42	Mixed
10.0	1.0	3.0	2.5	2.50	1.4	0.56	0.47	Mixed with more pentode
2.0	2.2	6.6	4.8	2.16	2.7	0.56	0.41	Mixed with more pentode
2.0	2.2	6.6	4.7	2.14	2.7	0.57	0.41	Mixed with more pentode
10.0	1.0	3.0	2.4	2.40	2.0	0.83	0.67	Less saturating pentode
3.0	1.8	5.4	4.2	2.30	3.7	0.83	0.69	Less saturating pentode

In addition, if the ratio l_c/d_c is used as a criterion, when its value ranges from 0.45 to 0.55, the

SIT presents ideal mixed I–V characteristics. As the ratio l_c/d_c is larger than 0.8, the I–V character-

istics is inclined towards less saturating mode. The representative mixed I-V characteristics appears only at $l_c \approx 0.5d_c$ that is the optimum channel length for realizing mixed I-V characteristics. In fact, as the ratio l_c/d_c is close to 0.5, various mixed characteristics with different component of pentode-like might be obtained. The experiments show, SIT exhibits the I-V characteristics of JFET (junction field effect transistor) when the ratio l_c/d_c is larger than 1.2. Oppositely, when the ratio l_c/d_c is too small (such as 0.2), the I-V characteristics of SIT is identical with a resistance.

On the basis of above discussion, β is usually selected smaller than 3 (such as 2.2~ 2.7), $d \approx 1.7d_c$ or $d_c \approx 0.588d$, $d_c \leqslant 2.7a_0$ indicating that designed pitch d (gate to gate spacing) is about 1.7 times of actual channel thickness for SIT with mixed I-V characteristics. If a_0 is used as a length, d is expressed by the next equation:

$$d \leqslant 4.59a_0 \qquad (13)$$

which shows that designed pitch is about 4.59 time of a_0 for mixed characteristics. According to the definition of β, $d_c = \beta a_0 \approx 0.588d$, thus "controlling factor" β might be expressed as:

$$\beta \approx 0.558d/a_0 \qquad (14)$$

This equation demonstrates that once device types and electrical parameters are determined, the relationship between designed structural parameter d and material parameter a_0 is defined. For the given β and l_c with an increase in designed pitch d, the doping concentration of epitaxial wafer should be correspondingly reduced. In other words, the resistivity of silicon wafer should be increased appropriately. It can also be seen that for determined d, β ought to be increased with diminishing of a_0; for fixed $a_0(N_D)$, β is increasing with raising of d. Finally, when β is determined d should be increased with $a_0(N_D)$ simultaneously. It must be pointed out that d indicates designed value of gate-to-gate spacing defined by selective etching of gate stripe window.

4　Conclusions

The controlling principles, methods, and criteria for fabricating high performance SIT as well as the effect of controlling factor β are discussed in detail. Although these results have some approximations, they are very useful and convenient for design and fabrication of static induction devices because they are based on the technological practice. Though the above discussion is aimed at SIT, it is generally applicable to BSIT, SITH, and other SID[9~13].

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具有混合 *I-V* 特性的静电感应晶体管的电性能

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摘要: 研究了具有混合型 *I-V* 特性的静电感应晶体管, 提出了实现混合 *I-V* 特性所必需的器件结构参数、材料参数和工艺参数之间的最佳匹配关系. 工艺实践表明沟道尺寸在确定器件特性是混合型、类三极管型还是类五极管型方面有着重要作用. 讨论了静电感应晶体管性能控制的一般原则、方法和制造参数的控制判据以及控制因子 β 的作用. 研究结果对静电感应晶体管的设计和制造, 特别对具有混合型 *I-V* 特性的静电感应晶体管有实用价值.

关键词: 静电感应晶体管; 夹断; 混合特性; 饱和

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