# SCDI Flash Memory Device II: Simulation and Analysis\*

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Abstract: Step channel direct injection (SCDI) flash memory device which had been developed changes the hot carrier injection method by making a shallow step in the middle of channel [1]. Therefore high speed for programming, high efficiency for injection, and lower working voltage are obtained. Simulation and analysis for the proposed SCDI structure device are done and an optimization scheme to improve the utmost performance of SCDI device is given.

Key words: SCDI; flash memory; programming speed; optimization; low voltage

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### 1 Introduction

Flash memories received widespread attention due to their nonvolatility and online programmable/erasable characteristics. They were widely used in mobile computing system such as handheld PC, notebook, digital still picture camera, smart digital phone, minidisk, audio recorder, GPS system for automobiles, ships, and planes, and communication equipment, including cellular base station, PBS equipment, and digital routing switches.

Requirements for flash memory are usually as follows

- (1) High reliability: retention> 10 years.
- (2) Long life: Endurance> 10<sup>5</sup> cycles.
- (3) Low working voltage, low power, the best is the same as the voltage of CMOS device.
  - (4) High programming/erasing speed.

However, for traditional floating gate flash memory device, in order to avoid leakage by pin holes and make it reliable, the thickness of gate oxide must be greater than 7nm. In the mean time, the electric field distribution in the channel results in hot carrier injection near the drain region. This makes the carriers easier to be drained out and lowers the injection efficiency. Therefore, this device needs high voltage to achieve acceptable programming and erasing speed. The research of flash memory focuses on how to improve the programming/erasing speed and lower the work voltage so as to be more compatible with the CMOS device. A lot of work had been done in this field by the researcher all over the world<sup>[2-15]</sup>.

SCDI structure used to improve the program-ming/erasing speed and lower the work voltage was proposed in Reference [1]. This device achieved good results in improving programming/erasing speed. This paper gives a detailed simulation and analysis. An optimization scheme was concluded for further improvement on the performance of SCDI device.

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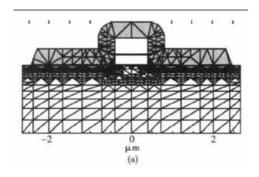
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### 2 Simulation and analysis

The simulation of conventional flash memory device and SCDI device was done by MEDICI. Figures 1 (a) and (b) are the simulation grids for conventional device and SCDI device, respectively. Figure 2(a) is the electric field distribution of planar flash memory device. It shows that the maximum value of lateral electric field is near the drain region. That is to say, the carriers injection occurs near the drain region where they can get enough energy to tunnel through the gate oxide into the floating gate. The shortcoming of this injection is that the carriers are more probably to drain out into the drain and injection efficiency is low. To obtain acceptable programming speed, high operating voltage is needed. The veritical electric field distribution is gradually reduced from source to drain, and the vertical electric field near the drain is mini-

mum, so high control gate voltage is also needed to pull the carries into the floating gate. Due to this main disadvantage, the conventional flash memory device is hard to lower the operating voltages. Figure 2(b) is the electric field distribution of SCDI device. It shows that after making a step in the midchannel, the electric field distributions are remarkably changed, the maximum value of lateral electric field is moved to the mid-channel from hereabout the drain region as well as in conventional flash memory device, and the maximum value of vertical electric field is matched to the maximum value of lateral electric field in the mid-channel, this change in electric field makes it capable to improve injection efficiency. The injection will happen in the mid-channel and overcome the shortcoming of the conventional flash memory device as described above. So SCDI device can improve the injection efficiency and lower the operating voltage.



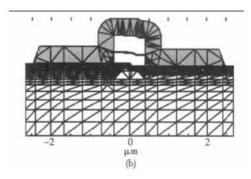
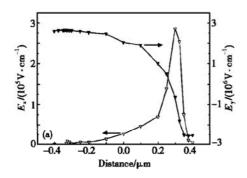


Fig. 1 Simulation grids (a) Conventional device; (b) SCDI device



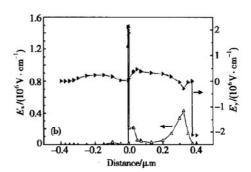


Fig. 2 Electric field distribution in the channels (a) Conventional device; (b) SCDI device

Figure 3 shows the original transfer characteristics of the devices. The threshold voltage of SCDI

device is increased as expected because the channel region underneath the Si<sub>3</sub>N<sub>4</sub> sidewall is hard to be

reversed. This distinctly increased the threshold voltage. And this is the reason that the electric field distribution is much more different from that of the conventional device, and this is just the purpose of designing SCDI device for improving injection efficiency. Figure 4 shows the programming characteristics of the two devices, the simulation condition is  $V_d = 5V$ ,  $V_g = 6V$ , and the total programming time is 1ms. These results show that the SCDI device can be programmed to a more high voltage level. That means more charges are injected into the floating gate, and high injection efficiency is obtained. In erasing process, these two devices are erased by adapting F-N tunnel mechanism, so there should be no difference in the erasing speed.

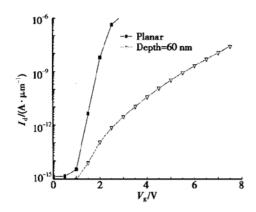


Fig. 3 Transition curves of planar device and SCDI device/Bias condition:  $V_{\rm d} = 0.1 \rm V$ 

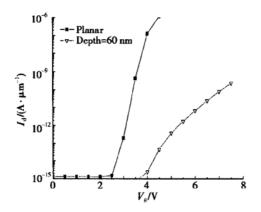
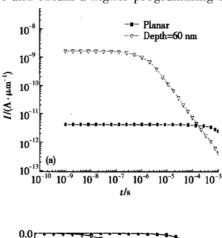


Fig. 4 Characteristics after programming Conditions:  $V_{\rm d}$ = 5V,  $V_{\rm g}$ = 6V,  $V_{\rm s}$ = 0V, total programming time: 1ms

Figure 5 (a) shows the comparison between the two injecting currents. It can be seen that the injecting current in SCDI device is higher than that in conventional device, and gradually reduced, the dropping trend is distinct. Whereas in conventional device, this trend is slower. The comparison between the injecting currents predicts that SCDI device will have higher programming speed than the conventional device. Figure 5(b) shows the comparison between the charges injected into the floating gate. This also predicts the same result that SCDI device can inject more charges into the floating gate and obtain a higher programming speed.



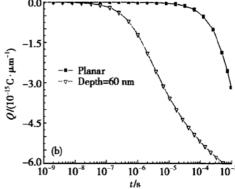


Fig. 5 Injection current and charges stored in the floating gate (a) Tunnel current; (b) Charges stored in the floating gate

## 3 Optimization

In the above simulation, SCDI structure can improve the carrier injection efficiency. In the meantime, the depth and angle of shallow step have influence on the performance of SCDI device. Simu-

lation was done to optimize the SCDI structure to obtain easy making and good performance of SCDI device. Figure 6 shows the programming characteristics of SCDI device with different depth of shallow step. The total programming time and programming conditions are the same. The results show that the best depth is not too deep or too shallow. Figure 7 shows the programming characteristics of SCDI device with different angle of shallow step. It shows that the angle of 80° is the best. From the results shown in Figs. 6 and 7, the optimization of SCDI structure is a shallow step with 60nm and the angle of 80°.

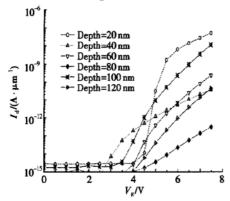


Fig. 6 Program performance versus step depth

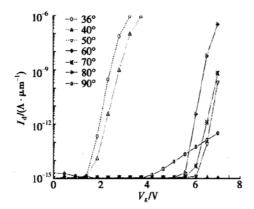


Fig. 7 Program performance versus step angle

### 4 Conclusion

From the simulation results, it shows that a special shallow step and a Si<sub>3</sub>N<sub>4</sub> spacer in SCDI device can change the electric field distribution in its channel, and this change in electric field will im-

prove the injection efficiency of carriers in SCDI device. This is useful for lowering the operating voltage and make SCDI device suitable for portable applications.

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## SCDI 结构快闪存储器件 II: 模拟与分析\*

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摘要:研制成一种台阶沟道直接注入(SCDI)器件,通过在沟道的中间制作一个浅的台阶来改变热载流子的注入方式,从而获得了高的编程速度和注入效率,降低了工作电压.并对SCDI器件结构和常规器件结构进行了模拟分析,提出了改进SCDI器件性能的优化方案.

关键词: SCDI; 快闪存储器; 编程速度; 优化; 低电压

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