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SCDI Flash Memory Device III: Experiments and Characteristics*

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Abstract: Step channel direct injection(SCDI) flash memory device is successfully achieved by 1.2μm CMOS technology, moreover good performance is obtained. At the bias condition of V_g= 6V, V_d= 5V, the programming speed of SCDI device is 42μs. Under the condition of V_g= − 8V, V_s= 8V, the erasing speed is 24ms. Compared with the same size of conventional flash memory device whose corresponding parameters are 500μs and 24ms, respectively, the performance of SCDI device is remarkably improved. During manufacturing of SCDI device, the key technologies are to make the shallow step with appropriate depth and angle, along with eliminating the etch damage during the process of Si_3N_4 spacer.

Key words: SCDI; flash memory; programming speed; key technology
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1 Introduction

Researchers all over the world have done a lot of work to improve the characteristics of programming/erasing speed of flash memory device[1~21]. All the aims are to advance the programming/erasing speed along with lowering the operating voltage, and to make it compatible with standard CMOS technology. The severe challenge to make flash memory device compatible with CMOS device is its higher programming/erasing voltage. In flash memory, it needs charge pump circuit to produce high voltage. That means there must be a high voltage device(10~ 15V) in flash memory circuit. This makes it difficult to manufacture and spends costly. If the operating voltage can be lowered to the level as the same as that of the CMOS device, it can be made by the standard CMOS technology and meet the requirement of SOC application.

The purpose of SCDI device proposed here is to improve programming/erasing speed and to lower the operating voltage. From the simulation results[22], this structure with a shallow step being made in the mid-channel can change the electric field in the mid-channel. This electric field distribution caused the carrier injection occuring in the middle of the channel, and improved the injection efficiency and lowered the operating voltage. This paper gives a detailed description about the processing technology and a detailed analysis on experimental results. During the process of SCDI device, the key technologies are to make the shallow step and etch the Si_3N_4 spacer with high selectivity

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to SiO_2, then, eliminate the damage of etchimg. The other processes are the same as the standard CMOS processes. Under the bias condition of V_g= 6V, V_d= 5V, the programming speed of SCDI device is 42μs. Under the condition of V_g= - 8V, V_s = 8V, the erasing speed is 24ms. Compared with the same size of conventional flash memory device whose corresponding parameters were 500μs and 24ms, the performance of SCDI device has been remarkably improved. At the same time, the measurement in lower operating voltage is done, and the results show that this SCDI device can work in a lower operating voltage. This make it suitable for SOC application.

2 Experiment

The main process flow is described below. The device was fabricated by adopting 1.2μm design rule and CMOS process technology. The starting wafer was p 〈100〉 silicon. After the field oxidation formed, a step of 80nm high was made(as shown in Fig. 1(a)). The angle of the step was about 90°. Then a sacrifice oxide was grown and V_{th} adjustment implantment was done. The sacrifice oxide was used to protect the silicon surface during the implantment process and remove the etching damage generated during the step formation. In the mean time, this sacrifice oxidation could make the step slightly sloped. After removing the sacrifice oxide, 10nm oxide and 80nm nitride were grown by oxidation and LPCVD, respectively. A etching back process with high selectivity to SiO_2 was performed to form nitride spacer(as shown in Fig. 1(b)) in order to avoid damaging the gate oxide. The Si_3N_4 etching process requires a higher selectivity to SiO_2. Then the damaged gate oxide was removed by HF solution(as shown in Fig. 1(c)) and gate oxide was grown again, so the damage caused by the Si_3N_4 etching back process can be eliminated. The rest of the processes were the same as that of the conventional flash memory. Table 1 shows the main processes and parameters of the SCDI device.

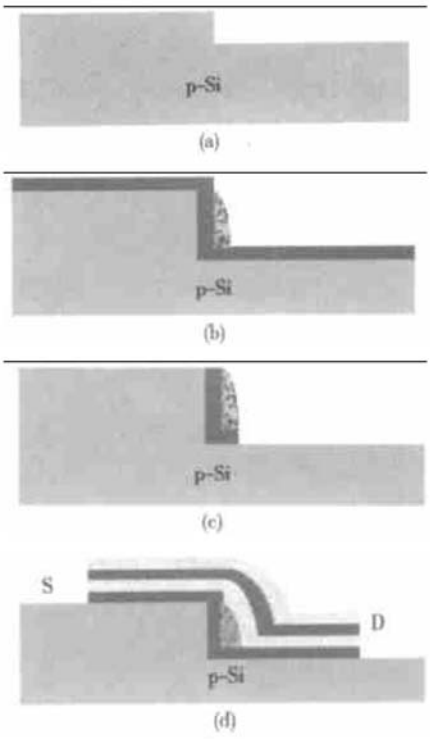

Fig. 1 Key processes for SCDI structure device (a) Field oxidation, lithograph for shallow step, etching shallow step; (b) Gate oxide formation, LPCVD Si_3N_4, Si_3N_4 spacer etching, sacrifice oxide, V_{th} adjustment implantment; (c) Remove damaged gate oxide; (d) Gate oxide reformation, LPCVD poly1, oixde/nitride/oxide multiple films, LPCVD poly2, LTO

Table 1 Key process parameters

Parameter	Value
W/L	1.2μm/1.2μm
Height of the mesa	80nm
Angle of the mesa	70°~ 80°
V_t adjust implantment	BF_2, 25keV, 4×10^{12}
Thickness of gate oxide	11nm
Thickness of first ploy-silicon	150nm
Effective thickness of ONO	25nm
Thickness of second poly-silicon	350nm
Source/drain implantment	As^+ 70keV, 3×10^{15}

3 Results and analysis

Figure 2 shows that the program performance of these two devices. It indicates that the SCDI device has higher programming speed than the conventional flash memory device. The program condition is V_d= 5V, V_g= 15V. The program time of SCDI device is about 42μs. But the program time of

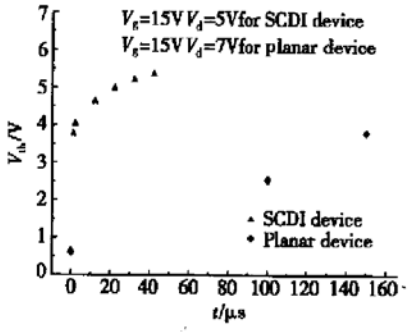

Fig. 2　Comparison of programming speed

conventional device is about 500μs, which is much longer than 42μs. This proved that SCDI device can improve the program speed remarkably. Figure 3 shows the comparison of erasing speed. There is no distinct difference in erasing time between these two devices due to the same FN tunnel mechanism. The problem of over erasing is one of the disadvantage of conventional flash memory device. From the shape of curves in Fig. 3, we can see that

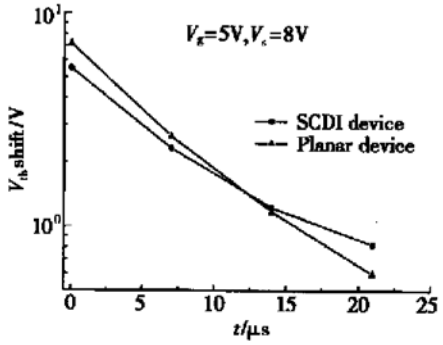

Fig. 3　Comparison of erasing speed

there is over erasing in conventional device, however, in SCDI device, this problem was restrained. Figure 4 shows the comparison of tunnel current between these two devices. These results were measured by the reference MOS device which has only the floating gate without making the ONO and control gate in the same process flow. The results show that the injection current of SCDI device is much higher than that of conventional device, and it also proved that the SCDI device can work in a lower operating voltage without degrading the performance compared with the conventional device. Figure 5 shows the drain currents of these two devices, the drain current of SCDI device is less than that of conventional device, so the injection efficiency (defined as I_g/I_d) of SCDI device was about 1000 times than that of conventional device. The SCDI device obtained remarkable improvement in programming speed and injection efficiency.

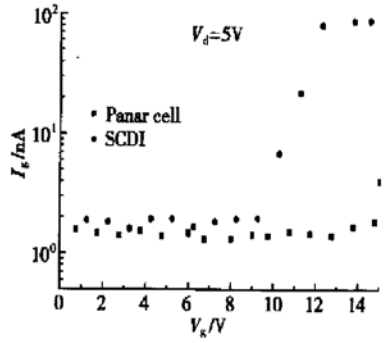

Fig. 4　Comparison of tunnel current

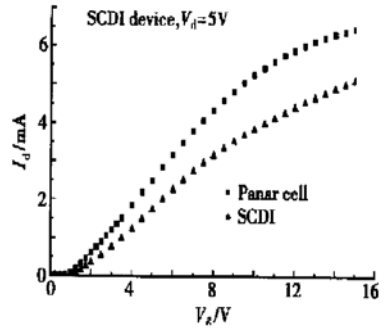

Fig. 5　Comparison of drain current

Figure 6 shows the influence of drain voltage on program speed. In this figure, we can see that the drain voltage has less effect on the program speed. It was expected that the shallow step in the mid-channel makes the gate voltage also accelerate the hot carriers to be injected into the floating

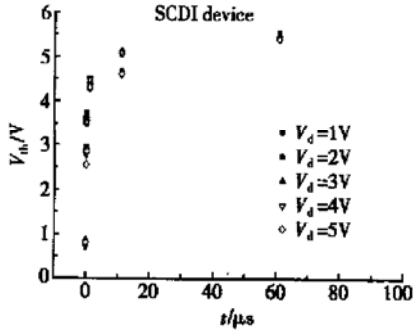

Fig. 6　Influence of drain voltage on program speed

gate. This means that lowering the drain voltage will not distinctly decrease the accelerated electric field (the lateral electric field). This result shows that the operating voltage (i. e. drain voltage, gate voltage) can be reduced because in SCDI device both drain voltage and gate voltage accelerate the carriers and pull them into the floating gate. Whereas in conventional device only drain voltage accelerates the carriers.

Figure 7 shows the threshold voltage shift after baking for 200h at 200℃. These results show that the data stored in SCDI device can be kept as long as 10000h, which can meet the requirements of applications and also indicate the SCDI device is reliable. Figure 8 shows the endurance characteristics of SCDI device. It shows that SCDI device has good writing/erasing performance because the difference

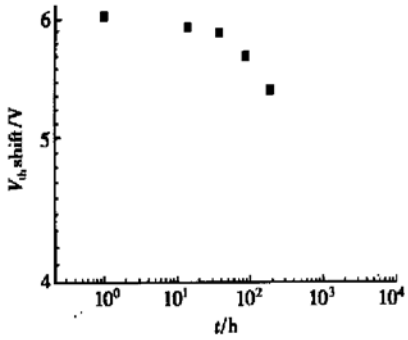

Fig. 7 Reliability of SCDI device

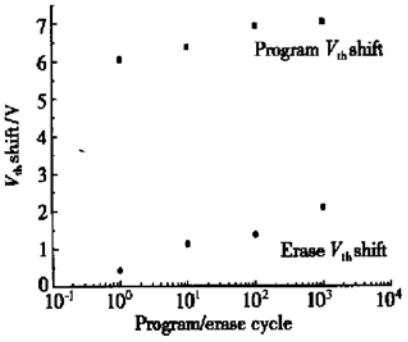

Fig. 8 Endurance characteristics of SCDI device

in Fig. 8, between the program V_{th} shift and the erasing V_{th} shift is nearly the same. The threshold voltage increased with increasing the writing/erasing cycles. This may be caused by the trap in the Si_3N_4 spacer. After programming, some charges maybe trapped in the Si_3N_4. This will increase the threshold voltage of SCDI device.

4 Conclusion

The experiment results show that SCDI structure flash memory device remarkably improved the programming speed and injection efficiency. The injection efficiency has been improved by the ratio of 1000 by comparison with that of the conventional flash memory device. Along with the improvement in injection efficiency, the operating voltage of the SCDI device can be lowered. The application in portable system is available.

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SCDI 结构快闪存储器件Ⅲ: 实验与器件特性*

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摘要: 采用 1.2μm CMOS 工艺技术制作出台阶沟道直接注入(SCDI)快闪存储器件, 该种器件具有良好的器件特性. 在 V_g= 6V, V_d= 5V 的编程条件下, SCDI 器件的编程速度是 42μs, 在 V_g= 8V, V_s= 8V 的擦除条件下, SCDI 器件的擦除速度是 24ms. 与相同器件尺寸的普通平面型的快闪存储器件相比, SCDI 器件的特性得到了显著地提高. 在制作 SCDI 器件的工艺中, 关键技术是制作合适的深度和倾斜角度的浅的台阶, 同时减少在制作 Si_3N_4 侧墙的刻蚀损伤.

关键词: SCDI 器件; 快闪存储器; 编程速度; 工艺优化; 关键技术

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