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# Effect of Metal Contamination on Characteristics of Ultra-Thin Gate Oxide

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**Abstract**: The purpose of this work relates to study on the characteristics of ultra-thin gate oxide (2.5nm thickness) and the effect of metal Al, Zr, and Ta contamination on GOI. The controlled metallic contamination experiments are carried out by depositing a few ppm contaminated metal and low pH solutions on the wafers. The maximum metal surface concentration is controlled at about $10^{12}cm^{-2}$ level in order to simulate metal contamination during ultra-clean processing. A ramped current stress for intrinsic charge-to-breakdown measurements with gate injection mode is used to examine the characteristics of these ultra-thin gate oxides and the effect of metal contamination on GOI. It is the first time to investigate the influence of metal Zr and Ta contamination on 2.5nm ultra-thin gate oxide. It is demonstrated that there is little effect of Al contamination on GOI, while Zr contamination is the most detrimental to GOI, and early breakdown has happened to wafers contaminated by Ta.

**Key words**: gate oxide integrity; metal contamination; charge to breakdown; ramped current stress; MOS capacitor
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## 1 Introduction

It is well known that gate oxide integrity (GOI) is closely related to the lifetime of devices. It was reported that GOI depends strongly on the wafer cleanness before gate oxidation[1,2]. Different contaminants have different influences on the performance, yield, and reliability of the devices. Metal contamination, for example, will cause a low breakdown field and a high junction leakage current and an increased oxide trap. which leads to a reduced minority carrier lifetime, a shifted threshold voltage and hot carrier degradation. However, little has been investigated about the effect of metal contamination on the properties of ultra-thin gate oxide (2.5nm). For thicker gate oxide (4.5~ 12nm), it was reported that these contaminants could be cleaned using various cleaning processes. It is found that all group Ⅱ elements will cause a high defect density[2]. It has been demonstrated that a great influence of the transition metal-contaminants, V, Ni, and Co on the GOI, while Mn or Zn does not have such a large impact[3]. No significant difference was observed on breakdown of thin gate oxide from the influence of Al contamination[3].

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However, little has been investigated about the effect of some metals such as Zr and Ta, which will be used for high-*k* materials, on the properties of ultra-thin gate oxide.

It is the first time to investigate the influence of metal Zr and Ta contamination on ultra-thin gate oxide of 2.5nm. Three kinds of metals, Al, Zr, and Ta, in this paper, are used respectively to contaminate the wafer surfaces before oxidation through controlled metal contamination procedure[4]. This paper focuses on evaluation of IMEC-clean™ performance and the effect of metal contamination on ultra-thin gate oxide breakdown characteristics.

## 2 Experiment

### 2.1 Metal contamination and measurement

200mm n-type (100) Si wafers were employed in this experiment. The wafer surface solutions contaminated by metal were used to spin (Al, Zr, and Ta) from standard stocks for atom absorptance spectrum (AAS) or inductively coupled plasma (ICP), respectively.

The controlled metallic contamination experiments were carried out by depositing contaminated 1w-ppm metal, low pH solutions on the wafers, exposure time: 120s, followed by high speed rotation drying. Wafers contaminated by Al were measured by AAS. Al metal concentration on the wafer surfaces was performed by VPD-DC technique, which is fully automated in the wafer surface preparation system (WSPS) tool[4]. The standard analysis solution containing 50ppb Al droplet solution etching (DSE) was used to calibrate the background of AAS tool, which is the model 4110 ZL AAS (Perkin Elmer). Metal concentration on the wafer surfaces was determined directly by TXRF for wafers contaminated by Zr, Ta, and blank wafers, respectively. TXRF measurements were performed with the Atomika model 8300W.

### 2.2 Device fabrication

All wafers were cleaned using IMEC-clean™ (reference) or contaminated with desired metals. Then all wafers were immediately transfered into gate oxidation furnace (ASM A400), followed by deposition of 250nm amorphous-silicon gate. Gate oxidation was carried out by dry $O_2$+ NO at 800℃, thickness of 2.5nm nitrided oxide. MOS capacitors were made with different areas.

### 2.3 Electrical measurements

Manual measurements were done on Cascade Summit Probe Stations with a HP4156A or HP4156B Parameter Analyser by means of a ramped current stress (RCS), gate injection mode, with 10 points/decade. The delay time was 100ms. The *I*-*V* curves were taken on at least three different positions on the wafer for different capacitor areas: E-, F-, G-MOS capacitors, $2.55\times10^{-4}$, $5.03\times10^{-5}$ and $1.26\times10^{-5}$ $cm^2$, respectively. At least 30 MOS capacitors were used to measure *I*-*V* for each kind of capacitor area.

## 3 Results and discussion

### 3.1 Contamination level before and after oxidation

Figure 1 presents the measured concentrations of surface contaminants. It can be seen that for clean wafers, metal surface concentrations are about $10^9 cm^{-2}$ before and after oxidation, approaching the limited detection of TXRF tool. This means that metal removal efficiency is very high using IMEC-clean.

For the contaminated wafers, the Al surface concentration was about $4.7\times10^{12}cm^{-2}$ and $3.9\times10^{10}cm^{-2}$ before and after gate oxidation by AAS measurement. Zr surface concentration was about $5.4\times10^{12}cm^{-2}$ and $3.8\times10^{10}cm^{-2}$; for Ta about $4.2\times10^{12}cm^{-2}$ and $4.4\times10^{10}cm^{-2}$ before and after oxidation by TXRF tool, respectively. It has been found that for all three metals, contamination loss

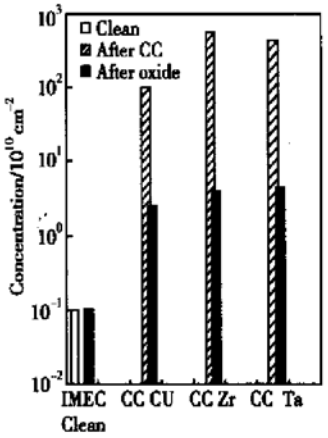


Fig. 1 Metal surface concentration measured by TXRF for Zr, Ta and by AAS for Al

is very great after gate oxidation under investigation.

### 3.2 *I–V* characteristics of 2.5nm gate oxide of clean wafers

*I–V* characteristics are shown in Fig. 2(a) for the clean wafers with three areas of capacitors. One can see that *I–V* curves are repeated well for each area of capacitors. Figure 2(b) shows Weibull plots of the $Q_{BD}$ distribution of MOS capacitor structures of the clean wafers. It is found that the Weibull slope, the 63%-value of the breakdown distribution becomes area almost independent on 2.5nm ultra-thin gate oxide and tightly grouped. But it is obvious that the plot is smaller shifted to left with an increase of capacitor area. This suggests that the $Q_{BD}$ values of the distribution decrease very little with the increase of area.

The conclusion is made according to the results above: (1) the $Q_{BD}$ value of distribution increases very small with decreasing capacitor area. (2) the Weibull slope (which is a measure of the spread of the distribution) is independent on capacitor area under investigation. This means that the quality of ultra-thin gate oxide of 2.5nm is perfect using IMEC-clean recipe and defined as a reference.

### 3.3 Effect of metal contamination on GOI

The following will be discussed that the effect

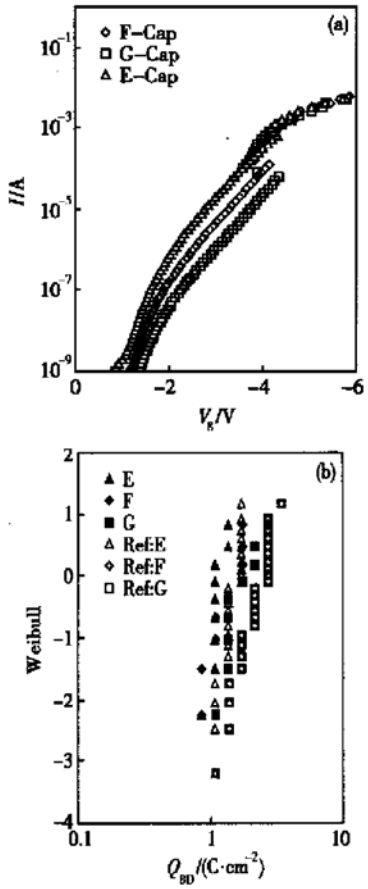


Fig. 2 *I–V* curves (a) and Weibull plots (b) of the $Q_{BD}$ distribution of MOS capacitors of the clean wafers for E-, F-, G-capacitors

of each metal contamination on GOI in details, respectively.

It can be found for the wafer contaminated by Al that *I–V* curves are plotted in Fig. 3(a) while they are also agreed well for each area of capacitors and reproducible well. Compared to the reference wafer, $Q_{BD}$-distributions of wafer contaminated by Al, are greatly similar to these of the references.

For the wafer contaminated by Zr, *I–V* curves are plotted in Fig. 4(a) with three area capacitors. It is found that *I–V* curves are also agreed well for each area of capacitors and reproducible well. However, it can be observed clearly in Fig. 4(b) that the Weibull slope, the 63%-value of the breakdown distribution decreases significantly with the capacitor area contaminated by Zr. Compared to the reference wafer, $Q_{BD}$-distributions of capacitors contaminated by Zr is greatly far away.

For Ta contamination, it can be seen that $I$–$V$ curves plotted in Fig. 5 are not good while early breakdown has happened to each area of capacitors.

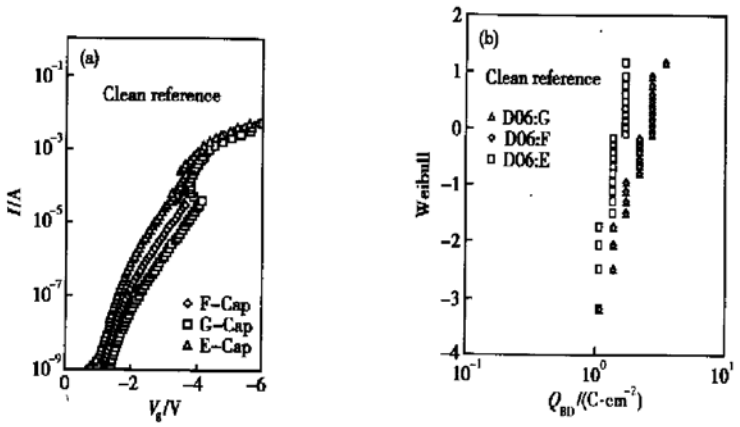


Fig. 3　(a) $I$–$V$ curves of MOS capacitors contaminated by Al; (b) Weibull plot of the $Q_{BD}$ distribution of comparison of wafer contaminated with reference wafer.

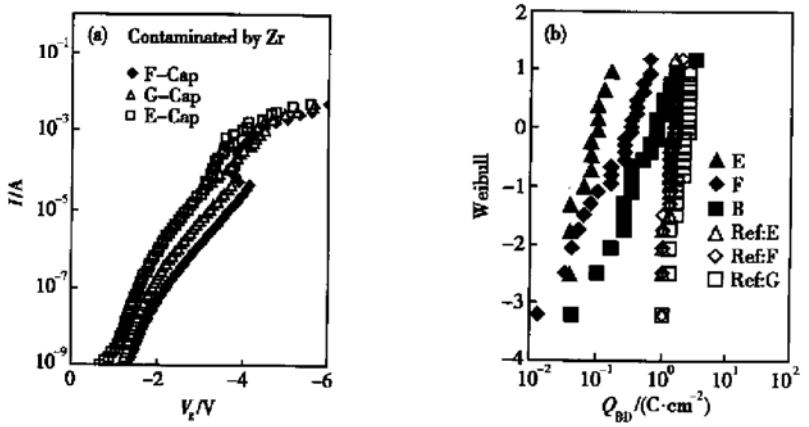


Fig. 4　(a) $I$–$V$ curves of MOS capacitors contaminated by Zr; (b) Weibull plot of the $Q_{BD}$ distribution.

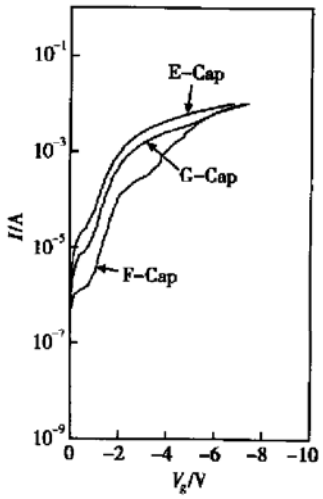


Fig. 5　$I$–$V$ curves of MOS capacitors of wafers contaminated by Ta: E-, F-, G-Cap.

It is well known that a redistribution of metal surface concentration upon thermal oxidation is much different between metals due to vapor pressure, or diffusivity or solubility in silicon at some temperature. Metal can diffuse into silicon substrate due to its solubility and diffusion constant in the silicon at the oxidation temperature. The diffusivity and solubility of some metals in silicon and vapor pressure of metals at 800℃ is shown in Table 1 from Ref. [1].

It can be seen in Table 1 that, for Al contamination, vapor pressure is the largest about $6.44\times10^{-5}$Pa. The most Al is gone out into gas phase so that Al contaminantion can be purged out of the furnace. Our results agree well with one in Ref.

[3]. It was found that Al exists in the top surface of the oxide and its concentration decreases as the $SiO_2$/Si interface draws near. They suggest that the presence of Al in the top layer of the oxide film minimizes the degradation of device characteristics. It is very consistent with the fact that the Weibull slope is almost similar to the reference (clean wafer), and $Q_{BD}$-distributions of E-capacitor were made very little shift to left in comparison with the reference wafer in this work.

Table 1 Diffusivity, solubility of metals in silicon and vapour pressure of metals

| Element | Mass /a.m.u | Diffusivity at 800℃/ ($cm^2 \cdot s^{-1}$) | Solubility at 800℃ /$cm^3$ | Vapor pressure at 800℃/Pa |
|---|---|---|---|---|
| Zr | 91.224 | | | $1.80\times10^{-17}$ |
| Ta | 180.948 | $< 1.0\times10^{-15}$ | $< 3.00\times10^{13}$ | $3.44\times10^{-27}$ |
| Al | 26.98 | $3.9\times10^{-16}$ | $1.19\times10^{19}$ | $6.44\times10^{-5}$ |

However, for Zr, vapor pressure is very low at about $1.80\times10^{-17}$Pa and it is not known about diffusivity and solubility of Zr. We can see in Fig. 4 (b) that Weibull slope decreases significantly, compared to reference wafer, $Q_{BD}$-distributions of wafer contaminated by Zr, it is also greatly changed though the data of TXRF told us the Zr surface concentration was $3.8\times10^{10}$ atoms/$cm^2$ after gate oxidation. This means that it is very serious of the effect of Zr contamination on the characteristics of the ultra-thin gate oxide.

Ta contamination gives no good results. One of possibilities could be due to the Ta standard stock containing HF. Ta metal solution consists of 1000 μg/ml in 0.5% HF for ICP standard. And then spinning solution contains 1w-ppm Ta while concentration of HF is $5\times10^{-6}$(v/v). This means that for these wafers, the surfaces were etched slowly by HF solution due to evaporation so that the roughness of wafer surface could seriously influence the quality of ultra-thin gate oxide of "2.5nm". This suggests that other Ta standard stocks will be used when Ta contamination experiment is carried out.

## 4 Conclusion

In this work we have investigated the characteristics of ultra-thin gate oxide (2.5nm thickness) and the effect of metal contamination on GOI. In conclusion, it could be found as follows: (1) The quality of ultra-thin gate oxide of 2.5nm is perfect for cleaning wafers using IMEC-clean according to the $Q_{BD}$ value of distribution and Weibull slope independent on capacitor area under investigation condition. (2) It was not observed about the effect of Al contamination on GOI. (3) It was found early breakdown had happened for wafers contaminated by Ta. It is assumed that one of possibilities could be due to the Ta standard stock containing HF. It needs to be proved.

### References

[1] Bearda T. Gate oxide evaluation by characterisation of oxide breakdown. Thesis for PhD, 2001

[2] Heyns M M, Cornelissen I, Mertens P W, et al. Developments in cleaning technology for critical layers. IMEC Papers on Ultra Clean Processing Silicon Surface (UCPSS) 2000, A14: 124

[3] Lim S W, Machuca F, Liao Hongmei, et al. Effect of initial Al contamination on ultrathin gate oxides. JES, 2000, 147(6): 1136

[4] De Gendt S, Sne P, Cornelissen I, et al. Vapor phase decomposition-droplet collection evaluation of a wafer surface preparation system. IMEC Papers on UCPSS 1999, A14: 289

# 金属沾污对超薄栅氧(2.5nm)特性的影响

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**摘要**: 采用可控的金属沾污程序,最大金属表面浓度控制在 $10^{12}cm^{-2}$数量级,来模拟清洗工艺最大可能金属沾污表面浓度.利用斜坡电流应力和栅注入方式测量本征电荷击穿来评估超薄栅氧特性和金属沾污效应.研究了金属锆和钽沾污对超薄栅氧完整性的影响.实验结果表明金属锆沾污对超薄栅氧完整性具有最严重危害;金属钽沾污的栅氧发生早期击穿现象,而金属铝沾污对超薄栅氧完整性没有明显影响.

**关键词**: 栅氧完整性; 金属沾污; 本征电荷击穿; 斜坡电流应力; MOS 电容器

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