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CEE-Gr: A Global Router with Performance Optimization Under Multi-Constraints*

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Abstract: A global routing algorithm with performance optimization under multi-constraints is proposed, which studies RLC coupling noise, timing performance, and routability simultaneously at global routing level. The algorithm is implemented and the global router is called CEE-Gr. The CEE-Gr is tested on MCNC benchmarks and the experimental results are promising.

Key words: VLSI/ULSI; physical design; global routing; multi-constraints; performance optimization
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1 Introduction

As VLSI/ULSI technology moves into very deep sub-micron (VDSM) device size and gigahertz clock frequencies, performance optimization becomes an increasingly dominant factor in global routing[1,2] besides traditional congestion optimization[3~5]. It brings two major concerns for performance optimization. One is interconnect delay reduction. The other is coupling noise estimation and elimination.

Previous works[6~18] have various contributions to timing optimization for global routing, which includes timing models[6,7], timing-driven Steiner tree algorithms[8,9], interconnect design algorithms considering buffer insertion or/and wire sizing[10~12], and timing optimization global routing algorithms[13~19].

Increasing concerns have been raised regarding the coupling noise effects. There have been some works focusing on the noise reduction. These approaches mainly fall into two categories: noise modeling[20~23] and noise minimization[24~29]. Among noise minimization algorithms, most optimizations are done after the process of global routing.

The noise minimization introduced in Refs. [24, 25] is done after the detailed routing phase. Spacing algorithm proposed in Ref. [24] expands the distance between sensitive nets to reduce crosstalk. It uses Lagrangian relaxation technique and is efficient for non-congested routing regions. The track permutation algorithm[25] swaps tracks

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to avoid crosstalk for grid detail routing. It solves a mixed integer linear programming to decide which track should be permuted. Similar to the spacing algorithm, it is efficient for routing area with more unused tracks.

References[26, 27] introduced detailed routing algorithms to minimize crosstalk. Reference[26] introduced the wire perturbation algorithm. By defining BPI (basic perturbation interval), it can accurately calculate the best wire position to minimize crosstalk. But in order to obtain optimal solution, this algorithm consumed much time. Crosstalk minimization algorithm for river routing was proposed in Ref. [27]. It minimized crosstalk by converting two adjacent parallel wires into stair-shaped wires and using net flow method to distribute resource in the river routing region. With fixed pin on the top/bottom in the riverside, there is a limitation of its minimization capability.

Some algorithms reduce crosstalk after global routing. One is the two-part algorithm, region-based crosstalk risk estimation and crosstalk reduction, described in Ref. [28]. There is a high timing complexity in part two. Reference[29] proposed the iSINO algorithm. It eliminates crosstalk by inserting shields.

Researchers find that it is more flexible if they reduce noise in the process of global routing. A few recent works[30, 31] have addressed crosstalk avoidance techniques throughout global routing phase. In Ref. [30], global routing with crosstalk constraints has been studied. It constructs Steiner tree with a cost function including crosstalk consideration. If the crosstalk of initial routing solution still exceeds the given bound, then do rip up. Reference [31] proposed the GSINO algorithm. It gives a Steiner tree cost function containing the estimated shield number. Thus, the global router can reduce the total shield number and eventually reduce the total routing area. The objective of the two algorithms is to minimize crosstalk effects. Both of them do not take timing and congestion optimization into consideration. Among these approaches, there is still an absence of performance (including coupling noise, timing, and routability) optimization algorithms for global routing.

The main contribution of this paper is that the coupling noise, timing performance, and routability are studied simultaneously at global routing level. Regarding wire length as the objective and letting timing, RLC coupling noise, and routability be the constraints, this paper presents a performance optimization global routing algorithm under multi-constraints. This algorithm has been implemented and the global router is called CEE-Gr.

2 Preliminaries

2.1 Definitions

We assume that the whole chip is divided into a rectangular array of $N_{row} \times N_{col}$ cells called global routing cells (GRCs). Global routing graph(GRG) is the dual graph of GRCs, which is composed of the gridlines and crossings. Figure 1 shows an example GRG that holds 4×4 GRCs. Node v_i represents the center point of GRC_i. The edge links node v_i and node v_j is named as e, l is called the length of edge e, which equals the distance between node v_i and node v_j. A non-negative number c_e, called edge capacity, is assigned to the edge e. c_e indicates the number of available tracks between every two corresponding GRCs.

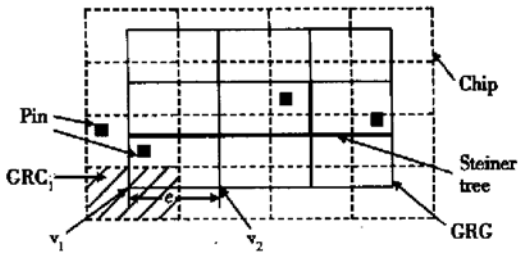

Fig. 1 Global routing graph(GRG)

Thus, a net can be specified as a set of nodes in GRG. Then, the problem of routing a net in GRG can be described as a Steiner tree problem of specified nodes in GRG.

2.2 Notations

The following notations are used in this paper.

N	the set of nets.
E	the set of GRG edges.
E_h	the set of horizontal GRG edges.
E_v	the set of vertical GRG edges.
CLM	one column of horizontal edges.
ROW	one row of vertical edges.
N_n	the total number of nets.
N_e	the total number of GRG edges.
l_t	the length of edge t.
f_t	the number of used tracks in edge t.
f_{max}	the maximum f for all edges.
h(CLM)	the number of used tracks in CLM.
h_{max}	the maximum h for all CLMs.
w(ROW)	the number of used tracks in ROW.
w_{max}	the maximum w for all ROWs.
γ	weight factor, between 0 and 1.
θ	weight factor, between 0 and 1.
sn_t	shield number in edge t.
o_t	obstacles in edge t.
c_t	capacity of edge t.
$T(i,j)$	delay from source i to sink j.
$T_D(i,j)$	delay constraint from souce i to sink j.
$s(i)$	sink set of net i.
$e(i)$	edge set of net i.
K_{ij}	LSK value of source sink pair i,j.
$\overline{K_{ij}}$	LSK bound of source sink pair i,j.
K_{it}	LSK value of net segment i in edge t.
$\overline{K_{it}}$	LSK bound of net segment i in edge t.
$k_{i,j}$	coupling coefficient between net i,j.
L_{ij}	mutual inductance between net i,j.
L_i	self inductance of net i.
α_t	a parameter related to sensitive rate.
β_t	a constant for edge t.
S_{it}	marker to indicate whether edge t contains net i.
L	total wire length.

2.3 Problem formulation

Let

$$S_{it}=\begin{cases}1, \text{edge } t \text{ is used by the Steiner tree of net } i\\ 0, \text{otherwise}\end{cases}$$

That means, S_{it} is a kind of marker to indicate whether the edge t contains net i.

Then we get the following problem formulation:

$$\text{Minimize} \quad L = \sum_{i=1}^{N_n}\sum_{t=1}^{N_e} S_{it} l_t$$

Subject to:

$$f_t = \sum_{i=1}^{N_n} S_{it} + sn_t + o_t \leqslant c_t, \forall\, t \in E \tag{1}$$

$$T(i,j) \leqslant T_D(i,j), \forall\, i \in N, \forall\, j \in s(i) \tag{2}$$

$$K_{ij} \leqslant \overline{K_{ij}}, \forall\, i \in N, \forall\, j \in s(i) \tag{3}$$

Formula (1) is the congestion constraint, which forbids the overflow on each GRG edge. Formula (2) guarantees that the actual delay value of source i to sink i. $T(i,i)$ is no more than its corresponding timing constraint $T_D(i,j)$, and formula (3) sets the upper bound of LSK, $\overline{K_{ij}}$ for each source sink pair i,j, and the actual LSK value of this pair, K_{ij} could not exceed that.

3 RLC noise model

The LSK model for RLC crosstalk[23,31] is used in this paper. Different from earlier noise models[20,21], the LSK model considers coupling inductance between adjacent and non-adjacent sensitive nets and points out coupling inductance could not be ignored while clock frequency is more than 1GHz.

For any two net segments N_{it} and N_{jt} in GRG edge t, the inductive coupling coefficient between them is

$$k_{it,jt} = \frac{L_{it,jt}}{\sqrt{L_{it}L_{jt}}} \tag{4}$$

where $L_{it,jt}$ is the mutual inductance between N_{it} and N_{jt}, and L_{it} and L_{jt} are the self inductance for N_{it} and N_{jt}, respectively. A formula-based K_{eff} model has been developed in Ref. [23] to calculate the coupling coefficients $k_{it,jt}$. Furthermore, the total amount of inductive coupling induced on N_{it} can be

represented by the sum of the inductive coupling coefficients.

$$K_{it} = \sum_{j \neq i} k_{it,jt} \tag{5}$$

For all net segments N_{jt}'s are sensitive to N_{it}.

To consider the effect of interconnect length and the general case where the total coupling is not uniform in all routing regions, a length-scaled K_{eff} (LSK) model was proposed in Ref. [31], where the LSK value is defined as

$$K_{ij} = \sum_{t} l_t K_{it} \tag{6}$$

where l_t is the length of edge t and K_{it} is total coupling for N_{it}.

4 Global router CEE-Gr

4.1 Outline of CEE-Gr

The global router CEE-Gr consists of two parts:

(1) Gr: timing and congestion optimization.

(2) CEE: crosstalk estimation and elimination.

Gr firstly generates an initial routing solution considering congestion and timing optimization. Then, CEE eliminates the crosstalk from the solution by inserting shields and gets a mid-result. Finally, regard the mid-result as input and send it to Gr for iterations. The flow chart of CEE-Gr is shown in Fig. 2.

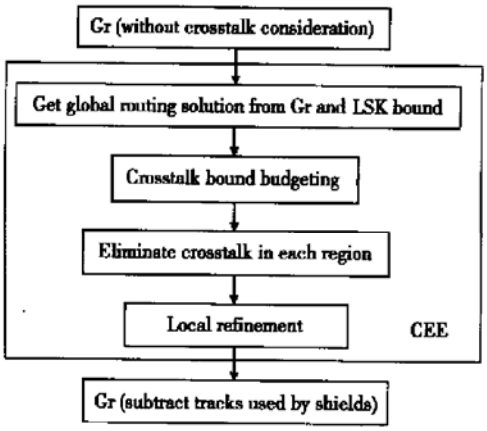

Fig. 2 The flow chart of CEE-Gr

The pseudo code of CEE-Gr is as follows:

Step1, Call Gr to generate a minimum wire length initial solution X_0 without congestion and timing violation;

Step2, X_1= CEE(X_0);

Step3, If (no edge overflow in X_1) do go to step4;
Else do go back to step1 to generate a new solution;

Step4, X_2= Gr(X_1);

Fig. 3 Pseudo code of CEE-Gr

4.2 Part One: Gr

The objective of Gr is wire length and the constraints are congestion and timing. The timing analysis and optimization method used in Gr follows critical-network-based technology introduced in Ref. [17].

To reduce congestion, Gr uses SSTT (search space traversing technology)[2] and considers independent of net ordering[3].

4.3 Part Two: CEE

The flow chart of CEE is shown in Fig. 2. This sub-section introduces CEE in detail.

(1) LSK bound budgeting: We partition the LSK bound at each sink of a net into the GRG edges belonging to the source-sink paths. There are two strategies for budgeting:

(a) CBUD (uniform distributed crosstalk budgeting) strategy

This strategy uniformly partitions the LSK bound into edges according to their length, and it is based on formula:

$$\overline{K_{it}} = \frac{\overline{K_{ij}}}{l_t} \tag{7}$$

If the segment N_{it} is shared with multiple paths starting from the same source to different sinks, we use the minimum value computed for these paths according to Eq. (1).

(b) CBLP (linear programmed crosstalk budgeting) strategy

CBUD distributes LSK bound according to segment length without consideration of its congestion. To overcome this shortcoming, CBLP parti-

tions the LKS bound by solving a linear programming problem.

In one dimension case, there are only horizontal wires routing in one row. Using the notations above, the one dimensional problem could be described as

Minimize $f_{\max} = \max\{f_t \mid \forall t \in E\}$

Subject to

$$\sum_{i \in t} \alpha_t \overline{K_{it}} + \beta_t + \sum_{i=1}^{N_n} S_{it} + O_t \leqslant f_{\max}, \forall t \in E \tag{8}$$

$$\sum_{t \in e(i)} l_t \overline{K_{it}} \leqslant \overline{K_{ij}}, \forall i \in N \quad \text{and} \quad \forall j \in s(i) \tag{9}$$

$$\sum_{i \in t} \alpha_{it} \overline{K_{it}} + \beta_t \geqslant 0, \forall t \in E \tag{10}$$

The left of Eq. (10)

$$\sum_{i \in t} \alpha_{it} \overline{K_{it}} + \beta_t = sn_t$$

is an experiential equation representing the shield number in edge t obtained in Ref. [29], so it could not be negative. α_{it} is a parameter related to sensitive rate, and β_t is a constant for edge t.

For the two-dimensional problem, we can derive similar formula below:

Minimize $\gamma h_{\max} + \theta w_{\max}$

Subject to

$$\sum_{t \in \mathrm{CLM}} \left(\sum_{i \in t} \alpha_t \overline{K_{it}} + \beta_t + \sum_{i=1}^{N_n} S_{it} + O_t \right) \leqslant h_{\max}, \quad \forall \mathrm{CLM} \in E_h \tag{11}$$

$$\sum_{t \in \mathrm{ROW}} \left(\sum_{i \in t} \alpha_t \overline{K_{it}} + \beta_t + \sum_{i=1}^{N_n} S_{it} + O_t \right) \leqslant w_{\max}, \quad \forall \mathrm{ROW} \in E_v \tag{12}$$

$$\sum_{t \in e(i)} l_t \overline{K_{it}} \leqslant \overline{K_{ij}}, \forall i \in N \quad \text{and} \quad \forall j \in s(i) \tag{13}$$

$$\sum_{i \in t} \alpha_{it} \overline{K_{it}} + \beta_t \geqslant 0, \forall t \in E \tag{14}$$

(2) Crosstalk elimination in each region: According to each $\overline{K_{it}}$ computed in step 4.3(1), this step applies simulated annealing method in each region to insert shields, so that the crosstalk of all regions is within bound value.

(3) Local refinement: Check each net to eliminate possible remnant crosstalk and delete unnecessary shields so the final area is minimized.

First, to eliminate remnant crosstalk, the net N_{it} with most critical crosstalk violation is chosen, and the shield will be inserted into the least congested region R_t on N_i's path.

Second, to reduce total area, the most congested region R_j is chosen, and the slack $K_i - K_{th}$ of all nets in R_j is computed. If possible, shield could be deleted when K_{th} increases properly.

The pseudo code of CEE is as follows:

1. Get X_0, LSK bound at each net sink and remnant GRG resources on each edge as input.
2. For (each global routing tree in X_0) do:
   Distribute LSK bound at sink point onto each GRG edge this tree occupies, the result is $\overline{K_{it}}$ for net i in edge t. CBUD or CBLP strategy could be applied for this calculation.
3. For (each GRG edge) do:
   Calculate the actual LSK value K_{it} with LSK model for each net in this edge.
   Compare K_{it} with $\overline{K_{it}}$.
   If (all K_{it} is no more than $\overline{K_{it}}$) do go for next edge.
   Else, apply simulated annealing method to eliminate crosstalk in this edge.
4. For (each GRG edge) do:
   Calculate K_{it} with LSK model for each net in this edge to verify non-violation, if find any remnant crosstalk violation, insert one shield, and recalculate.
5. For (each GRG edge) do:
   If (there is at least one shield in this edge) do
   5a. Remove one shield from this edge and calculate K_{it} with LSK model for each net in this edge.
   If (no violation) do, go back to 5a.
   Else, add one shield and go for next edge.

Fig. 4 Pseudo code of CEE-Gr

5 Experimental results and discussion

The global router CEE-Gr is implemented in the C language. It runs on a SUN V880 workstation with Unix OS. There are two running modes: T mode is timing-driven mode; W mode is non-timing-driven mode. We only reduce congestion in W mode, and optimize both congestion and timing performance in T mode.

5.1 Benchmark Data

We tested three MCNC benchmarks under 0.2μm technology. Sensitivity rate of 0.5 is given to all nets and a random sensitivity matrix is created. LSK bound at each sink is set to be 1000. Table 1 summarizes the benchmark data sets.

Table 1 Benchmark data

Circuit	Number of net	Grid
C2	745	9×11
C5	1764	16×18
C7	2356	16×18

5.2 Results

The experimental results are shown in Tables 2 and 3.

5.3 Discussion

(1) The crosstalk is serious in the initial routing solution of all these test cases. CEE-Gr can eliminate all crosstalk by adding shields. CEE-Gr is efficient in crosstalk estimation and elimination.

(2) Row 4 in Table 2 shows that the increase in wire length of CEE-Gr is only from 2% to 4%, and when the circuit scale goes larger, the increase ratios get smaller.

(3) The minimum redundancy of delay (requiredDelay-currentDelay), denoted as Min-R in Table 2 and shown in row 9 and raw 10 in Table 2, is almost unaffected. So, CEE-Gr maintains the effectiveness in timing optimization of Gr.

(4) We notice that the CBLP strategy consumes more routing area (see row 5 and row 10 in Table 3) than CBUD strategy since CBLP inserts more shields. The reason is that the objective function of the linear programming problem is to minimize the track utility of the most congested GRG edges. To do that, it must give such edges a relative high $\overline{K_{iu}}$, so $\overline{K_{iu}}$ of many other edges is set very low

Table 2 Comparison between Gr and CEE-Gr with CBUD

Circuit		C2	C5	C7
W mode	(Gr) Wire length/μm	459786	1297814	1545454
	(CEE-Gr) Wire length/μm	473588	1336102	1564408
	Increase in wire length	3.00%	2.95%	1.23%
	Overflow edge number	0	1	0
T mode	(Gr) Wire length/μm	466288	1298210	1569038
	(CEE-Gr) Wire length/μm	468836	1326670	1570882
	Increase in wire length	0.55%	2.19%	0.16%
	(Gr) Min-R	-0.007417	0.006431	0.000910
	(CEE-Gr) Min-R	-0.006042	0.010355	0.003196
	Overflow edge number	0	1	0

Table 3 Comparison between CBUD and CBLP in CEE-Gr

Circuits		C2	C5	C7
Wire length of Gr in W mode/μm		459786	1297814	1545454
Sink number that violates the crosstalk bound		583	1570	1845
CEE-Gr (CBUD)	Shield number	158	483	595
	Area	154×200	273×298	346×380
	Wire length/μm	473588	1336102	1564408
	Increase in wire length	3.00%	2.95%	1.23%
	Overflow edge number	0	1	0
CEE-Gr (CBLP)	Shield number	422	1315	1769
	Area	150×229	267×343	344×448
	Wire length/μm	478240	1330950	1580938
	Increase in wire length	4.01%	2.55%	2.30%
	Overflow edge number	3	2	3

or even zero. In order to satisfy such low or zero crosstalk bounds, much more shields must be inserted into these regions. Thus, it makes CBLP use much more shields than CBUD does.

(5) Using simulated annealing method to insert shields into each region makes CEE-Gr require long running time, which is about 40min for C2, and much longer for larger circuits.

6 Conclusion and future work

RLC coupling noise, timing performance, and routability in global routing phase are studied in the paper. A multi-constraint performance optimization global router, called CEE-Gr, is presented. The experimental results are promising. The experimental results show that the CEE-Gr router is able to do as follows:

(1) Tackle coupling noise, timing performance, and routability simultaneously;

(2) Take coupling inductance into consideration;

(3) Obtain good routing results;

(4) Efficiently eliminates crosstalk throughout the process of global routing by inserting shields, which has little influence on wire length and timing performance.

As future work, we plan to reduce the time complexity of CEE-Gr and find better strategies for bound partitioning.

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CEE-Gr: 一个在多约束下进行性能优化的总体布线器*

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摘要: 提出了一个在多约束下进行性能优化的总体布线算法. 研究了在总体布线阶段同时进行 RLC 耦合噪声(串扰)、时延性能和布线拥挤优化的问题. 根据所提出的算法思想已实现了相应的总体布线器: CEE-Gr. 并对所实现的总体布线器 CEE-Gr 进行了 MCNC 电路例子的测试, 得到令人满意的结果.

关键词: VLSI/ULSI; 布图设计; 总体布线; 多约束; 性能优化

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