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New Forward Gated-Diode Technique for Separating Front Gate Interface- from Oxide-Traps Induced by Hot-Carrier-Stress in SOI-NMOSFETs*

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Abstract: The front gate interface- and oxide-traps induced by hot-carrier-stress in SOI-NMOSFETs are studied. Based on a new forward gated-diode technique, the R-G current originating from the front interface traps is measured, and then the densities of the interface- and oxide-traps are separated independently. The experimental results show that the hot-carrier-stress of front channel not only results in the strong generation of the front interface traps, but also in the significant oxide traps. These two kinds of traps have similar characteristic in increasing with the hot-carrier-stress time. This analysis allows one to obtain a clear physical picture of the effects of the hot-carrier-stress on the generating of interface- and oxide-traps, which help to understand the degradation and reliability of the SOI-MOSFETs.

Key words: SOI-NMOS device; hot-carrier-effect; interface traps; oxide traps; gated-diode
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1 Introduction

The interface and oxide traps seriously degrade the performance and also influence the lifetime of MOSFET devices[1,2]. For SOI N-MOSFET devices, this effect becomes more evident due to the existing of the interfaces and the coupling of each other of front and back oxide-semiconductor[3,4]. In this case, extraction or measure of interface and oxide-traps are very important work in modeling of the performance and designing of the device structure.

However, the analysis of hot-carrier-stress (HCS) which induced degradation of SOI-MOSFETs is a complicated problem due to the dual channel and the front-back-interface coupling effect[5,6]. Most of the previous studies only used the channel current or transconductance as the monitor of the induced degradation in SOI-NMOSFETs. The kinds of methods often do not allow clear separation of the interface-traps from the oxide-traps generation.

Recently, the forward gated-diode method has been used to characterize the interface traps and to extract the bulk carrier recombination lifetime in

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the SOI devices. By extracting recombination-generation (R-G) current, some very good results have been achieved[7~12]. It has been shown that the method is simple, sensitive, quickly applicable and nondestructive.

In this paper, a new forward gated-diode technique is presented to study the separation of the front gate interface- traps from the oxide- traps due to the hot-carrier-stress in SOI-NMOSFETs. Due to the unique feature of the forward gated-diode method, the amplitude of its R-G peak current only depends on the interface traps while the critical gate voltage associated with the R-G peak current is related with the interface- and oxide-traps induced[7,11]. From the analysis of the height and position shift of R-G peak current, this method enables us to separate the interface-traps from oxide- traps effectively. The validity of this method has been verified experimentally in this paper.

2 Principle of measurement

The diode operates in the sub-threshold region when the small forward bias ($V_b < 0.7$V) is applied to the gated-diode. Thus, the diode current comprises a small diffusion current component and a large R-G current component arising from the recombination-generation mechanism of the front interface traps. According to the SRH theory, the maximum rate of the recombination will occur when the front interface potential coincides with the intrinsic Fermi level or N_s-P_s. By scanning the front gate voltage to make the front interface potential vary from the accumulation to depletion. The maximum recombination condition will be satisfied along the channel region from the edge of source toward the edge of drain. As a result, the diode current demonstrates a sharp peak at certain critical gate voltage, which arises from the contribution of the generation-recombination via interface traps, as shown in References[7~12].

Based on the discussion mentioned above, it can be concluded that the hot-carrier-stress induced interface traps which contribute an increase of the R-G current, leading a significant increase in the diode R-G peak current. Thus this increased amplitude can be used in determining the density of induced interface traps. Following the stress, the increased R-G current component induced by the hot-carrier-stress can be simply modeled

$$\Delta I_{\text{pure}} = I_{\text{peak-stress},j} - I_{\text{peak-origin}} \tag{1}$$

where j represents the j-th stress experiment; $I_{\text{peak-stress},j}$ represents the diode R-G peak current after the hot-carrier-stress and $I_{\text{peak-origin}}$ is defined as the diode R-G peak current before the hot-carrier-stress.

Thus, we can extract the values of increased R-G peak current from equation (1) for the different hot-carrier-stress time and bias voltage. Based on the SRH statistics theory, the relationship between the value of induced R-G peak current and the density of interface traps can be simply described by[7]

$$\Delta I_{\text{pure}} = \frac{1}{2} q n_i (c_n c_p)^{1/2} \Delta D_{it} A_G e^{\frac{qV_b}{2kT}} \tag{2}$$

where n_i represents the density of intrinsic carrier, ΔD_{it} represents the density of the induced interface traps, A_G is the effective area of gate, V_b is the diode forward voltage, and $c_n = c_p = 10^{-8}\text{cm}^{-3} \cdot \text{s}^{-1}$.

On the other hand, that the hot-carrier-stress induced interface- and oxide-traps will increase the critical gate voltage associated with the R-G peak current, demonstrating a significant shift of position in gate voltage at which the R-G peak current occurs. The amplitude of shift of critical gate voltage directly indicates the amount of generation of the interface- and oxide- traps. This effect can be expressed as

$$\Delta V_{\text{G-peak}} = V_{\text{G-peak-stress},j} - V_{\text{G-peak-origin}} = \Delta V_{it} + \Delta V_{ot} \tag{3}$$

where $V_{\text{G-peak-stress},j}$ represents the position of diode R-G peak current after the hot-carrier-stress experiment and $V_{\text{G-peak-origin}}$ is defined as the position of diode R-G peak current before the hot-carrier-stress. $\Delta V_{it} = \dfrac{q\Delta D_{it} - e\Phi_t}{C_{ox}}$ and $\Delta V_{ot} = \dfrac{qN_{ot}}{C_{ox}}$ repre-

sent the R-G peak current and voltage shift due to the interface traps and oxide traps, respectively.

Since the density D_{it} of generated interface traps has been calculated from the increased height of the R-G peak current, the density N_{ot} of generated oxide trap can also be determined from equation (3). Thus, by the means of shift of the R-G peak current, the oxide traps induced by the hot-carrier-stress can be readily measured directly.

In order to avoid the influence of the back gate interface, we have to measure the R-G current by scanning the front gate voltage when the back gate interface is forced into the strong accumulation by using a negative back gate voltage. As a result, the measured R-G current only reflects the effect of front gate interface traps due to the hot-carrier-stress.

3 Experiments and measurement

The devices used in this study were SOI-NMOSFETs made in SIMOX wafers with n^+-poly gate. The final thickness of the gate oxide, the silicon film and the buried oxide were 20, 160 and 400nm, respectively. The impurity concentration in the silicon film was adjusted to about $10^{16}cm^{-3}$. The channel length is 4μm with the width of 8μm. A body contact was made on one side of the MOSFET for the gated-diode measurement. The top view of the device is shown in Fig. 1, which consists of the source and drain/body n^+p junction.

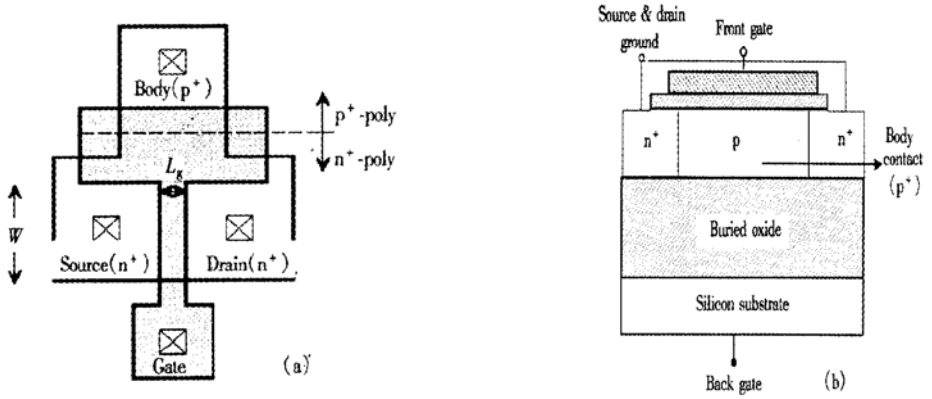

Fig. 1　Top view of the fabricated SOI device (a) and diagram of the experimental set-up (b)

In the measurement, the source and drain are connected to ground while applying biased voltage V_b to the body contact. As a result, the source and drain/body contact formed a forward diode. Based on the principle of measurement discussed above, by scanning the front gate voltage, the R-G current originating from the front gate interface- and oxide-traps was obtained under the condition of back gate voltage V_{g2} of − 10V for the back interface into the strong accumulation. In order to perform a hot-carrier-stress experiment, we applied a constant gate voltage of 0.55V and drain voltage of 6V to the respective contacts while the source and body contacts were grounded. The accumulated stress time is changed from 0s, through 20, 60, 100, 200, 500, 1000s, finally to 5000s. The R-G current characteristics of the devices were automatically recorded by a semiconductor parameter analyzer HP-4156B after each stress duration.

4 Results and discussion

The plots of Fig. 2 show the diode current against the scanned front gate voltage, showing the evolution of the R-G current with the hot-carrier-stress time. As seen in this figure, following the stress, the sharp R-G peak current grows in magnitude, exhibiting accumulated stress-time dependence. It is also apparent that the hot-carrier-stress causes a positive shift of the critical voltage of the

front gate R-G peak current position, this can be explained by the electron-hole pairs generation due to the hot-carrier-stress. And then electron were trapped at the front gate oxide layer.

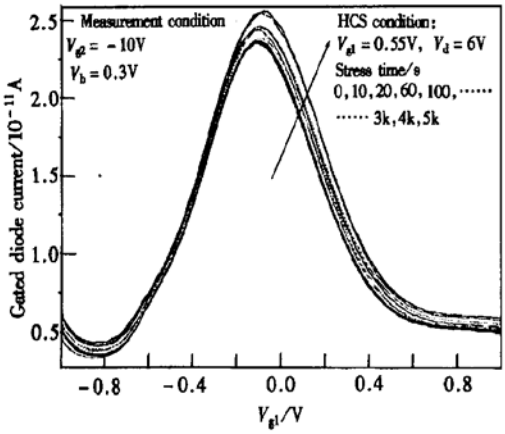

Fig. 2 Front interface R-G current versus the front gate voltage curves at the different hot-carrier-stress times

From these measurements, the R-G current component induced by the hot-carrier-stress was simply modeled with the equation (1) for the different stress time. And then, the induced front interface traps can be directly extracted with the equation (2) at the different hot-carrier-stress time. The results are shown in Fig. 3. As seen in this figure, the density of interface traps significantly grows with the accumulated stress time, exhibiting logarithmic time dependence. From these measured scatter points, we further revealed that the front interface-trap density induced by hot-carrier-stress increases in a power law with relationship of ΔN_{it}-t^n where the factor n is fitted to 0.7, as shown in Fig. 3.

Based on the obtained front interface traps, we extracted the induced oxide traps from the measured R-G peak current position and the equation (3). The calculated results are shown in Fig. 4. As seen in this figure, also does the induced oxide traps increase exponentially with an increase of the stress time, showing a quite same trend as that of the interface traps. The fit relationship of ΔN_{ot}-t^n is of the factor n of 0.85, a slightly larger than that of interface traps.

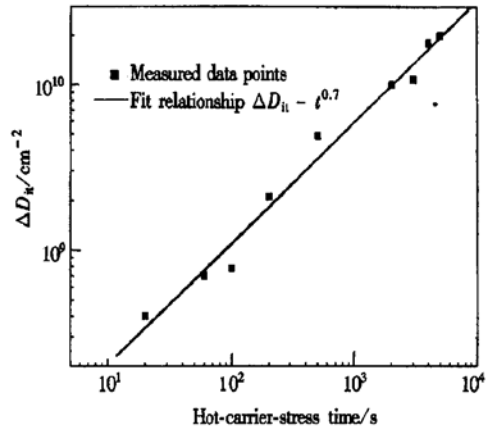

Fig. 3 Extracted and fit relationship between the density of front interface traps induced by hot-carrier-stress and the time of stress

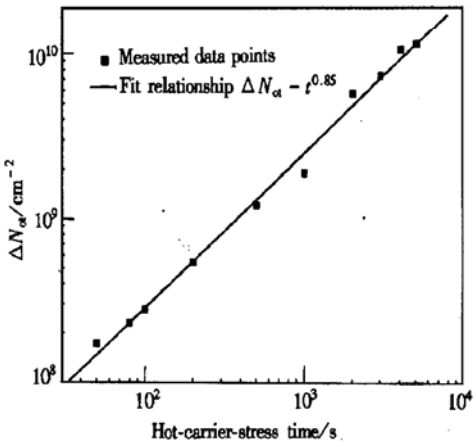

Fig. 4 Extracted and fit relationship between the density of front interface oxide trap induced by hot-carrier-stress and the times of stress

5 Conclusion

In this paper, the generation of the front gate interface- and oxide-traps due to the front channel hot-carrier-stress has been studied experimentally by a new forward gated-diode technique. Based on the measurement of the R-G peak current and its critical gate voltage associated with the hot-carrier-stress time, the induced interface- and oxide-traps have been extracted separately. The experimental results show that the increase of the oxide- and interface- traps with an increase of the hot-carrier-

stress time obeys the similar power-law relationship, indicating the close correlation of each other. This result can help to understand the hot-carriers generation dynamics and the degradation mechanism of the SOI-NMOSFETs.

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新的正向栅控二极管技术分离热载流子应力诱生 SOI NMOSFET 界面陷阱和界面电荷的研究*

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摘要：报道了用新的正向栅控二极管技术分离热载流子应力诱生的 SOI-MOSFET 界面陷阱和界面电荷的理论和实验研究. 理论分析表明：由于正向栅控二极管界面态 R-G 电流峰的特征，该峰的幅度正比于热载流子应力诱生的界面陷阱的大小，而该峰的位置的移动正比于热载流子应力诱生的界面电荷密度. 实验结果表明：前沟道的热载流子应力在前栅界面不仅诱生相当数量的界面陷阱，同样产生出很大的界面电荷. 对于逐渐上升的累积应力时间，抽取出来的诱生界面陷阱和界面电荷密度呈相近似的幂指数方式增加，指数分别为为 0.7 和 0.85.

关键词：热载流子应力效应；界面陷阱；界面电荷 R-G 电流；栅控二极管；SOI NMOSFET

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