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Unified Degradation Model in Low Gate Voltage Range During Hot-Carrier Stressing of p-MOS Transistors*

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Abstract: Hot-carrier effects of p-MOSFETs with different oxide-thicknesses are studied in low gate voltage range. All electrical parameters follow a power law relationship with stress time, but degradation slope is dependent on gate voltage. For the devices with thicker oxides, saturated drain current degradation has a close relationship with the product of gate current and electron fluence. For small dimensional devices, saturated drain current degradation has a close relationship with the electron fluence. This degradation model is valid for p-MOSFETs with 0.25μm channel length and different gate oxide-thicknesses.

Key words: hot carrier effects; p-MOSFET; degradation model, electron fluence
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1 Introduction

One of the most serious problems posed by the continuing integration of silicon CMOS transistors into the submicrometer gate length range is the hot carrier effects (HCE)[1~3], which occurs when energetic carriers cause interfacial damage or oxide trapping. The degradation of the resulting current drive of the transistors eventually causes circuit failure. Recently, more and more attentions have been paid to p-MOSFETs with the characteristic size scaling down. Although under the same bias, there are fewer hot carriers in p-MOSFET's than those in n-MOSFET's, they may create different kinds of device instabilities, which degrade small-dimension p-MOSFET rapidly[1]. In addition, several techniques for improving the hot carrier performance of n-MOSFETs do not necessarily work for p-MOSFET.

However, there are no satisfied degradation models for p-MOSFETs which can be applicable for different range of working conditions since the mechanism of p-MOS devices' degradation is more difficult to understand than that of n-MOSFETs'[1~3]. The purpose of this paper is to develop a unified degradation model in low range of gate voltage to give an empirical unified model for p-MOSFETs with different gate oxide-thicknesses. Experimental details are demonstrated in Section 2. The degradation mechanisms for p-MOSFETs in low gate voltage range are discussed in Section 3. A new degradation model which is responsible for p-MOS devices in low voltage range

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is developed in Section 4.

2 Experiment

In order to develop a unified model, we designed a series of experiments with stress voltages near the threshold voltage (V_{th}) of the device, which can be classified into 3 groups. All the devices have the same drain voltage stress. These 3 groups are as follows.

(1) The gate voltage ($|V_g|$) was always higher than $|V_{th}|$ of p-MOSFETs; ($|V_g| > |V_{th}|$)

(2) The device worked between overlapping region, which means that $|V_g| \approx |V_{th0}|$ (V_{th0} is the fresh threshold voltage) (or $|V_g| < |V_{th0}|$) was at first, then after a long period of stressing, it became $|V_g| < |V_{th}|$ (or $|V_g| > |V_{th}|$); ($|V_g| \approx |V_{th}|$)

(3) The device's gate voltage ($|V_g|$) was lower than threshold voltage ($|V_{th0}|$); ($|V_g| < |V_{th}|$) all the time

Conventional p-MOSFETs with oxides of 4.0 and 9.0nm and channel length of 0.25μm were employed. The thickness of oxide was measured by using high-frequency C-V method. All the devices were fabricated through the same standard CMOS processes. The stresses and normal I-V measurements were performed by means of precision semiconductor parameter analyzer HP4156B. All experiments were done at room temperature, i.e. 300K, and all the instruments were controlled by a PC using GPIB interface.

3 Degradation characteristics and mechanisms in low voltage range

Under the condition of first group ($|V_g| > |V_{th0}|$), after a long period of stressing, it was found that the degradation characteristics for 2 gate oxide-thicknesses are different. dI_{dsat} ($(I_{dsat} - I_{dsat0})/I_{dsat0}$) and ΔV_{th} ($\Delta V_{th} = V_{th} - V_{th0}$) are positive for 9nm gate oxide (V_{th0} is about -0.95V), while negative for 4nm gate oxide (V_{th0} is about -0.45V). In other words, $|I_{dsat}|$ increases with stressing time for 9nm p-MOSFET, while it decreases with stressing time for 4nm p-MOSFET. The shift of V_{th} (ΔV_{th}) is on the contrary to that of $|I_{dsat}|$. The possible reason of the difference of degradation characteristics for p-MOSFETs with different oxide-thickness may be that trapping oxide-volume decreases with the decrease of oxide-thickness and interface-state generation becomes more and more important in device degradation[3]. The exact reason needs further research. For simplicity, we use the absolute value of dI_{dsat} to compare the degradation characteristics of two gate oxide-thicknesses below.

V_g at all stress conditions for p-MOSFET with gate oxide of 4nm and 9nm are summarized in Table 1.

Table 1 Stress conditions ($V_d = V_{dd} = -4.6$V)

	9nm	4nm
(1)	-1.0	-0.50
(2)	-0.9	-0.45
(3)	-0.8, -0.7, -0.6, -0.5, -0.3, -0.1	-0.40, -0.35

Figure 1 shows the degradation characteristics of I_{dsat} under different stress voltages. For p-MOSFET with the same thickness, the higher stresses are, the more significant device degradation is. Figure 1 also shows that shift of dI_{dsat} for different thickness and different stress voltages is still logarithmic in time. The relationship can be expressed as:

$$D = t^{n(V_g)} \tag{1}$$

where n is the slope of degradation and dependent on stress voltage V_g. The n increases with the decrease of stress voltage ($|V_g|$) for different thicknesses of gate oxide. The increase of n with the decrease of $|V_g|$ means that the degradation mechanism changes with the change of stress voltage ($|V_g|$).

Figure 2 shows the relationship of n vs normalized stress voltage (V_g/V_{th0}) for different gate oxide-thickness. From the Fig. 2, it can be seen that n of different oxide-thicknesses has a linear rela-

tionship with V_g. The relationship can be expressed as:

$$n = a + bV_g \quad (2)$$

where $a = 0.64679$, $b = 0.50347$ for 9nm p-MOSFET, and $a = 1.88157$, $b = 2.54424$ for 4nm p-MOSFET. The a and b are two fitting parameters. This shows the higher the stress voltages are, the smaller the degradation slopes are.

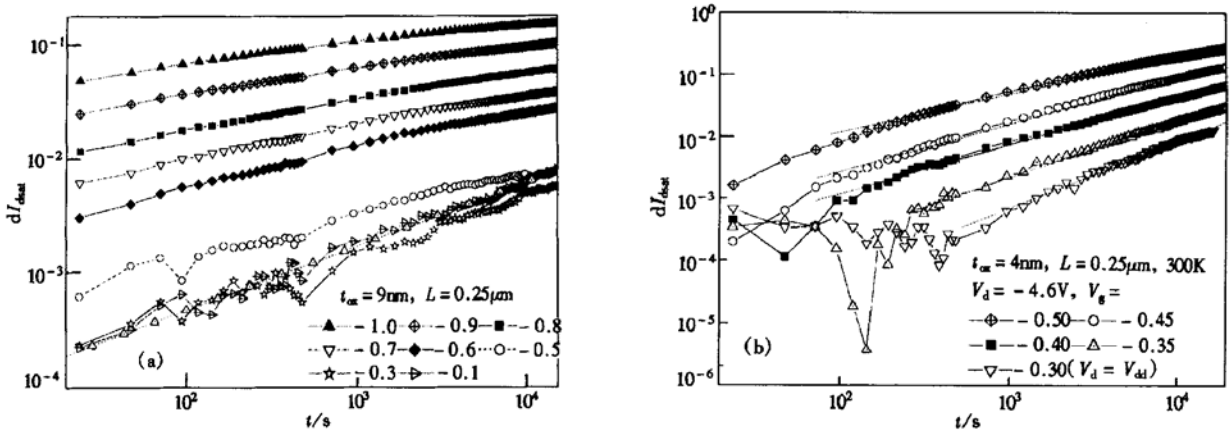

Fig. 1 dI_{dsat} degradation characteristics of p-MOSFET with 9.0nm(a) and 4nm(b) gate oxide The gradient varies with V_g. The higher stress voltages are, the smaller the slopes are.

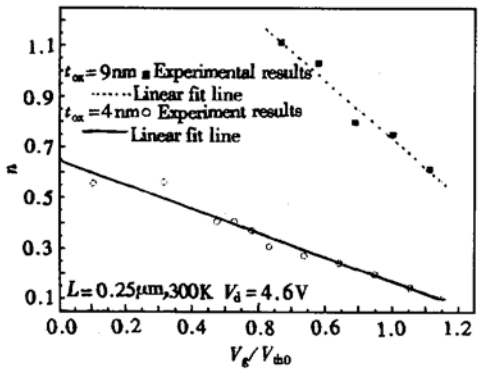

Fig. 2 Relationship of stress voltage V_g vs n

For 9nm gate oxide, n is about 0.2 under $|V_g| \geqslant |V_{th}|$ stress mode, but n is about 0.65 for 4nm gate oxide at the same stress mode. The value of 0.2 and 0.65 is typical for electron trapping and interface-state generation for p-MOSFET for dI_{dsat} degradation, respectively[5]. So the main degradation mechanism is electron trapping for 9nm and interface-states generation for 4nm when V_g is about V_{th}. For p-MOSFET with 9nm gate oxide, when $|V_g/V_{th0}|$ is about 0.5, n is 0.5, which is typical for interface-state generation[5]. When $|V_g/V_{th0}|$ decreases below 0.5, n becomes higher than 0.5. Hu *et al*. demonstrated that the slope for interface trap generation is expected to be between 0.5 (diffusion limited) and 1(reaction limited)[6]. So, the point ($V_g \approx V_{th}/2$) is the exact turning point of the change of degradation mechanism for 9nm gate oxide. This shows that the main mechanism of degradation for p-MOSFET with 9nm gate oxide will change from electron trapping to interface-states generation with the decrease of $|V_g|$.

For p-MOSFET with 4nm oxide, n is always larger than 0.6, so the device's main mechanism of degradation in the whole low voltage range is interface-trap generation. n increases to 1.1(> 1) when $|V_g/V_{th0}|$ decreases below 0.6, which seems to be contrary to Hu's model. The possible reason may be that quantum-mechanical effects become noticeable and leads to the accelerated degradation of threshold voltage, channel mobility and transconductance when the thicknesses of gate oxide decreases[8].

4 Unified degradation model in low voltage range

4.1 9nm p-MOSFETs

Figure 3 shows the relationship between I_{dsat}

degradation and electron fluence F_b times gate current I_g in low voltage range with stress conditions ranging from lower to higher gate voltages. As expected, the universal characteristics are valid for various drain voltages. It means that the values of I_gF_b are the same for different stress conditions when the I_{dsat} degradation reaches the failure criterion, though the lifetimes are different for different stress voltages. The failure criterion is set to be 10% of I_{dsat} degradation. It can be derived from Fig. 4 that the critical value of I_gF_b for the failure criterion is

$$(I_gF_b)^{crit} = I_g(\tau)\int_0^{\tau}(I_{SUB}/qS)\,dt = 1.215\times10^{13}\,A\cdot cm^{-2} \quad (3)$$

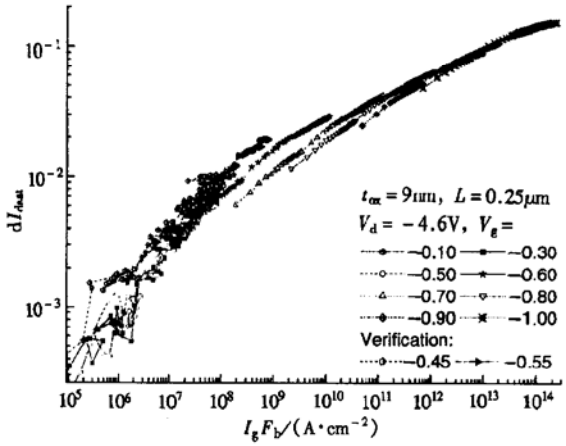

Fig. 3　Unified degradation model for p-MOSFETs with 9nm oxide and verification

To get the lifetime of the device, it must be known the corresponding stressing time when I_gF_b reaches $(I_gF_b)^{crit}$. where τ is the lifetime, q is unit electron charge and S is gate area of device.

It is found that I_gF_b has a power law relationship with respect to stressing time, as shown in Fig. 4. The curves of I_gF_b vs t in log-log scale can be fitted linearly very well. And the curves are parallel. It can be obtained from Fig. 6 that for any stress voltages

$$I_gF_b = A(V_g)\,t^n \quad (4)$$

where $A(V_g)$ is dependent on stress voltage and device fabrication processes, n= 0.89 is a constant that is dependent on device fabrication processes and structures. A and n are two fitting parameters.

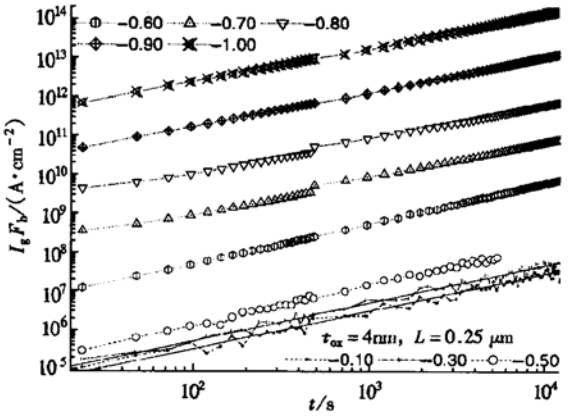

Fig. 4　Relationship between electron fluence F_b times gate current I_g and stress time

It can be seen from Eq. (3) and Eq. (4) that if A is known for any stress voltage. the lifetime can be calculated directly. So the degradation prediction method is changed to be the extrapolation method for the parameter A.

Figure 5 shows the relationship between log$A$ and gate voltage V_g. log$A$'s are the interceptions of

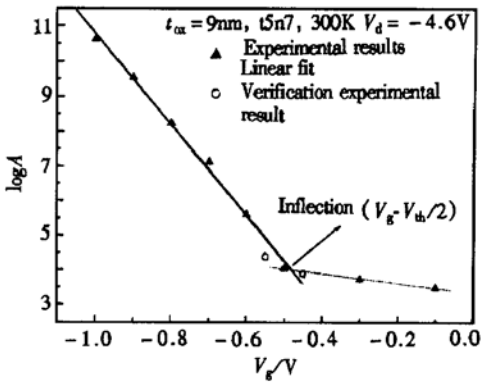

Fig. 5　Relationship between log$A$ and gate voltage V_g and verification

the fitted lines in Fig. 4. The linear fit line is also shown in this figure. The slope and intercept of $A(V_g)$ are not fixed for different stress voltages and have a inflexion at $|V_g| \approx |V_{th}|/2$, but a good linear relationship is found between log$A$ and V_g in the region of $|V_g| > 0.5$ and $|V_g| < 0.5$. The linear relationship of log$A$ for any gate voltage can be expressed as:

$$\log A(V_g) = B + CV_g \quad (5)$$

where $B = 4.6544$ and $C = -13.6157$ under the condition $|V_g| \geqslant |V_{th}|/2$, and $B = 3.3585$ and $C = -1.36445$ under the condition $|V_g| < |V_{th}|/2$.

The reason for the inflexion may be that the degradation mechanism changes from electron trapping to interface traps generation with the decrease of $|V_g|$ as discussed before. The inflection ($|V_g| \approx |V_{th}|/2$) is the exact turning point of the degradation mechanism.

To verify this model, we performed an experiment under stress voltages less and larger than $|V_{th}/2|$. Figure 3 also shows the I_{dsat} degradation characteristics under $V_g = -0.45$V ($|V_g| < |V_{th}|$) and $V_g = -0.55$V ($|V_g| > |V_{th}|$). It can be seen that under these stress voltages, the degradation is also aligned into the universal curve. Figure 5 also shows the comparison between verification experiment and the lifetime prediction model. The experimental results have a good agreement with the model. Therefore, this degradation model should be valid for the whole low voltage range.

4.2 4nm p-MOSFETs

Figure 6 shows the relationship between I_{dsat} degradation and electron fluence F_b in low voltage range with stress conditions ranging from lower to higher gate voltages. As expected, the universal characteristics are valid for various gate voltages. It means that the values of F_b are the same for different stress conditions when the I_{dsat} degradation reaches the failure criterion, though the lifetimes are different for different stress voltages. The failure criterion is set to be 10% of I_{dsat} degradation. It can be derived from Fig. 6 that the critical value of F_b for the failure criterion is

$$(F_b)^{crit} = \int_0^{\tau} I_{SUB}\,dt/qS = 1.345 \times 10^{25}\,cm^{-2} \quad (6)$$

To get the lifetime of the device, it must be known the corresponding stressing time when F_b reaches $(F_b)^{crit}$, where τ is the device lifetime.

From Fig. 7, it is found that F_b also has a power law relationship with respect to stressing time

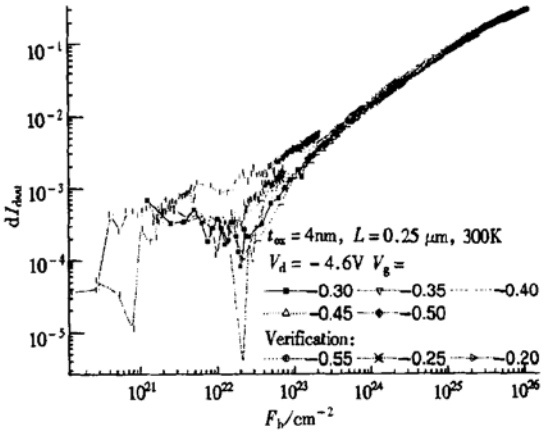

Fig. 6 Comparison of experimental results with verification and the other aging experimental results for 4nm

for p-MOSFETs with 4nm gate oxide. The curves of F_b vs t in log-log scale can be fitted linearly very well. And the curves are parallel. It can be obtained from Fig. 6 that for any stress voltages

$$F_b = A_1(V_g)\,t^n \quad (7)$$

where A_1 is a constant that is dependent on stress voltage and device fabrication processes, $n = 0.99$ is a constant that is dependent on device fabrication processes and structures. A_1 and n are two fitting parameters.

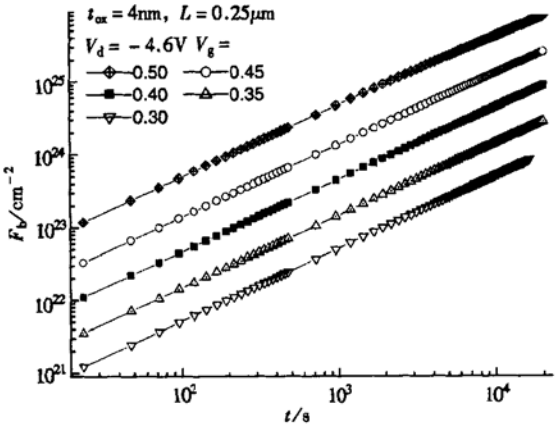

Fig. 7 Relationship between electron fluence F_b and stress time

It can be seen from Eq. (6) and Eq. (7) that if $A_1(V_g)$ is known for any stress voltage, the lifetime can be calculated directly. So the degradation prediction method is changed to be the extrapolation method for the parameter A_1.

Figure 8 shows the relationship between log$A$ and gate voltage V_g. Log$A$'s are the interceptions of F_h vs stressing time. A good linear relationship is found between log$A$ and V_g. The linear fit line is also shown in this figure. On this basis, the logA_1 for any drain voltage can be expressed as:

$$\log A_1(V_g) = B_1 + C_1 V_g \qquad (8)$$

where $B = 16.57168$ and $C = -10.32574$ are two constants those are dependent on device fabrication processes.

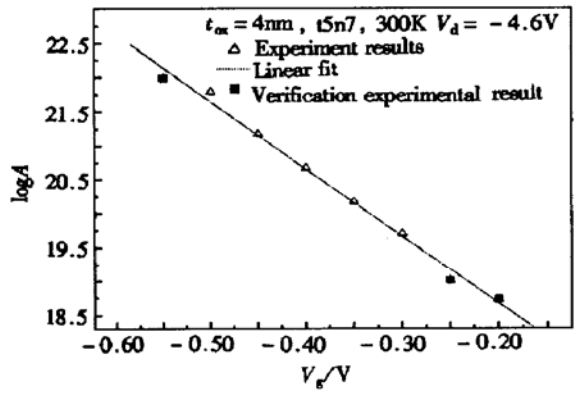

Fig. 8　Relationship between log$A$ and gate voltage V_g with verification

For 4nm device, the unified characteristics do not have inflexion at $|V_g| = |V_{th}/2|$ like 9nm. The reason for this is that its main mechanism of degradation does not change in the whole range of low voltage.

To verify this model, we performed an experiment under stress voltages less and larger than $|V_{th}|$. Figure 6 also shows the I_{dsat} degradation characteristics of 4.0nm p-MOSFET under $V_g = -0.25$V, $V_g = -0.20$V ($|V_g| < |V_{th}|$) and $V_g = -0.55$V ($|V_g| > |V_{th}|$). It can be seen that under these stress voltage, the degradation is also aligned into the universal curve. Figure 8 shows the comparison between verification experiment and the lifetime prediction model. The experimental result has a good agreement with the model. Therefore, this degradation model should be valid in the whole voltage range for p-MOSFETs with 4nm gate oxide.

5 Conclusion

Hot-carrier effects of p-MOSFETs with different oxide-thicknesses were studied under various stress voltages. All electrical parameters have a power law relationship with stress time, but degradation slope (n) is dependent on stress voltage (V_g) and has a linear relationship with the normalized stress voltage (V_g/V_{th0}). Different literature reported that the degradation mechanism is dependent on the thickness of gate oxide at the same normalized stress voltage (V_g/V_{th0}). Our results show that the degradation mechanism is dependent on the stress voltage for p-MOSFET with the same thickness.

For the devices with thicker oxides, I_{dsat} degradation has a close relationship with gate current times electron fluence ($F_h I_g$). For small dimensional devices, I_{dsat} degradation has a close relationship with electron fluence (F_h). Based on the universal relationship, an empirical degradation model was developed and verified through experiments. This degradation model is valid for p-MOSFETs with 0.25μm channel length and different gate oxide-thickness working in low voltage range. The model is only applicable in low voltage range and can not be extrapolated to the whole region. The possible reason is that p-MOS devices' degradation do not follow the time power law in intermediate and high voltage range.

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热载流子应力下 p-MOSFETs 在低栅电压范围的统一退化模型*

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摘要: 研究了低栅电压范围的热载流子统一退化模型. 发现对于厚氧化层的 p-MOSFETs 主要退化机制随应力电压变化而变化, 随着栅电压降低, 退化机制由氧化层俘获向界面态产生转变, 而薄氧化层没有这种情况, 始终是界面态产生; 此外退化因子与应力电压成线性关系. 最后得出了不同厚度的 p-MOSFETs 的统一退化模型, 对于厚氧化层, 退化由电子流量和栅电流的乘积决定, 对于薄氧化层, 退化由电子流量决定.

关键词: 热载流子效应; p-MOSFET; 退化模型; 电子流量

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