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Modeling and Parameter Extraction of VDMOSFET

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Abstract: A sub-circuit model for VDMOS is built according to its physical structure. Parameters and formulas describing the device are also derived from this model. Comparing to former results, this model avoids too many technical parameters and simplify the sub-circuit efficiently. As a result of numeric computation, this simple model with clear physical conception demonstrates excellent agreements between measured and modeled response (DC error within 5%, AC error within 10%). Such a model is now available for circuit simulation and parameter extraction.

Key words: vertical double-diffused MOSFET; parameter extraction; sub-circuit model; JFET effect
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NOTATIONS

I_{DS}	drain current
I_S	diode saturated current
I_{SD}	source to drain current
V_{DS}	drain-source voltage
V_{SD}	source-drain voltage
V_{GS}	gate-source voltage
V_{XS}	(x) drain-source voltage of MOSFET
V_{sat}	saturated voltage of MOSFET
V_{th1}	threshold voltage of MOSFET
V_{th2}	threshold voltage of JFET
V_C	thrift velocity saturation voltage
$V_{DD'}$	voltage on the bulk resistor
V_j	voltage on the diode
V_{jds}	D-S contact voltage
V_{jgd}	G-D contact voltage
k_{mos}	plus coefficient of MOSFET
k_{jfet}	plus coefficient of JFET
R_S	bulk resistance of the source region
R_d	bulk resistance of the drain region
R_{SD}	bulk resistance of the effective diode
C_{gs}	gate source capacitance
C_{gd}	gate drain capacitance
C_{ds}	drain source capacitance
C_{gs0}	gate source overlap capacitance
C_{gdc}	gate drain overlap capacitance
C_{jds}	zero-biased drain to source junction capacitance
C_{jgd}	critical gate drain junction capacitance
C_S	surface capacitance
m_{jds}	drain source exponential coefficient
m_{jgd}	gate drain exponential coefficient
θ	vertical field modulation coefficient
N_D	diode emission coefficient
C_{iss}	short-circuit input capacitance, common-source
C_{oss}	short-circuit output capacitance, common-source
C_{rss}	short-circuit reverse transfer capacitance, common-source

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1 Introduction

Vertical double-diffused MOSFET is a widely used device in power MOSFET family. Comparing to the bipolar junction devices, its better processing ability in high-voltage and high frequency circuits ensures a promising future. Therefore, a set of formula describing its DC and AC performance are needed for circuit simulation software. At present, the VDMOS model in circuit simulation[1] and parameter extraction software[2] applies MOS1 or MOS2 for DC part, which could not exhibit its specialty. On the other hand, sub-circuits of VDMOS are developed in many aspects like exterior character[3], charge sheet[4] and on-resistance[5] which introduced too many technical parameters or employed complex formulations unsuited for optimization or depicted only partial regions. Hence, a simple, efficient model with clear physically based conception is crutial for parameter extraction software.

2 Brief introduction to VDMOS

2.1 Structure and working principle

The structure of VDMOS cell is shown in Fig. 1. The first step of the technological fabrication is to grow an N^- epitaxy on the N^+ substrate. Then double-diffusion of N^+ and P forms both the source region and the channel, which locates in the transverse-diffused junction difference. Furthermore, precisely technical control shapes the device a short-channel one ($L = 1 \sim 2\mu m$). When a forwarding voltage turns on the device, electrons flow from the source region, crossing the inverse channel and the drift area, to the drain zone. A reverse biased source-to-drain voltage turns on the parasitic diode between P^+ substrate and N^- epitaxy. Here the device works in the forward source-drain bias state[6].

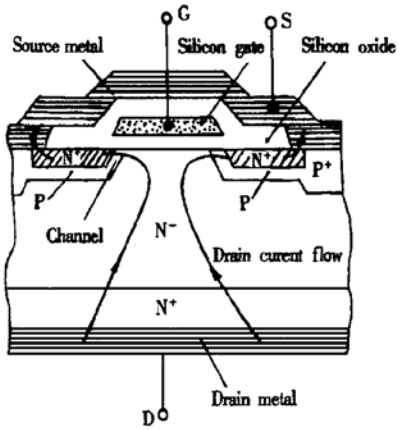

Fig. 1 Cell structure of VDMOS

2.2 Basic DC and AC property

2.2.1 Output characteristics (DC)

Figure 2 shows the typical output characteristics of VDMOS. It distinctly represents the special trait comparing to BJT and ordinary low power MOSFET. Of the six regions, Ohmic or linear ①, off-state ② and breakdown ④ region share common points with familiar MOSFET. In saturated region ③, the short channel length results in linear transconductance rather than a quadratic one. Not existing in traditional MOS, quasi-saturation region ⑥ is the most distinctive character of VDMOS. Due to the JFET effect[3], the output curves keep close to each other in high V_{GS}. As mentioned above, the forward drain-source biased region ⑤ also identifies the device[6].

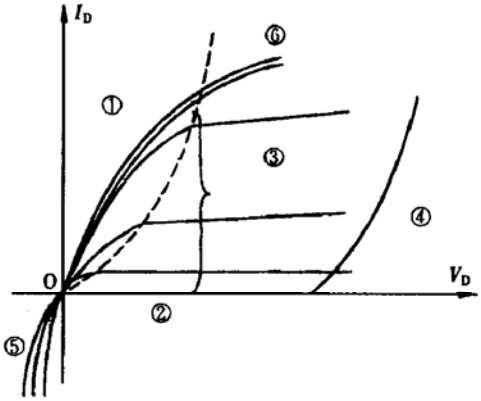

Fig. 2 Typical VDMOS output characteristics

2.2.2 Capacitance characteristics (AC)

Two types of interior capacitor, MOS and PN

junction, exist in VDMOSFET. Here C_{gs} is the gate source overlap capacitor, C_{ds} represents the potential barrier capacitance, and two capacitors, C_{gdc} and C_s, connect in series to form C_{gd}. Reflected in exterior circuits, these capacitors behave as three ones—short circuit input C_{iss}, short circuit output C_{oss} and short circuit reverse transfer C_{rss}. They confine the switching time of VDMOS, and their variation with voltage could be consulted in data sheet[7,8].

3 Sub-circuit and DC, AC model

According to the analysis above, there are two mechanisms that limit the drain current of MOSFET and JFET in forward-biased circuits. And VDMOS can be viewed as a parallel connection of MOSFET and diode when reverse-biased. We now may constitute the sub-circuit of VDMOS as Fig. 3. Its DC part is composed of one short-channel MOSFET, one JFET, one diode and body resistors (Note the point X is both the drain of MOS and the source of JFET); four capacitors compose its AC part. Apparently it is greatly simplified comparing to the one in Reference[3]. We also simulated the sub-circuit with software HSPICE, which showed fine accordance with Fig. 2. Details of the model formula are listed below.

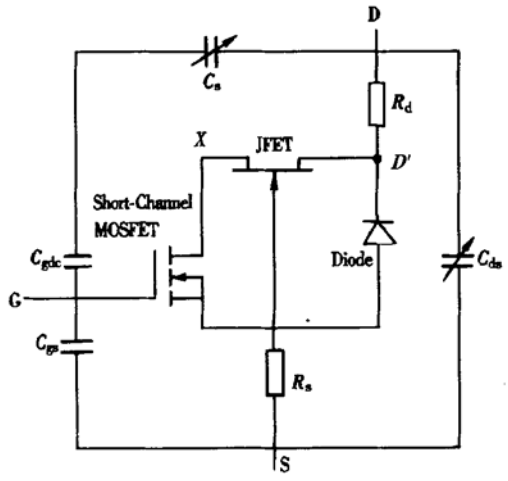

Fig. 3　Sub-circuit of VDMOS

3.1 DC forward-biased part

All the components are in serial connection with a same current (I_{DS}) flowing by. Therefore equations of each component are listed together to find the solution. When talking about short-channel MOSFET[9], vertical field modulation effect and thrift velocity saturation effect in drain port should be considered. To the parasitic JFET, even the simple quadratic formula[9] permits good result. The value of R_s is so small that even first-degree modification is acceptable. R_d could be treated as R_s, or be substituted into simultaneous equations. Detailed functions are:

MOS current, in which $x = V_{XS}$, namely the source-drain voltage of the short-channel MOSFET.

$$\begin{aligned} I_{DS} &= k_{mos}\frac{(V_{GS}-V_{th1})x-\frac{1}{2}x^2}{[1+\theta(V_{GS}-V_{th1})](1+x/V_C)} \\ &= f_1(x), \quad x < V_{sat} \qquad (1) \\ I_{DS} &= f_1(V_{sat}), \quad x \geqslant V_{sat} \qquad (1') \end{aligned}$$

where $V_{sat}=\dfrac{\sqrt{V_C^2+2V_C(V_{GS}-V_{th1})}-V_C}{1+\theta(V_{GS}-V_{th1})}$.

In which Eq. (1) for linear region, Eq. (1′) for saturated region.

JFET current, here $x = V_{XS}$, see annotation above.

$$\begin{aligned} I_{DS} &= k_{jfet}[(-x-V_{th2})(V_{DS}-x)-\frac{1}{2}(V_{DS}-x)^2] \\ &= f_2(x), \quad V_{DS} < -V_{th2} \qquad (2) \\ I_{DS} &= k_{jfet}(x+V_{th2})^2/2 = f_2'(x), V_{DS} \geqslant -V_{th2} \qquad (2') \end{aligned}$$

In which Eq. (2) for linear region, Eq. (2′) for saturated region

R_d current,

$$I_{DS} = V_{DD'}/R_d \qquad (3)$$

or first-degree modification

$$I_{DS} = I_{DS0}/(1+R_d g_{ds}) \qquad (3')$$

here g_{ds} is the drain-source transconductance.

Drain current I_{DS} is obtained by settling simultaneously the equation from Eq. (1) to Eq. (3) with Newton method. More specifically, we find the root of x first, then decide the working state of

the device according to the criterion above, finally calculate I_{DS} with Eq. (1) or Eq. (1′). The range of x already known ($0< x< V_{sat}$), root could be found more easily with halving method if R_d is viewed as first-degree modification. Computer simulation under this circumstance requires far less runtime, which ensures its feasibility in optimizing arithmetic. The former method is suited for high power VDMOS, whose saturation comes slowly because the influence of body resistance is greater than that of JFET. On the other hand, the simplified way is enough for low and medium VDMOS because the JFET effect is quite dominating that the drain current rises like parabola. Furthermore, the merit of these equations is self-evident. Adjusting V_C and θ to modify the saturated current, regulating k_{jfet} and V_{th2} to control the starting slope of the quasi-saturation region, handlers could easily estimate the initial value for parameter extraction.

3.2 DC reverse-biased part

The reversed-biased region, namely the forward source-drain biased region, could be viewed as parallel connection of diode and MOS. The formula of MOS is listed above as Eqs. (1) ~ (3), and the exponential form to describe diode is sufficient here:

$$I_{SD}= I_S(e^{V_j/N_D V_T}- 1)$$

Here $V_j= V_{SD}- I_{SD}R_{SD}$ is the actual voltage upon PN junction, $V_T= k_BT/q$[9]. Note that the signs of current and voltage are checked and required to be positive for NMOS in normal simulation software. So we replace the x-, y-coordinate by V_{SD} and I_{SD}.

3.3 AC capacitances

Capacitance characteristics are measured under zero-biased G-S voltage in data sheet. Then C_{gs} is the G-S overlap capacitor, irrelevant with V_{DS}. C_{ds} is actually the negative-biased PN junction capacitance because the P^+ substrate is short-circuited to N^+ source region. Composed of two parts (mentioned before), C_{gd} (C_{rss}) still falls exponentially after surface strong inversion occurs, which accounts for the condition of suddenly changing voltage. In that moment, the minority has little chance to be produced, so that the gate voltage is shielded mostly by ionized charge of the exhausted layer. After this happens, the surface type remains exhausted other than inverse, which matches the deep-exhausted case of C-V characteristics[10]. Formula below,

$$\begin{aligned} C_{gs} &= C_{GSO} \\ C_{ds} &= \frac{C_{jds}}{(1 + V_{DS}/V_{jds})^{m_{jds}}} \\ C_{gd} &= \frac{C_{GDC}C_S}{C_{GDC} + C_S},\ C_S = C_{jgd}\left(\frac{V_{jgd}(C_{GDC} + C_S)}{V_{DS}C_{GDC}}\right)^{m_{jgd}} \end{aligned} \tag{4}$$

Approximate exhaustion equation is applied instead of inversion to depict C_s. V_{DS} can be limited to a small but non-zero value to avoid numerical divergence.

The exterior capacitance is easy to obtained.

$$C_{iss} = C_{gs} + C_{gd};\ C_{oss} = C_{ds} + C_{gd};\ C_{rss} = C_{gd} \tag{5}$$

4 Computational results

Parameter extraction is a process that makes best agreement between measured data and modeled results by optimized arithmetic. Furthermore, the error of extraction vividly reflects the evaluation of the model.

NEWPEX system, developed by Institute of Microelectronics of Tsinghua University, is parameter extraction software for semiconductor devices. The optimized arithmetic integrated inside could complete the extraction task and error display.

Figure 4 shows the DC parameter extraction result, in which curves represent the model result while data points are from Motorola SMARTMOS[3,11]. Numeric error is 2.57% and the parameter value is listed in Table 1.

Figure 5 shows the AC parameter extraction result, in which curves represent the model result while data points are from Motorola BUZ80A[11]. The error is 4.64% and the parameter value is listed in Table 2.

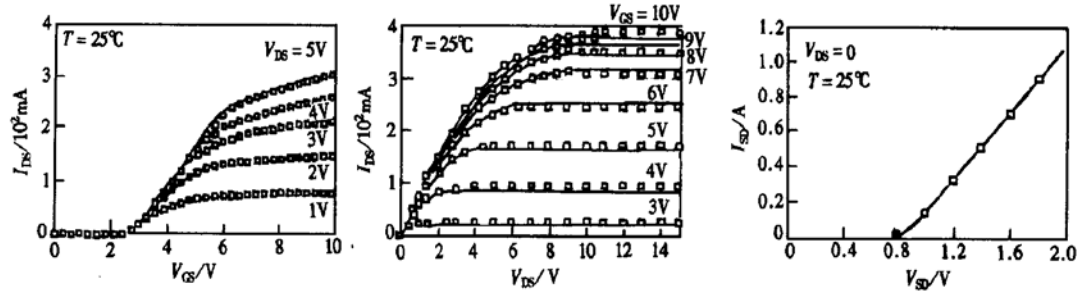

Fig. 4　VDMOS DC results

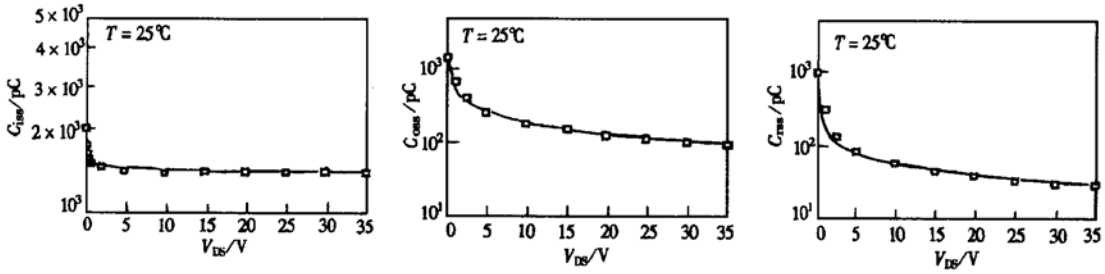

Fig. 5　VDMOS AC results

Table 1　DC extraction value

Parameter	V_{th1}/V	k_{mos}/(A·V^{-2})	V_C/V	θ/V	V_{th2}/V	k_{jfet}/(A·V^{-2})
Parameter value	2.22174	0.10678	1.99246	0.045797	−9.33235	0.010860
Parameter	R_S	R_d	I_S		R_{SD}	N_D
Parameter value	0.01	0.099998	9.998×10^{-16}		1.00001	1.00031

Table 2　AC extraction value

Parameter	C_{gso}/F	C_{gdc}/F	C_{jds}/F	V_{jds}/V
Parameter value	1.37805×10^{-9}	1.02319×10^{-9}	5.30979×10^{-10}	0.70795
Parameter	m_{jds}	C_{jgd}	V_{jgd}	m_{jgd}
Parameter value	0.49969	2.3×10^{-10}	1	0.650219

Furthermore, we compared our results with experimental data of various types (including Mini-MOS, Medium to High Power MOS) to verify that it is better than the ones in current software, which apply MOS1 or MOS2 model. The errors of sample devices retain less than 5%, quite viable for parameter extraction.

5　Conclusion

A new sub-circuit model for VDMOS was developed and presented in this paper. Numerical results show this simple, clear-concept model demonstrates excellent agreements between measured and modeled response. Strongpoint of the sub-circuit, which splits the on-resistance to several components, is apparent because relevant parameters can be adjusted respectively in approximating output curve. The model avoids too many technological parameters, while effectively simplifies the sub-circuit and retains good accordance (Error within 10% for AC and DC). It fills up the defect of former VDMOS model and suits for parameter extraction software.

References

[1] NIST Dynamic Electro-Thermal VDMOSFET Model, Developed by Al Hefner (NIST), 1997

[2] NEWPEX 1.0 Release, Technical Reference

[3] Fernandez J, Hidalgo S. Parameter extraction for a SPICE II VDMOS model. Proc IEEE 1989 Int Conference on Microelectronic Test Structure, 1989, 2(1): 35

[4] Victory J J, Sanchez J J. A static, physical VDMOS based on the charge-sheet model. IEEE Trans Electron Devices, 1996, 43(1): 157

[5] Kim S D, Kim I J. An accurate on-resistance model for low voltage VDMOS devices. Solid-State Electronics, 1995, 38: 345

[6] Rossel P. Power MOS devices. Microelectronics & Reliability, 1984, 24: 339

[7] Kim Y S, Fossum J G. Physical DMOST modeling for high-voltage IC CAD. IEEE Trans Electron Devices, 1990, 37: 797

[8] Wang Shouwu. VDMOSFET application reference book, First version, 1990

[9] Cao Peidong. Principle of transistor. Institute of Microelectronics of Tsinghua University, 1999

[10] Gu Zuyi. Semiconductor physics. First version, 1995

[11] MOTOROLA TMOS POWER MOSFET DATA SHEET

VDMOS 场效应晶体管电路模型的构造及参数提取

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摘要: 从 VDMOS 的物理结构出发建立子电路模型, 进而导出描述其交直流特性的参数及模型公式. 相对以往文献的结果, 该模型避免了过多工艺参数的引入, 同时对子电路进行了有效的简化. 在参数提取软件中的加载结果表明, 该模型结构简单, 运算速度快, 物理概念清晰, 拟合曲线与测试数据符合精度高(直流误差 5% 以内, 交流误差 10% 以内), 适于在电路模拟及参数提取软件中应用.

关键词: 垂直双扩散 MOS 管; 参数提取; 子电路模型; JFET 效应

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