

# A Novel Charge-Transfer Matching Cell for High-Precision Correlation and Low-Power

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**Abstract:** A novel matching cell-circuitry using charge-transfer circuit technique for high-precision correlation calculation is presented. The cell calculates the absolute value of the difference between two analog input voltages and amplifies the result. Amplification gain can be designed by the capacitance size in the cell and threshold voltage mismatch can be canceled automatically, thus high-precision operation of the circuit is achieved. The circuit can be operated with low power dissipation of about  $12\mu\text{W}$  at a frequency of 50MHz. Because of its simple structure and small silicon area, the matching cell is suitable to realize the correlation dealing with many template vectors that have many elements in a chip.

**Key words:** CMOS IC; amplification; capacitance-store

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## 1 Introduction

Correlation calculation is one of the fundamental functions for intelligent information processing that has been widely used, such as vector quantization and motion compensation of image compression, image or speech recognition, etc. In the circuit of the correlation calculation, the distance between template vector and input vector is computed and the resultant dissimilarity metric is used to search the most similar case. The so-called winner-take-all (WTA) circuit, which has been reported by many researchers<sup>[1~4]</sup>, searches the most similar case. A matching cell is important to calculate the metric used for WTA searching operation. There

are several metrics for correlation calculation. Due to the application or circuit configuration, another matching cell is used in calculating similarity metric such as template vector and input vector are matched closely. In the digital approach, matching operation is carried out by MPU. Multiple adders are sequentially used and the calculation results can be obtained as an output representing Manhattan distance. The computation power for calculation of the metric, however, is very expensive because of its iteration full nature. Aiming application in which the real-time response of a system is extremely important, it is useless for realizing correlation function. Alternatively, parallel architecture was also proposed, but hardware cost becomes large. In the analog approach, matching operation

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can be implemented in a small circuit cell and its full parallel processing nature enables a system to produce a real-time response. Two-valuation function is mainly used in real applications<sup>[5,6]</sup>. They are Manhattan distance and Euclidean distance computations. Employing the square-law of MOS-FET, the computation of Euclidean distance is realized for two analog inputs. The circuit in the Reference[6] realizes the Manhattan distance calculation by using a unique sequence. Therefore, maximum and minimum values are calculated firstly and the subtraction of the minimum value from maximum gives an output representing the Manhattan distance. However, these circuits are current-mode circuits. The performance of the circuits is restricted by passing current. In this respect, Ref. [6] might give an opportunity for low power circuit operation owing to its subthreshold region operation. On the other hand, purely voltage-mode circuit gives another opportunity for low power operation. The voltage-mode matching cell that realized by using a neuron MOS has been proposed<sup>[7]</sup>. In neuron MOS matching cell, however, there is a big problem with the output voltage signal attenuation. The resultant output must be amplified for WTA stage to execute a high accuracy operation. Inserting amplifier for each cell increases hardware cost. Generally, amplification accuracy is affected by parameter fluctuation and hence it imposes a limit on the precision of the total system. As a strategy for amplifying the signal with low-power, high-accuracy operation, charge-transfer type circuit has been reported in several articles<sup>[8,9]</sup>. The circuit technique is utilized as a preamplifier in a DRAM sense amplifier and CMOS configuration circuit for building the low-power, high-accuracy comparator in analog-to-digital converter (ADC). In this paper, a matching cell was developed for low-power high-precision correlation calculation employing the charge-transfer circuit technology. The circuit is not only with small silicon area but also with an amplification technique. It is robust to threshold voltage fluctuation.

## 2 Circuit configuration of charge-transfer matching cell

Figure 1(a) shows the circuit configuration of charge-transfer matching cell. It consists of two n-type floating-gate MOS (FGMOS for short) whose drain electrodes are both connected to the output node and source electrodes are connected to the transfer capacitance  $C_T$  through CMOS switches. Analog input voltages  $V_A$  and  $V_B$  applied to the input gates of the FGMOS through CMOS switches.

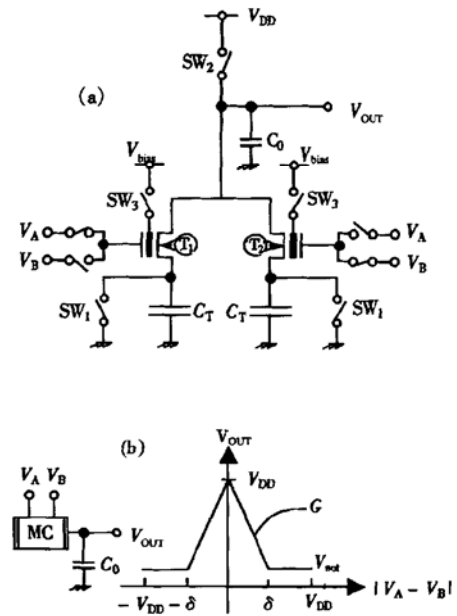


Fig. 1 Circuit configuration of charge-transfer matching cell

The expected relation of the input and output is shown as following.

$$V_{OUT} = \begin{cases} V_{DD} - G|V_A - V_B| & |V_A - V_B| < \delta \\ V_{Osat} & |V_A - V_B| > \delta \end{cases}$$

This is illustrated in Fig. 1(b). The circuit produces higher voltage when  $|V_A - V_B|$  becomes smaller and lower voltage when  $|V_A - V_B|$  becomes bigger, which represents degree of matching, i. e. similarity metric.

Figure 2 explains how the circuit works to calculate a degree of matching. The circuit operation

consists of three phases, namely, (1) reset phase, (2) pre-charge phase, and (3) amplified phase. In reset phase, the floating gates of the FGMOS are connected to the reset voltage ( $V_{\text{bias}}$ ) with two analog voltages,  $V_A$  and  $V_B$  being applied to the respective input gates. At the same time, the switches  $SW_1$  and  $SW_1'$  reset the source nodes of two FGMOS to be grounded with switch  $SW_2$  being turned

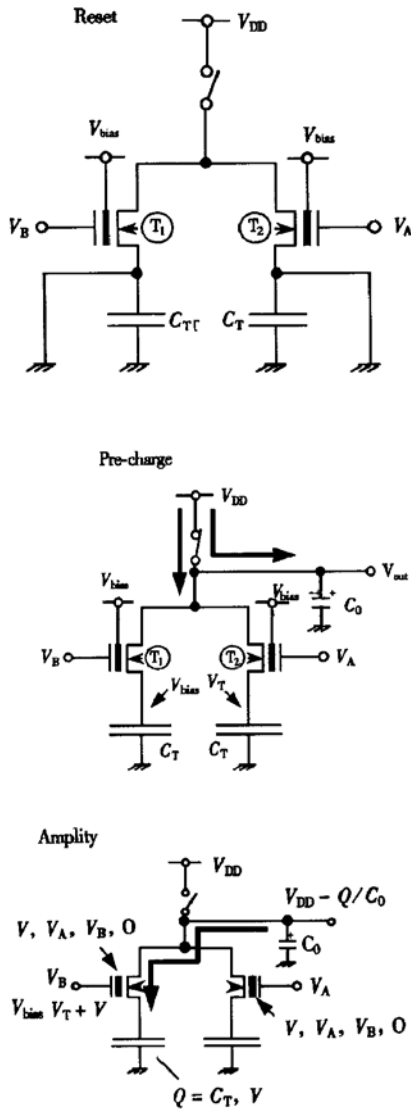


Fig. 2 Circuit operates to calculated a degree of matching

off. Then, in pre-charge phase, the switches  $SW_1$  and  $SW_1'$  are turned off and the switch  $SW_2$  is turned on. The source follower action of each FGMOS is activated to pre-charge the source node equal to be  $(V_{\text{bias}} - V_T)$ . At the same time, the out-

put terminal is reset to  $V_{\text{DD}}$ . Then the switch  $SW_2$  is turned off again and the pre-charge phase is terminated. Finally, in amplified phase, the switches  $SW_3$  and  $SW_3'$  are turned off and the floating gates are made electrically separating from reset voltages. Then, two input voltage are exchanged. It is assumed that  $V_A$  is greater than  $V_B$ . The FGMOS  $T_2$  is not activated, but the FGMOS  $T_1$  is activated as source follower because the gate voltage increases from  $V_B$  to  $V_A$ , that is  $\Delta V$ . Then the source node of FGMOS  $T_1$  is charged up to  $(V_{\text{bias}} - V_T + \Delta V)$ . Therefore, the charge  $\Delta Q = C_T \Delta V$ . Here,  $C_0$  is defined as the next input capacitance. So it can be mentioned that the gain  $G$  is described as  $C_T/C_0$ . It should also be noted that the threshold voltage mismatch of the FGMOS does not affect the accuracy of circuit output because it is canceled out by charging of the source nodes to  $(V_{\text{bias}} - V_T)$  in pre-charge phase.

### 3 Circuit operation analysis

In order to evaluate the basic performance of charge-transfer matching cell, the circuit operations were simulated by SPICE. At first, the input and output signal waveforms of the circuit as well as floating voltage waveforms are shown in Fig. 3(a). The operation frequency is set to 50MHz. Circuit operations have three phases, reset, pre-charge, and amplified. The capacitance ratio  $C_T/C_0$  is designed to be 10, and the parameter  $(V_{\text{bias}} - V_T)$  is 0. The difference of the input voltage  $\Delta V (|V_A - V_B|)$  is changed to be 250, 500, and 750mV. It is evident from the figure that the output is amplified for each  $\Delta V$  and output voltage at the end of amplified phase decreases corresponding to the increase of  $\Delta V$ .

Figure 3(b) shows the output voltage of the circuit as a function of  $(V_A - V_B)$ , namely  $\Delta V$ , at the floating gate terminal. The values of the capacitances  $C_T$  are designed 10 times that of  $C_0$  (Here,  $C_0$  is 5fF). The correct amplified output can be obtained in region where the difference of the inputs

is smaller than 1V. However, the output voltage is amplified by only about 3 times though  $C_T/C_0$  is designed as 10. The gain reduction is due to the parasitic capacitances. Moreover, the output voltage is saturated at 1.5V ( $V_{sat}$ ) in the region where the difference of the inputs is greater than 1V. This is because discharging process automatically stopped when the output voltage meets the source voltage of the activated FGMOS.

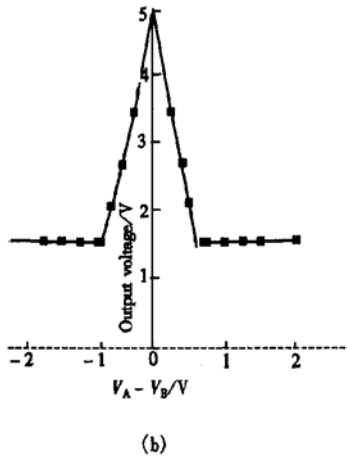
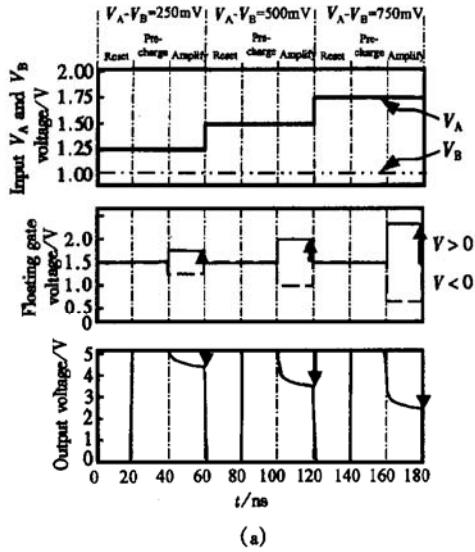
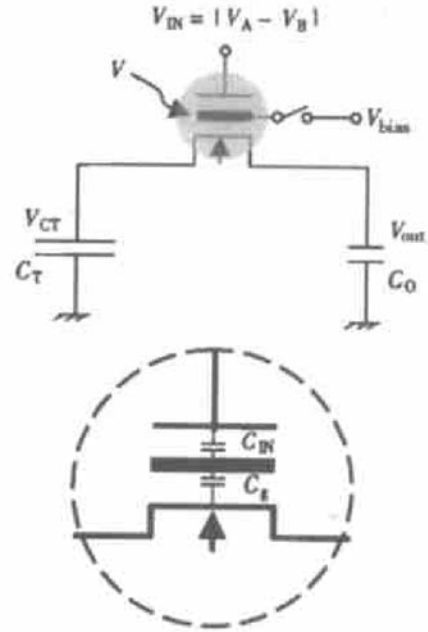


Fig. 3 Results of the circuit by HSPICE output characteristic of the circuit

Here, we calculate the output characteristic of the circuit from Fig. 4. Therefore, the major parameters such as the gain  $G$  and the saturated output voltage  $V_{osat}$  are described by only two designed pa-

rameters of the circuit, namely the transfer capacitance ratio  $C_T/C_0$  and the  $C_T$  pre-charge voltage ( $V_{osat} - V_T$ ). In the following calculation, the floating gate gain  $\gamma$  is assumed to be unity for simplicity and the voltage  $\Delta V$  is regarded to be equal to  $|V_A - V_B|$ .



$$\Delta V \frac{C_{IN}}{C_{IN} + C_g} \Delta V_{IN} = \gamma |V_A - V_B|$$

Fig. 4 Device model of charge-transfer matching cell

The output voltage saturation occurs when the voltage on the capacitor  $C_T$  and  $C_0$  reach to be the same voltage level. Moreover, the output voltage saturates in the region that  $\Delta V$  is greater than or equal to  $\delta$  ( $\delta$  is the voltage at which output saturates. See Fig. 2). So  $V_{CT}$  and  $V_{out}$  are equal to  $V_{sat}$  when  $\Delta V$  is equal to the value of  $\delta$ . Finally, we can determine the major parameters as follows.

$$G = \frac{C_T}{C_0}$$

$$\delta = \frac{V_D - V_{bias} - V_T}{1 + G}$$

$$V_{sat} = \frac{1}{1 + G} V_{DD} + \frac{G}{1 + G} (V_{bias} - V_T)$$

It can be seen from the formula for  $V_{sat}$  that the first term can be determined automatically by the gain  $G$  and supply voltage  $V_{DD}$ , but the second term can be removed by designing the parameter

( $V_{bias} - V_T$ ) to be zero volts. It also can be seen that when the gain  $G$  increased, the first term get close to zero and  $G/1+G$  in the second term gets close to 1. If the voltage ( $V_{bias} - V_T$ ) is designed to be closely 0, the second term becomes 0 no matter how large gain  $G$  is.

Figure 5 shows the calculation method for matching degree. The output voltage of matching cell of the charge-transfer type is determined by the value that is extracted from output node. Therefore, the summation result of the multiple outputs can be easily obtained by connecting their output nodes. The capacitance  $C_T$  can be designed to be small by minimizing the capacitance at the output  $C_0$  (including parasitic capacitances). Here, it is assumed that only the upper cell  $MC_1$  is active. In other words, the input voltage difference  $\Delta V$  occurs only in  $MC_1$  and 0 for the others. Therefore, the output voltage becomes the value, which is  $C_T/C_0$  designed in the single cell.

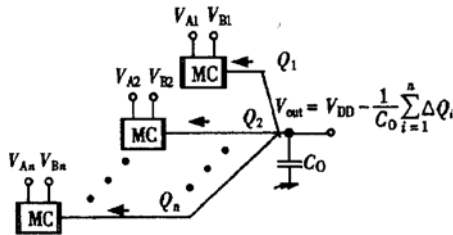


Fig. 5 Calculation method for matching degree

Figure 6(a) shows the photographs of the charge-transfer type matching cell test circuit. The circuit is designed by using  $1.5\mu\text{m}$  double-polysilicon double-metal CMOS process. The capacitance size ratio  $C_T/C_0$  is designed as 10. The area for the circuit is only about  $277\mu\text{m} \times 142\mu\text{m}$ . Therefore, it is suitable to realize the correlate dealing with many template vectors that have many elements in a chip because of its simple structure and small silicon area. Results of the test chip are shown in the Fig. 6(b). Test data are the same with HSPICE simulation, namely phase period is 20ns, the parameter ( $V_{bias} - V_T$ ) is 0, and the difference of the input voltage  $\Delta V$  is changed to be 250, 500, 750mV. From

Fig. 3 and Fig. 6(b), we can see the measurement results closely reproduce the behavior obtained by simulation. In this case, the circuit power is about  $12\mu\text{W}$ .

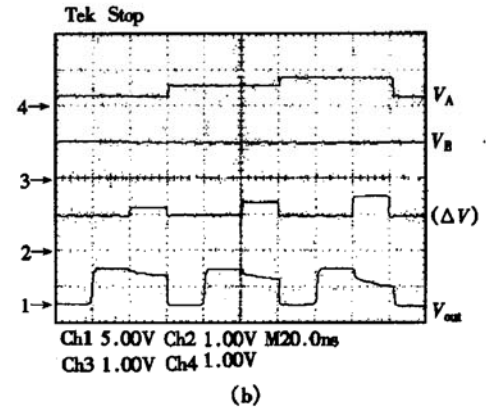
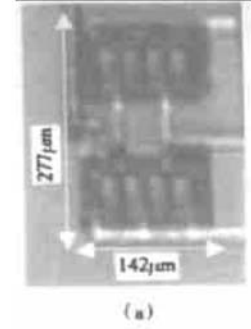


Fig. 6 Photographs of the charge-transfer type matching cell test circuit and results of the test chip

## 4 Conclusions

The charge-transfer matching cell for high-precision correlation calculation has been proposed. An amplified absolute value of difference between two analog input voltages can be obtained as the output and amplification gain can be designed by the capacitance size in the cell that is the value of the  $C_T/C_0$ , which include parasitic capacitance. The threshold voltage mismatch of the floating-gate MOS can also be canceled automatically by its source follower operation. It realizes the high-precision operation of total system. The circuit can be operated with low power dissipation of about  $12\mu\text{W}$  at a frequency of 50MHz. The matching cells are

suitable to realize the correlator dealing with many template vectors that have many elements in a chip because of its simple structure and small silicon area. It is essential for realizing intelligent information processing system.

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## 新型高精度低功耗电荷传输型匹配单元电路

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**摘要:** 提出了一种新型电荷传输型电路. 电路由 MOS 管及电容组成, 在计算相关量的匹配度时, 先计算出相关量的差值, 然后将此差值放大, 使电路的计算精度提高. 采用电荷传输型电路的方式, 大大降低了电路的功耗. 同时, 此电路还具有 MOS 管阈值偏差自动修正功能, 最大限度降低了制造工艺带来的误差.  $1.5\mu\text{m}$  双层多晶硅双层铝布线标准 CMOS 工艺所投样片的测试结果表明, 工作频率为 50Hz 时, 功耗仅为  $12\mu\text{W}$ .

**关键词:** CMOS 集成电路; 运算放大器; 电容存储

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