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# Oxide Thickness Effects on n-MOSFETs Under On-State Hot-Carrier Stress*

Hu Jing, Mu Fuchen, Xu Mingzhen and Tan Changhua

(*Institute of Microelectronics, Peking University, Beijing* 100871, *China*)

**Abstract**: Hot-carrier induced (HCI) degradation of surface channel n-MOSFETs with different oxide thicknesses is investigated under maximum substrate current condition. Results show that the key parameters $m$ and $n$ of Hu's lifetime prediction model have a close relationship with oxide thickness. Furthermore, a linear relationship is found between $m$ and $n$. Based on this result, the lifetime prediction model can be expended to the device with thinner oxides.

**Key words**: HCI; hot-carrier effect; oxide thickness effect; lifetime prediction model; device reliability
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## 1 Introduction

Society's increasing dependence on integrated microelectronics has brought urgency to the issue of reliability of the metal oxide semiconductor (MOS) structure. Of universal concern in analog, digital and memory technologies are the effects of hot carriers on the integrity of MOS gate oxides. One of the most serious problems posed by the continuing integration of silicon CMOS transistors into the submicrometer gate length range is the hot-carrier effect. Working on hot-carrier effects in MOSFETs started more than 30 years ago when the degradation problems induced by electric fields were first recognized[1]. After those early years of hot-carrier physics studies, a number of controversies arose concerning the physical mechanisms involved, until a picture finally evolved whose basic ideas are generally accepted today. The degradation due to hot-carriers has been variously attributed to trapped electrons, trapped holes and interface states. The degradation process is very complex and depends on the stress conditions as well as the device structure and the quality of the gate oxide[2].

Research groups are focused on two aspects of hot-carrier effects. They are degradation mechanism determining and lifetime prediction modeling. The lifetime prediction model based on lucky-electron model, which is proposed by Hu *et al.*, is widely used in hot-carrier induced (HCI) degradation[3]. But it can not be applied to the MOS devices with different oxide thicknesses because oxide thickness has some significant effects on hot-carrier effect[4~18]. In this paper. some n-MOSFETs

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Hu Jing male, was born in 1976, PhD candidate. His main research interest is the modeling and characterization of MOS devices and degradation of MOS devices under uniform, nonuniform stresses.

Mu Fuchen male, was born in 1970, PhD candidate. His main research interest is in small-size devices and reliability.

Xu Mingzhen female, was born in 1939, professor. Her current interests include physics and characterization of small dimensional devices and reliability of semiconductor material and devices.

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with different oxide thicknesses were stressed under $V_g = V_d/2$ condition. Oxide thickness effects on the key parameters of the lifetime prediction model[3] were investigated.

## 2 Model for n-MOSFETs under intermediate gate voltage stress

### 2.1 Model description

Device degradation is typically measured by the amount of saturated drain current degradation $\Delta I_{dsat}/I_{dsat0}$ ($I_{dsat0}$ is the fresh saturated drain current $I_{dsat}$), threshold voltage shift $\Delta V_t$, or transconductance degradation. They all exhibit the same power law behavior with respect to time. Here we generalize the degradation by using the symbol $\Delta D$. $\Delta D$ may be interchangeably replaced by any of the three degradation parameters in the following equations.

Under dc static stressing conditions, the amount of degradation as a function of time is given by[3]

$$\Delta D = A t^n \tag{1}$$

where

$$A = C_1 \left[ \frac{I_d}{W} \exp(-\Phi_{it}/q\lambda E_m) \right]^n \tag{2}$$

where $\Phi_{it}$ is the critical energy required for the creation of interface traps, $\lambda$ is the electron mean free path, $E_m$ is the maximum lateral channel field, $W$ is the device width, $I_d$ is the drain current, $C_1$ are dependent on the processing technology and $n$ is related with device degradation mechanism and fabrication process. Also from[3]

$$\frac{I_{sub}}{I_d} = C_2 \exp(-\Phi_i/q\lambda E_m) \tag{3}$$

where $\Phi_i$ is the critical energy required for impact ionization, $I_{sub}$ is the substrate current, and $C_2$ is a process technology constant. Equation (3) can be rearranged in the following equation.

$$\exp(-\Phi_{it}/q\lambda E_m) = [\exp(-\Phi_i/q\lambda E_m)]^{\Phi_{it}/\Phi_i} = \left[ \frac{I_{sub}}{C_2 I_d} \right]^m \tag{4}$$

$$m = \frac{\Phi_{it}}{\Phi_i} \tag{5}$$

By substituting the exponential term in Eq. (2) with Eq. (4) and merging all constants into the parameter $H$, we can obtain

$$A = \left[ \frac{I_d}{WH} \left( \frac{I_{sub}}{I_d} \right)^m \right]^n \tag{6}$$

$$H = \frac{C_2^n}{C_1^{1/n}} \tag{7}$$

where $n$, $m$ and $H$ are extracted parameters and are dependent on device processing technology. Thus, the expression for device degradation from Eq. (1) becomes

$$\Delta D = \left[ \frac{I_d}{WH} \left( \frac{I_{sub}}{I_d} \right)^m \right]^n t^n \tag{8}$$

From Eq. (7), we can obtain the expression for dc device lifetime $\tau$ from the fact that $\Delta D_f \equiv A\tau^n$ ($\Delta D_f$ is the amount of degradation at which device lifetime is defined):

$$\tau = BWI_{sub}^{-m} I_d^{m-1} \tag{9}$$

$$B = H \Delta D_f^{1/n} \tag{10}$$

In this model there are three key parameters. They are $n$, $m$, and $H$. The parameter $m$ is related with device fabrication process and the gate to drain transverse field. The parameter $H$ is process and device structure dependent. All these parameters can be extracted from experiments.

### 2.2 Experiment

Surface channel n-MOSFETs with 4, 5, 7, and 9nm gate oxides and 15/1 of $W/L$ were employed in experiments. All the experiments were performed at $V_g = V_d/2$ stress mode and at room temperature.

Figure 1 shows the degradation characteristics of saturated drain current ($I_{dsat}$) and threshold voltage ($V_t$) shift with respect to time. As expressed in Eq. (1), the degradation follows a time-power law, except for longer stress time or higher degradation level. The gradients are in the range of 0.7~0.9 and 0.9~1.3 for $I_{dsat}$ degradation and $V_t$ shift, respectively. They are a little larger than that reported (0.5) in literature. This probably is due

to electrons trapping in the gate oxide. Taking 10% of $I_{dsat}$ degradation and 0.1V of $V_t$ shift as failure criterions, lifetimes were derived from Fig. 1.

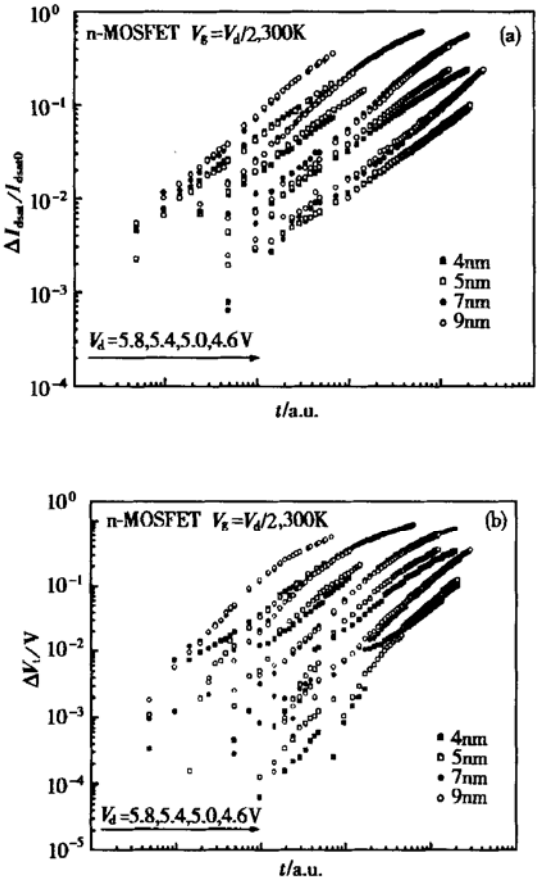


Fig. 1 $I_{dsat}$ and $V_t$ degradation with stress time of n-MOSFETs under $V_g = V_d/2$ stress mode (a) $I_{dsat}$ degradation, $n$: 0.7~ 0.9; (b) $V_t$ degradation, $n$: 0.9~ 1.3

## 2.3 Parameter extraction

Rearranging terms of Eq. (8), yields,

$$\frac{\tau I_d}{W} = B\left(\frac{I_{sub}}{I_d}\right)^{-m} \tag{11}$$

$$H = \frac{B}{\Delta D_f^{1/n}} \tag{12}$$

By plotting $\tau Id/W$ vs $I_{sub}/I_d$ in a log-log scale, the parameters $m$ and $B$ can be obtained from the slope and the interception. Once $B$ is obtained, $H$ can be extracted by Eq. (12). The parameter $n$ can be extracted from device degradation characteristics.

Figure 2 is a plot of $\tau Id/W$ vs $I_{sub}/I_d$ under $V_g = V_d/2$ stress mode. $I_{dsat}$ and $V_t$ are lifetime monitors for Fig. 2 (a) and (b), respectively. The substrate and drain current are the initial values measured at the beginning of stressing. Each data set for a specified oxide thickness follows a straight line very well. Therefore, two key parameters $m$ and $B$ can be obtained from this figure directly. The values of the parameter $m$ derived either from $I_{dsat}$ degradation or from $V_t$ shift are all in the range of literature reported (2.9~ 3.7)[3, 19~ 21]. Moreover, the values of $m$ are almost the same for these two lifetime monitors, especially for 4 and 5nm devices. This is similar to Ref. [21].

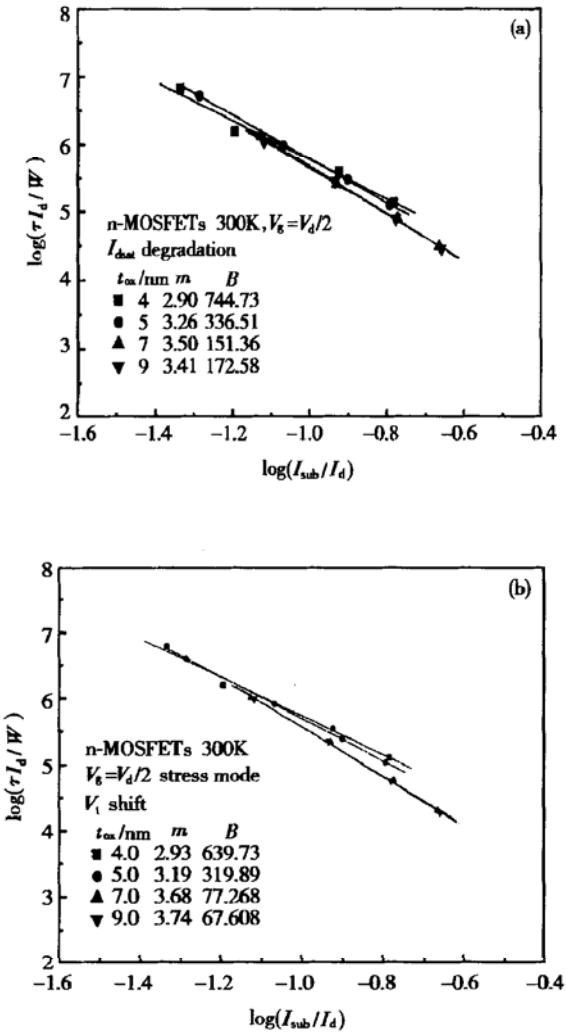


Fig. 2 $\tau I_d/W$ vs $I_{sub}/I_d$ plot for (a) $I_{dsat}$ degradation and (b) $V_t$ degradation under $V_g = V_d/2$ stress mode The straight lines are fitted results. Parameters $m$ and $B$ are derived from this figure directly.

## 3 Oxide thickness effects on the model parameters

It can be seen from Fig. 3 that the parameter $n$ and $m$ increase with oxide thickness increasing. This is probably due to the exact oxide thickness dependence of device degradation mechanism or oxide thickness dependence of $\Phi_{it}$ (the critical energy for interface trap creation) or both. It can be seen from Fig. 4 that the parameter $m$ has a linear relationship with the gradient $n$. The gradient $n$ implies device degradation mechanism. Therefore, the oxide thickness dependence of the parameter $m$ (or $\Phi_{it}$) may be due to device degradation mechanism. Parameter $m$ for devices with thinner oxides can be extrapolated from Fig. 4. The linear relationship between $m$ and $n$ is very useful for lifetime prediction. The lifetime prediction model can be expended to the devices with thinner oxides. The physical explanations for the oxide thickness dependence of parameter $m$ are not at hand. Thus it still needs study further.

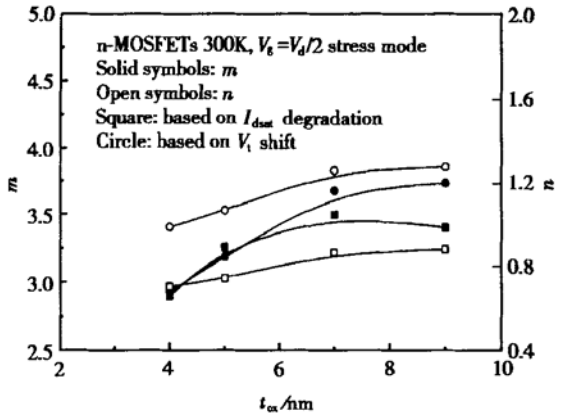


Fig. 3　Oxide thickness dependence of parameter $m$ (solid symbols) and the gradient $n$(open symbols) as a function of lifetime monitor　They both increase with oxide thickness increasing.

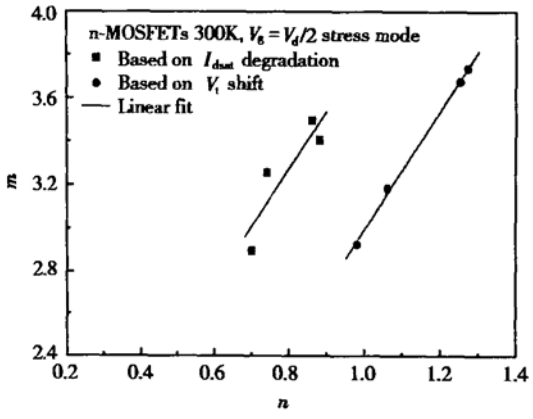


Fig. 4　$m$ vs $n$ as a function of lifetime monitor　A linear relationship is found between the parameter $m$ and $n$ taking $I_{dsat}$ and $V_t$ as lifetime monitors.

## 4 Discussion and conclusions

The oxide thickness effects on HCI reliability have been a subject of research recent years[4~18]. With the reduction in oxide thickness, less degradation in terms of charge trapping (as measured using threshold voltage shift) has been reported[7,12~15]. This can be attributed to reduced volume available for charge trapping[16] and tunneling of carriers from the oxide into the gate and substrate[4,17,18]. Recent work showed that the addition of Coulomb repulsion between the already trapped electrons and the injected ones[5] may play an important role in modeling HCI degradation. Consequently, as shown in Fig. 3, the gradients for the devices with thinner oxides are smaller than those for the devices with thicker oxides.

Based on the linear relationship between $m$ and $n$, as shown in Fig. 4, once the parameter $n$ is known, the parameter $m$ can be extrapolated directly. It is not necessary to stress the device till it fails. Though different oxide thicknesses give rise to different model parameters, the lifetime prediction model in Ref. [3] is still valid if the parameters $m$ and $n$ for the oxide thickness interested are employed.

Using n-channel MOSFETs with oxides ranging from 4 to 9nm, oxide thickness effects were studied in terms of the key parameters of Hu's lifetime prediction model. It shows that the model parameters $m$ and $n$ are related with oxide thickness. $m$ has a linear relationship with $n$. Based on this re-

sult, the lifetime prediction model can be expended to n-MOS transistors with thinner oxides.

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# 开态热载流子应力下的 n-MOSFETs 的氧化层厚度效应*

胡　靖　穆甫臣　许铭真　谭长华

(北京大学微电子所，北京　100871)

**摘要**：在最大衬底电流条件下($V_g = V_d/2$)，研究了不同氧化层厚度的表面沟道 n-MOSFETs 在热载流子应力下的退化. 结果表明，Hu 的寿命预测模型的两个关键参数 $m$ 与 $n$ 氧化层厚度有着密切关系. 此外，和有着线性关系，尽管不同的氧化层厚度会引起不同的模型参数，但是如果对于不同厚度的氧化层，采用不同的 $m$ 与 $n$，Hu 的模型仍然成立. 在这个结果的基础上，Hu 的寿命预测模型能用于更薄的氧化层.

**关键词**：HCI；热载流子效应；氧化层厚度效应；寿命预测模型；器件可靠性

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胡　靖　男，1976 年出生，博士研究生，从事小尺寸器件的可靠性研究.

穆甫臣　男，1970 年出生，博士研究生，从事小尺寸器件的可靠性研究.

许铭真　女，1939 年出生，教授，从事小尺寸器件的特性和物理以及半导体材料的可靠性.

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