第 23 卷第 7 期　　半 导 体 学 报　　Vol. 23, No. 7
2002 年 7 月　　CHINESE JOURNAL OF SEMICONDUCTORS　　July, 2002

Strained Si-Channel Heterojunction n-MOSFET*

Shi Jin, Huang Wentao and Chen Peiyi

(Institute of Microelectronics, Tsinghua University, Beijing 100084, China)

Abstract: The process parameters are adjusted and the process procedure is simplified on the basis of precursor's work and the strained Si-channel SiGe n-MOSFET is fabricated successfully. This n-MOSFET takes the strained Si layer(which is deposited on the relaxed SiGe buffer layer) as current channel and can provide a 48.5% improvement in electron mobility while keeping the gate voltage as 1V.

Key words: strain; SiGe; transconductance; mobility
EEACC: 2560R
CLC number: TN386　　**Document code:** A　　**Article ID:** 0253-4177(2002)07-0685-05

1 Introduction

As the silicon-based technology has developed to its limit, it brings an urgent to search for a procedure that can maintain the development of the nowadays technology. SiGe material can be a candidate. It can not only tailor the carrier distribution with the quantum well formed by band mismatch, but also improve the carrier mobility by the strain effect in its band structure.

The n-MOSFET, which has a strained surface Si-channel, belongs to the Ⅱ type band structure. Though suffering from the surface scattering, the strain effects in the surface silicon layer can lead to the enhancement of electron mobility and hence result in a higher transconductance.

2 Material and device fabrication

As a foundation, we should first confirm that the material to construct a device is "perfect". The word "perfect" reflects two standards: satisfied alloy quality and defect density as less as possible. Alloy quality is the basis of strain effect and also the guarantee of realization of SiGe device while defect density will dramatically affects the device performance.

The DCXRD result of SiGe material (sample 1120) is shown in Fig. 1 which indicates good alloy quality.

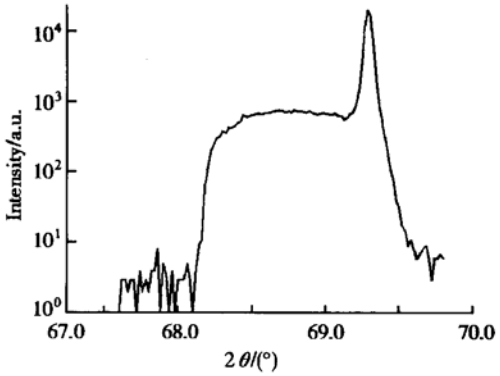

Fig. 1　DC XRD result of SiGe material

* Project supported by National Natural Science Foundation of China(No. 69836020), National Ninth 5-Year Science and Technology Program(No. 97-760-03-01)
Shi Jin　male, was born in 1978. His research subject is mainly about the SiGe device.
Received 2 November 2001, revised manuscript received 11 January 2002

Figure 2 is the TEM result of the device profile, from which we can see that there are many defects and thread dislocations in the SiGe grading layer, but few defects or thread dislocations in the SiGe buffer layer. It seems that the SiGe grading layer constrains all the defects and thread dislocations inside while keep the SiGe buffer layer and strained silicon layer "perfect". Figure 3 is the SIMS result of Ge grading.

Fig. 2 TEM result of SiGe layer

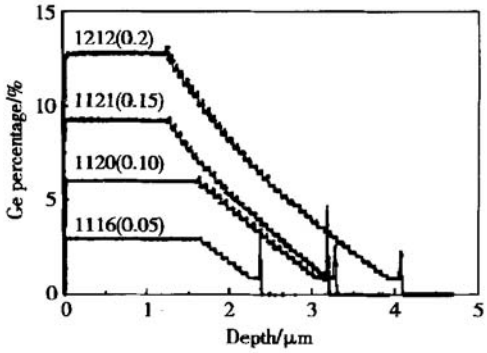

Fig. 3 SIMS result of Ge grading

We grew the SiGe layer in four kinds of conditions which should provide 5%, 10%, 15% and 20% SiGe buffer layers that corresponded to sample 1116, 1120, 1121, 1212 respectively. As shown in Fig. 3, the SIMS result was lower than that expected. The Ge composition decreased in the SiGe grading layer from its top value down to zero. The result of roughness test shown in Fig. 4 and Fig. 5 is 8.67nm.

For the simplicity of process, we took a simple device structure (Fig. 6) for the fabrication of strained Si-channel n-MOSFET. All the following layers were grown in the

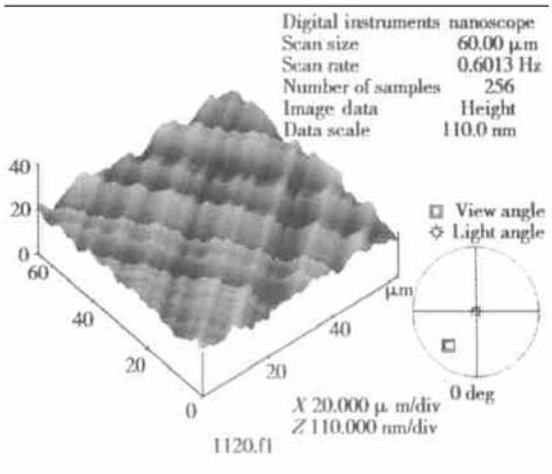

Fig. 4 Roughness diagram of sample 1120

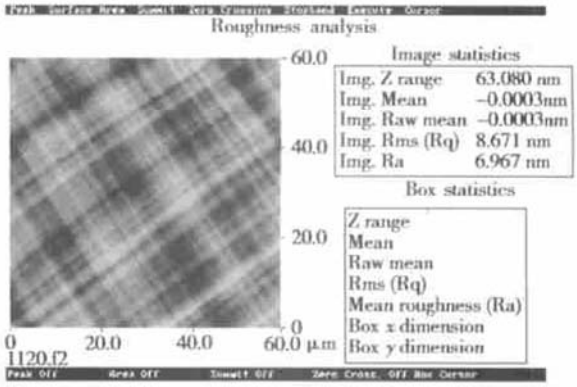

Fig. 5 AFM result of sample 1120 (0.10)

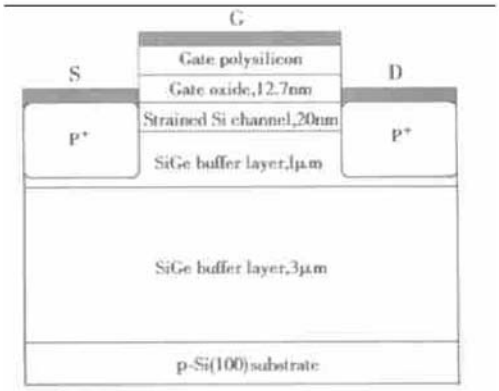

Fig. 6 Structure of SiGe n-MOSFET

home-made HV/CVD equipment. The n-MOSFET fabrication started with φ100mm〈100〉 p-type Si substrates. We used a 3μm-SiGe grading layer to eliminate the defects and thread dislocations. Upon the SiGe grading layer was the 1μm-SiGe buffer layer with different Ge contents. Then there was the strained Si layer with a thickness of

20nm. The gate oxide thickness was 12.7nm. During the whole process, high temperature was avoided as to prevent the strained layer from being relaxed. So, instead of the thermal oxidation, we took LTO as insulator spacer, which lasts for 60min, 850 ℃. Ion implantation and self-aligned technology were applied in the formation of source, drain and gate. The annealing condition was 850 ℃, 20min.

Following these steps, we got a family of SiGe devices, which indicated an increase in the electron mobility when the Ge fraction increased.

3 DC characteristics

After the test of the transition characteristics and the output characteristics of each device, we can get the corresponding threshold voltage and electron mobility by the formulas (1) and (2).

$$V_T = x\,\mathrm{int}\,\mathrm{ercept}(\max\,\mathrm{slope}(\mathrm{curve}(V_{GS}, I_{DS}))) - \mathrm{abs}(\mathrm{ave}(V_{DS}))/2 \quad (1)$$

$$\mu_0 = \frac{2L}{W} \times \frac{I_{DS1} - I_{DS2}}{C_{OX}[(V_{GS1} - V_T)^2 - (V_{GS2} - V_T)^2]} \quad (2)$$

$$G_m = \frac{I_{DS1} - I_{DS2}}{\Delta V_{GS}} = k(2V_{GS} + 1 - 2V_T) \quad (3)$$

We can directly get the transconductance G_m from the output characteristics. Here we present the formula (3) just to explain the phenomenon we will discover later. From this formula, we can see that the transconductance is also affected by the threshold voltage. So the larger V_T of Si sample will lead to relatively larger transconductance.

Tables 1 and 2 show the extracted G_m and electron mobility under different gate voltage. Figures 7 and 8 show the characteristics of G_m-V_{GS} and μ-V_{GS}. The G_m extracted here is only an average

Table 1　Extracted G_m under different V_{GS}

Device sample	G_m/(mS·mm^{-1}) V_{GS}= 1V	G_m/(mS·mm^{-1}) V_{GS}= 2V	G_m/(mS·mm^{-1}) V_{GS}= 3V	G_m/(mS·mm^{-1}) V_{GS}= 4V
1121(0.13)	14.3	35.7	45.7	53.6
1120(0.10)	7.14	28.6	42.9	46.4
1116(0.06)	14.3	25.7	31.4	41.4
Si	24.3	34.3	40.0	48.6

Table 2　Extracted electron mobility under different V_{GS}

Device sample	V_T/V	μ_{eff}/(cm^2·V^{-1}·s^{-1}) V_{GS}= 1V	μ_{eff}/(cm^2·V^{-1}·s^{-1}) V_{GS}= 2V	μ_{eff}/(cm^2·V^{-1}·s^{-1}) V_{GS}= 3V	μ_{eff}/(cm^2·V^{-1}·s^{-1}) V_{GS}= 4V
1121(0.13)	-0.6	303	239	197	141
1120(0.10)	-0.4	284	230	174	142
1116(0.06)	-0.4	251	201	163	130
Si	-1.0	204	182	160	142

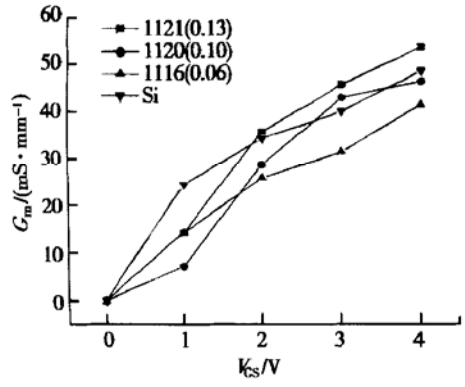

Fig. 7　G_m-V_{GS} curves

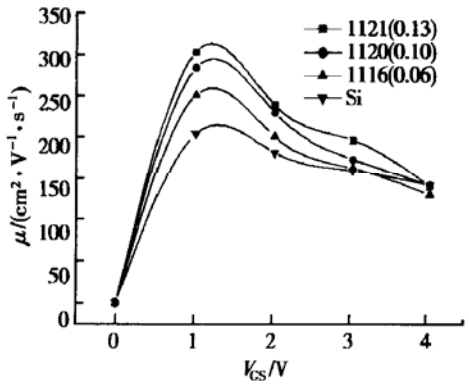

Fig. 8　μ-V_{GS} curves

value of saturate transconductance which equals to the difference between two output drain current under different gate voltage. The tab 1116, 1120, 1121 and 1212 each corresponds to sample whose Ge percentage is 5%, 10%, 15% and 20% respectively.

As we can see, the transconductance G_m does not increase with the Ge fraction because the G_m is also a function of the threshold voltage. But the extracted electron mobility increases visibly when the Ge fraction increases. Comparing to the silicon sample, there will be a 48.5% improvement at most in electron mobility.

Figures 9, 10, 11 and 12 present us with the output characteristics of SiGe HMOSFET with different Ge fraction. We apply a 0~ 5V sweep voltage on the drain electrode and a 0~ 4V step voltage on the Gate electrode (The x-coordinate is 0.2mA/ div and the y-coordinate is 0.5V/ div; the voltage step is 1V). For improper implantation dose, the threshold voltage of these n-MOSFET is negative while the normal threshold voltage should be positive. So we can see the first output line which indicates V_{GS}= 0V does not overlap with x-axis, which means there has been leakage current between source and drain when V_{GS}= 0V.

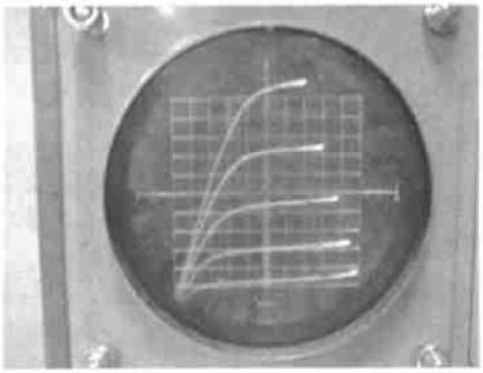

Fig. 9 Si sample

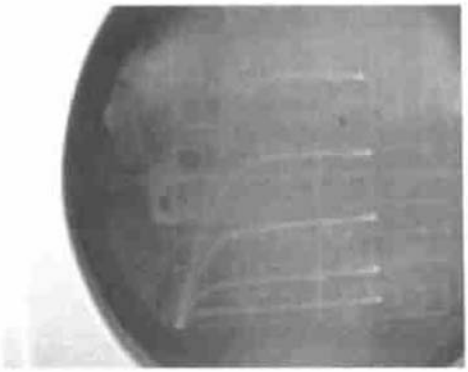

Fig. 10 1116 sample(0.06)

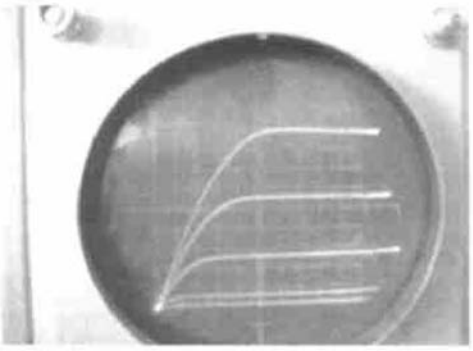

Fig. 11 1120 sample(0.10)

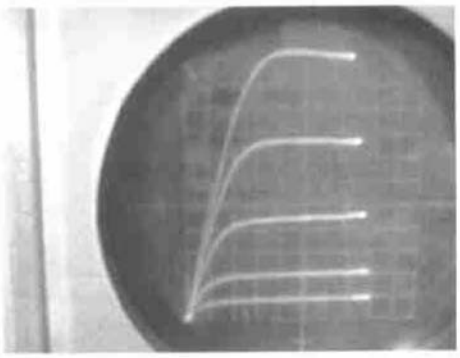

Fig. 12 1121 sample(0.13)

The extracted V_T is only an approximate value here. We can estimate the error caused by this approximation. We can see in formula (2) that V_T is functioning with the aid of V_{GS}. So when a sample device achieves the saturate transconductance (traditionally at 4~ 5V gate voltage), the V_T induced error in μ_0 calculation is quite trivial. Theoretically, we can rewrite formula (2) in this form:

$$\mu_0 = \frac{2L}{W} \times \frac{I_{DS1} - I_{DS2}}{C_{OX}(V_{GS1} + V_{GS2} - V_T)(V_{GS1} - V_{GS2})} \tag{4}$$

which indicates that the V_T influence is trailed off by the sum of V_{GS1} and V_{GS2}. For example, even in case of the smallest sum of V_{GS1} and V_{GS2}, a 0.2V error to V_T can cause only 6.7% error in the final μ_0 value. If we take

0.2V as the error bar of V_T extraction which is a reasonable assumption to our test (we took 0.2V as the gate voltage increase step), the max error of μ_0 will not exceed 7%.

4 Conclusions

After the construction and test of SiGe n-MOSFET, we can see that these devices have high mobility in the channel. As stated in some materials, the low field electron mobility in the strained Si channel can even reach $2500 cm^2/(V \cdot s)$, which can lead to a better performance. As an improvement, we suggest that the SiGe layer should be deposited after the buffer layer has been polished and then grow the strained Si layer on it so as to minimize the surface roughness.

Acknowledegment The authors would like to thank Doctor Luo Guangli for his contributions to this project.

References

[1] Li Chen, Zhu Peiyu, Luo Guangli, et al. SiGe PMOSFET's favorable for faboicating CMOS. Chinese Journal of Semiconductors, 2001, 22(7): 929[黎晨, 朱培喻, 罗广礼, 等. 一种适合制作CMOS的SiGe PMOSFET. 半导体学报, 2001, 22(7): 929]

[2] Verdonckt-Vandebroek S. SiGe-channel heterojunction p-MOSFET's. IEEE Trans Electron Devices, 1994, 41(1): 90

[3] Dong Zhiwei, Li Chen, Chen Peiyi, et al. The influence of GeSi MOSFET longitudinal stucture on device performance. Chinese Journal of Electronics, 2000, 28(8): 144

[4] Welser J. Electron mobolity enhancement in strained-Si n-type metal-oxide-semiconductor field-effect transistors. IEEE Electron Device Lett, 1994, 15(3): 100

[5] Maiti C K. Strained-Si heterostructure field effect transistors. Semicond Sci Technol, 1998, 13: 1225

[6] Maiti C K. Hole mobility enhancement in strained-Si pMOSFETs under high vertical field. Solid-State Electronics, 1997, 41(12): 1863

[7] Nayak D K. High-mobility strained-Si PMOSFET's. IEEE Trans Electron Devices, 1996, 43(10): 1709

[8] Sadek A. Design of Si/SiGe heterojunction complementary metal-oxide-semiconductor transistors. IEEE Trans Electron Devices, 1996, 43(8): 1224

应变 Si 沟道异质结 NMOS 晶体管*

史　进　黄文涛　陈培毅

(清华大学微电子学研究所, 北京　100084)

摘要: 通过参数调整和工艺简化, 制备了应变 Si 沟道的 SiGe NMOS 晶体管. 该器件利用弛豫 SiGe 缓冲层上的应变 Si 层作为导电沟道, 相比于体 Si 器件在 1V 栅压下电子迁移率最大可提高 48.5%.

关键词: 应变; SiGe; 跨导; 迁移率

EEACC: 2560R

中图分类号: TN386　　**文献标识码**: A　　**文章编号**: 0253-4177(2002)07-0685-05

* 国家自然科学基金(批准号: 69836020), 国家九五重点科技攻关(No. 97-760-03-01)资助项目

史　进　男, 1978 年出生, 硕士研究生, 研究方向为 SiGe 器件.

2001-11-02 收到, 2002-01-11 定稿